AUDIO AND RADIO PRODUCTS

1st EDITION

July 1987

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS MICROELETTRONICA SpA. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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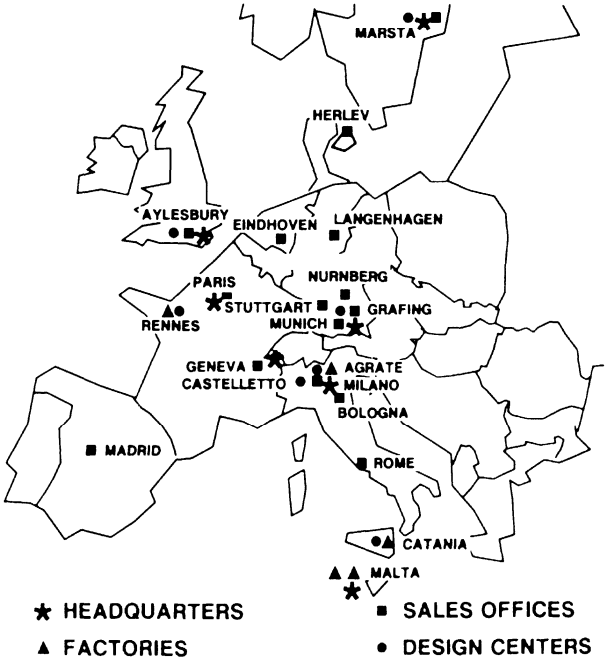
IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with bilings over 300 million dollars and employing over 9500 people.

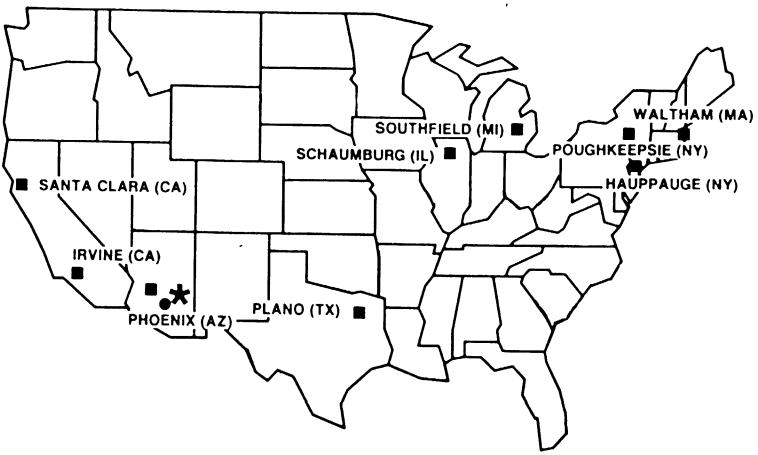
The SGS Group of Companies has now reached a total of 11 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Sweden, Switzerland, United Kingdom and the USA.

To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

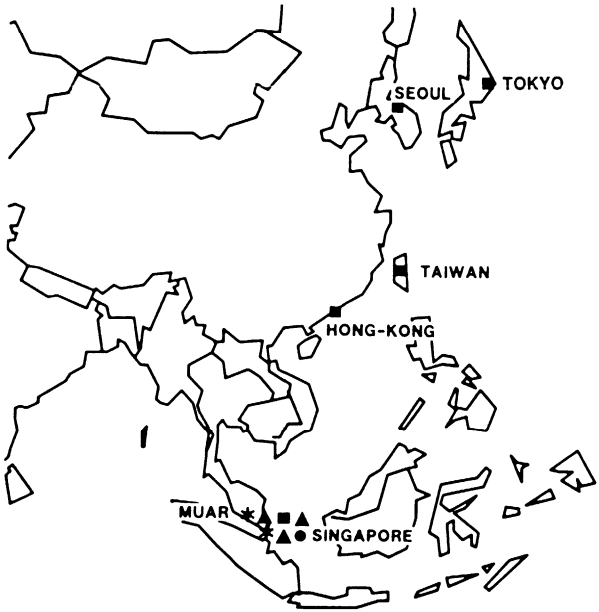
SGS IN EUROPE



SGS IN NORTH AMERICA



SGS IN ASIA/PACIFIC



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PRODUCT SELECTOR GUIDE

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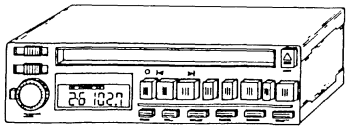

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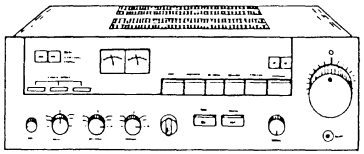

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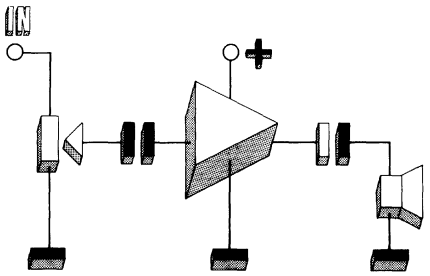

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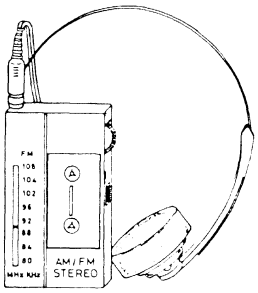

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PRODUCT SELECTOR GUIDE

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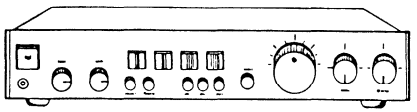

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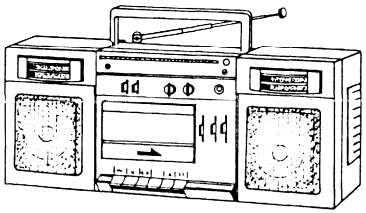

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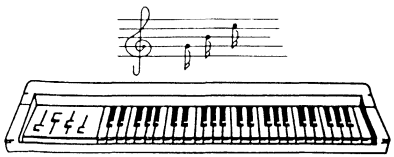

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PRODUCT SELECTOR GUIDE

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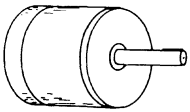

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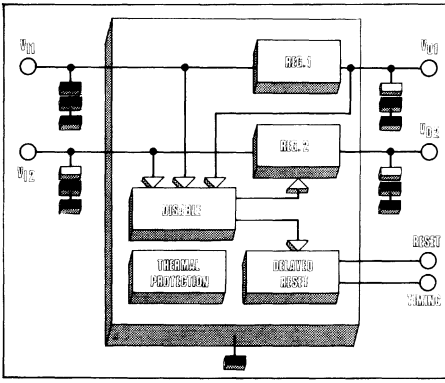

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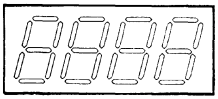

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ICs DATASHEETS

L272
L272M

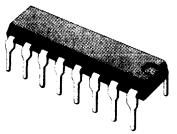
PRELIMINARY DATA

DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8)

Minidip Plastic

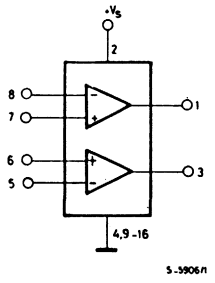
ORDERING NUMBERS:

L272 L272M

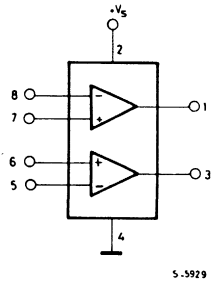
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (**L272**), T_{amb} = 50°C (**L272M**)	1	W
	T_{case} = 75°C (**L272**)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



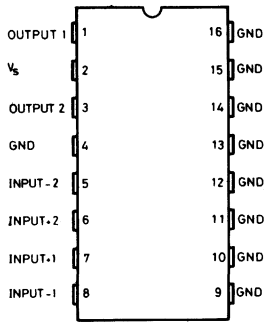
L272



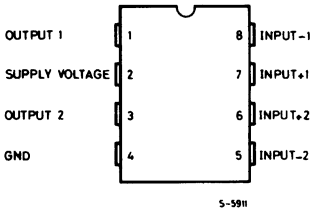
L272M

L272
L272M

CONNECTION DIAGRAM
(Top view)

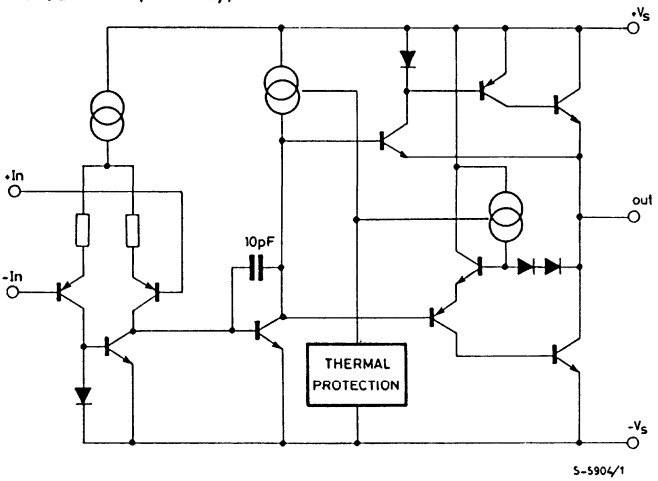


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

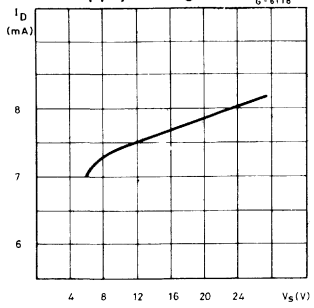


Fig. 2 - Quiescent drain current vs. temperature

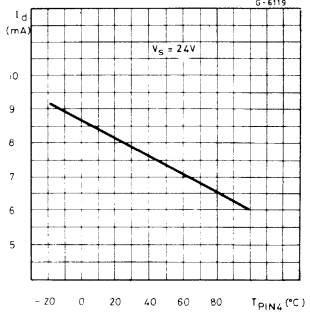


Fig. 3 - Open loop voltage gain

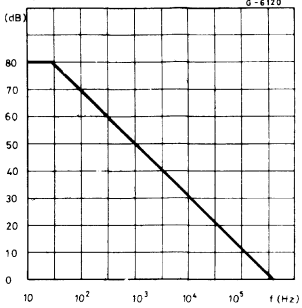


Fig. 4 - Output voltage swing vs. load current

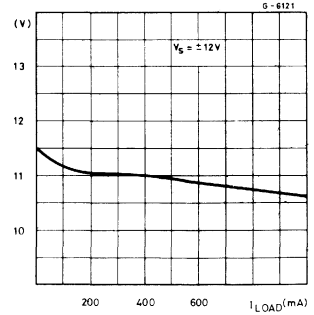


Fig. 5 - Output voltage swing vs. load current

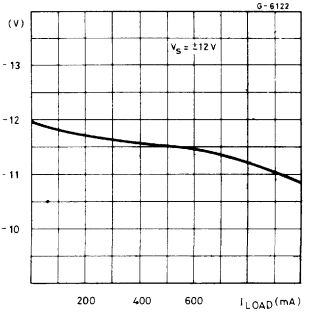


Fig. 6 - Supply voltage rejection vs. frequency

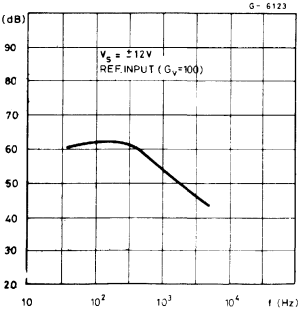


Fig. 7 - Channel separation vs. frequency

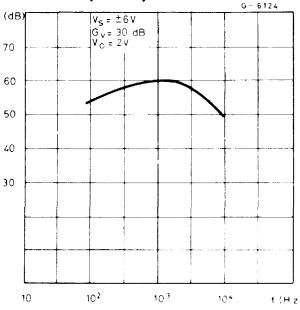
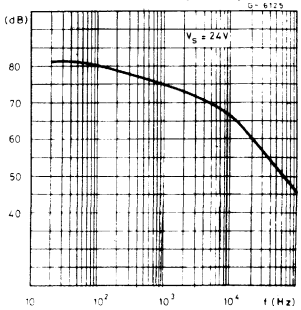


Fig. 8 - Common mode rejection vs. frequency



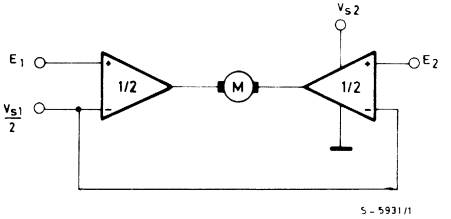
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

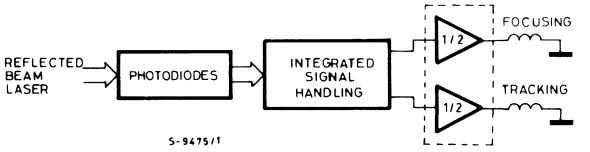


Fig. 11 - Capstan motor control in video recorders

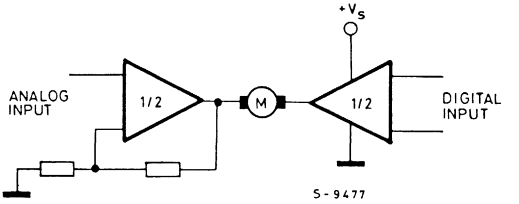
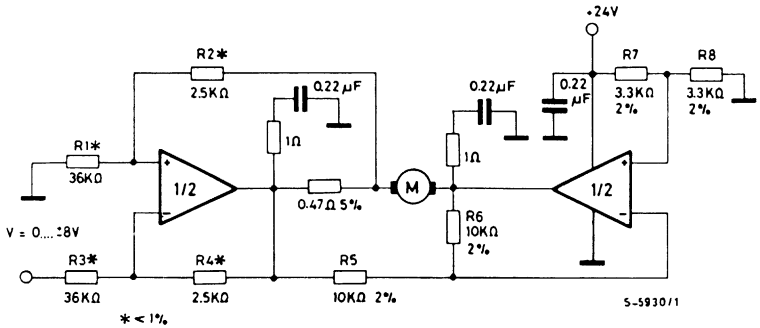


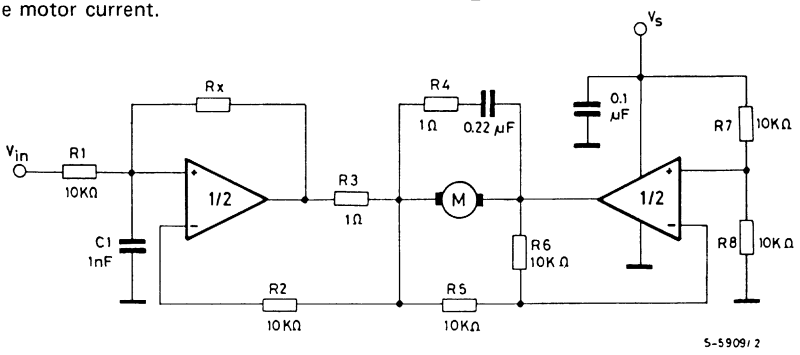
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_i - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R \circ R1}{R_X}$ and I_M is the motor current.



L293
L293E

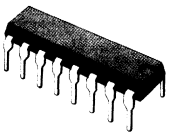
PUSH-PULL FOUR CHANNEL DRIVERS

- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (NON REPETITIVE)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION

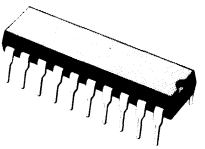
The L293 and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally, the L293E has external connection of sensing resistors, for switchmode control.

The L293 and L293E are packaged in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit board.



DIP-16 Plastic
(0.4)



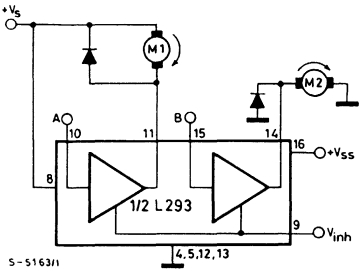
Powerdip
16 + 2 + 2

ORDERING NUMBERS: L293B (16 leads)
L293E (20 leads)

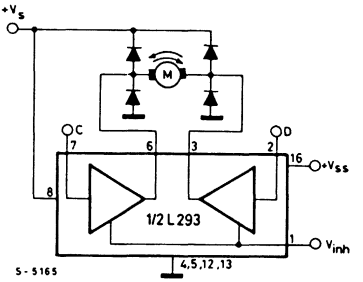
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
V_{ss}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{inh}	Inhibit voltage	7	V
I_{out}	Peak output current (non-repetitive t = 5ms)	2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

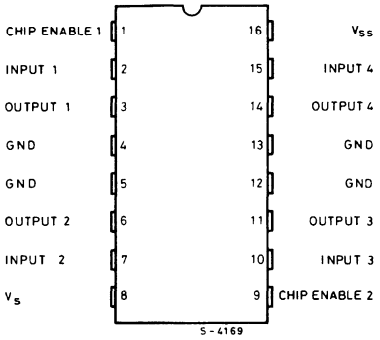
DC motor control

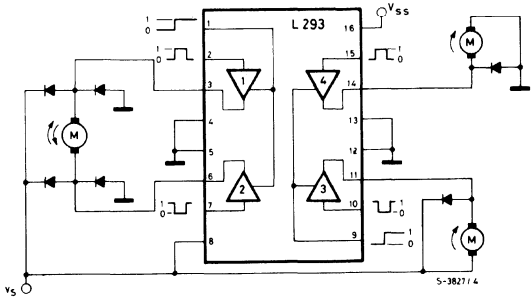


Bidirectional DC motor control

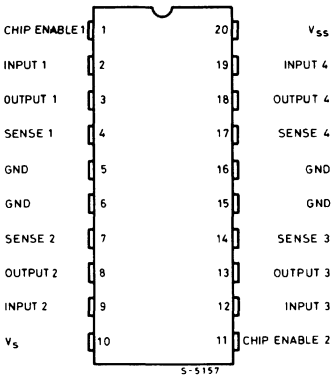


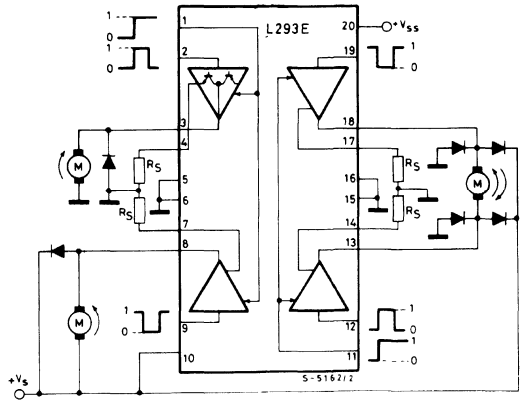
CONNECTION AND BLOCK DIAGRAM (L293)
(top view)



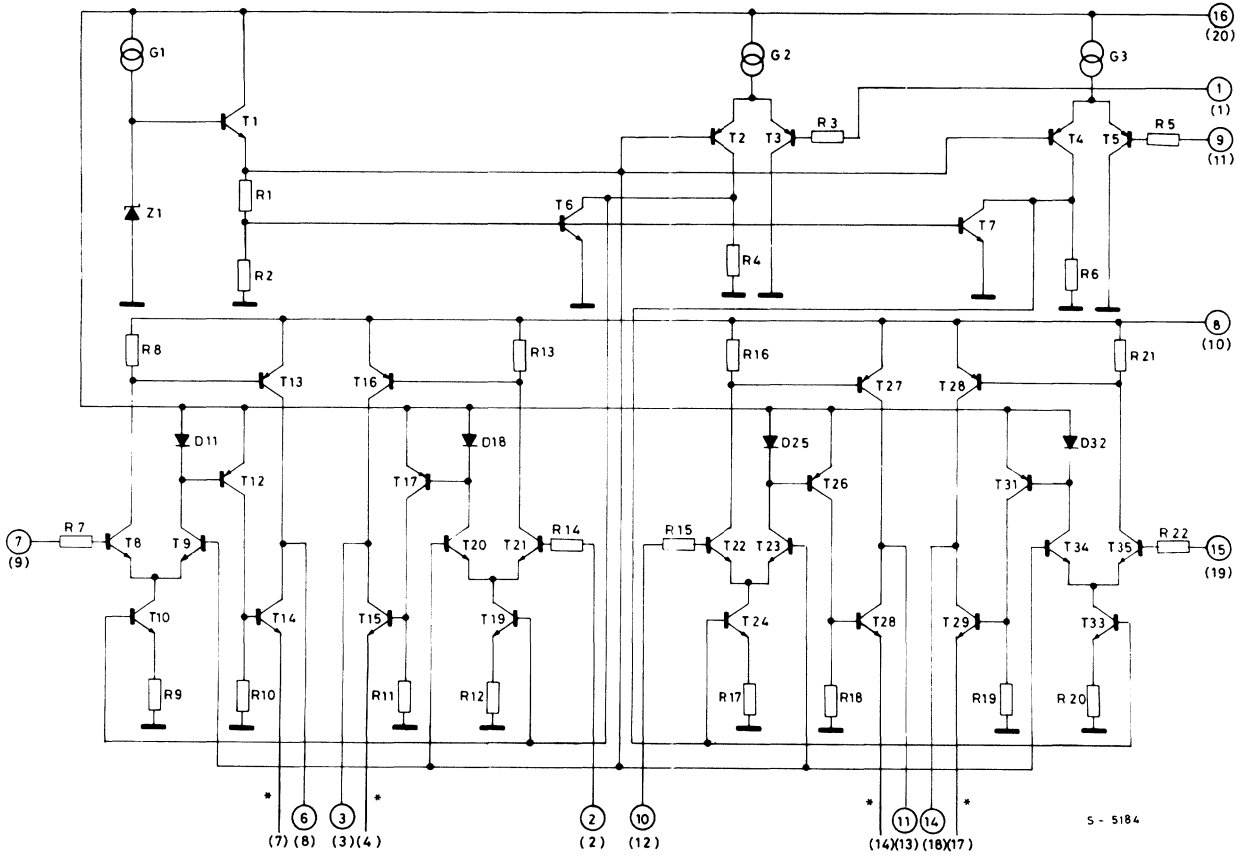


CONNECTION AND BLOCK DIAGRAM (L293E)
(top view)





SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).

○ Pins of L293 ( ) Pins of L293E

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_S= 24V, V_{SS}= 5V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		V_{ss}		36	V
V_{ss}	Logic supply voltage		4.5		36	V
I_s	Total quiescent supply current	V_i = L I_o = 0 V_{inh} = H		2	6	mA
		V_i = H I_o = 0 V_{inh} = H		16	24	
		V_{inh} = L			4	
I_{ss}	Total quiescent logic supply current	V_i = L I_o = 0 V_{inh} = H		44	60	mA
		V_i = H I_o = 0 V_{inh} = H		16	22	
		V_{inh} = L		16	24	
V_{iL}	Input low voltage		-0.3		1.5	V
V_{iH}	Input high voltage	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{iL}	Low voltage input current	V_{IL} = 1.5V			-10	μA
I_{iH}	High voltage input current	$2.3V \leq V_{iH} \leq V_{ss} - 0.6V$		30	100	μA
V_{inhL}	Inhibit low voltage		-0.3		1.5	V
V_{inhH}	Inhibit high voltage	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{inhL}	Low voltage inhibit current	V_{inhL} = 1.5V		-30	-100	μA
I_{inhH}	High voltage inhibit current	$2.3V \leq V_{inhH} \leq V_{ss} - 0.6V$			± 10	μA
V_{CEsatH}	Source output saturation voltage	I_o = -1A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage	I_o = 1A		1.2	1.8	V
V_{SENS}	Sensing Voltage (pins 4, 7, 14, 17) (**)				2	V
t_r	Rise time	0.1 to 0.9 V_o (*)		250		ns
t_f	Fall time	0.9 to 0.1 V_o (*)		250		ns
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o (*)		750		ns
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o (*)		200		ns

(*) See fig. 1.

(**) Referred to L293E.

TRUTH TABLE

V_i (each channel)	V_o	$V_{inh.}$ (°°)
H	H	H
L	L	H
H	X (°)	L
L	X (°)	L

(°) High output impedance.
(°°) Relative to the considerate channel.

Fig. 1 - Switching times

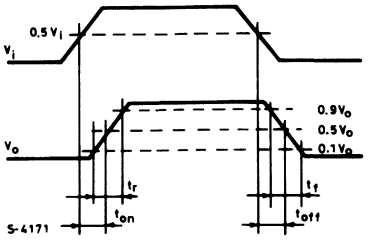


Fig. 2 - Saturation voltage vs. output current

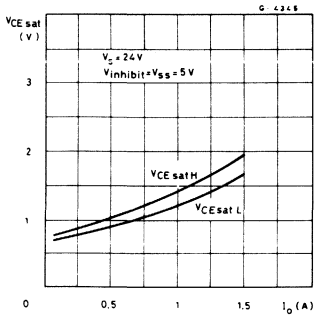


Fig. 3 - Source saturation voltage vs. ambient temperature

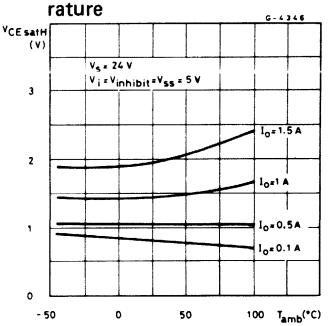


Fig. 4 - Sink saturation voltage vs. ambient temperature

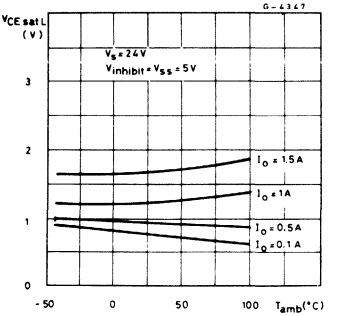


Fig. 5 - Quiescent logic supply current vs. logic supply voltage

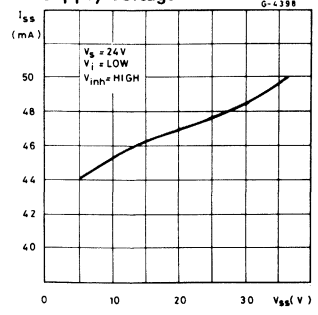


Fig. 6 - Output voltage vs. input voltage

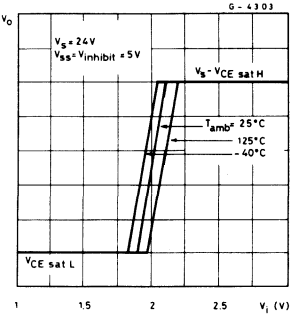
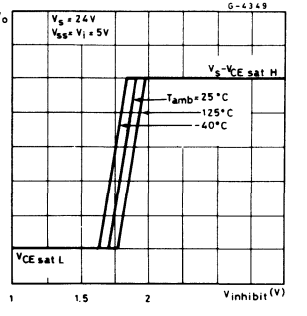
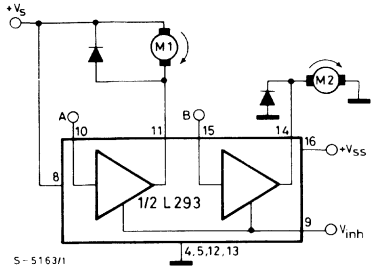


Fig. 7 - Output voltage vs. inhibit voltage



APPLICATION INFORMATION

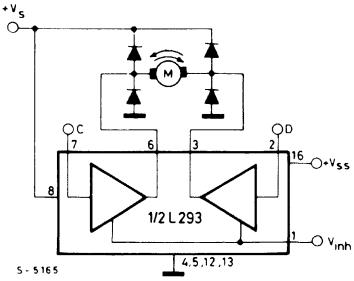
Fig. 8 - DC motor controls (with connection to ground and to the supply voltage)



V_{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

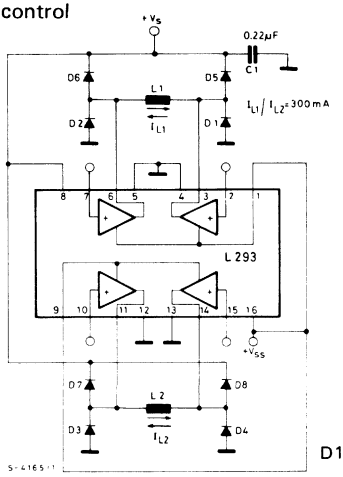
Fig. 9 - Bidirectional DC motor control



INPUTS		FUNCTION
V_{inh} = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{inh} = L	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

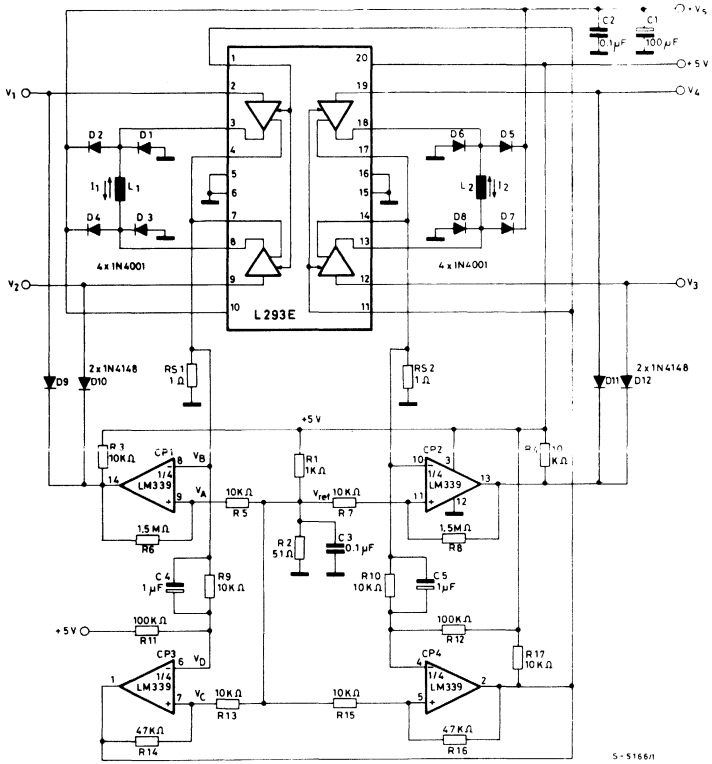
Fig. 10 - Bipolar stepping motor control



D1 - D8 = { $V_F \leq 1.2V$ @ I = 300 mA; trr ≤ 500 ns

APPLICATION INFORMATION (continued)

Fig. 11 - Stepping motor driver with phase current control and short circuit protection



D1 to D8 : $\begin{cases} V_F \leqslant 1.2V \text{ @ } I = 300\ mA \\ trr \leqslant 200\ ns \end{cases}$

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L293 and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 12 or to an external heatsink (figure 13).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area which is used as heatsink

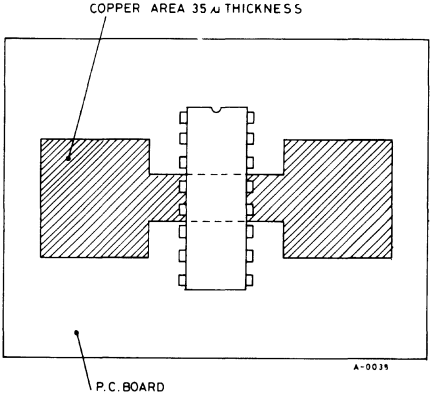
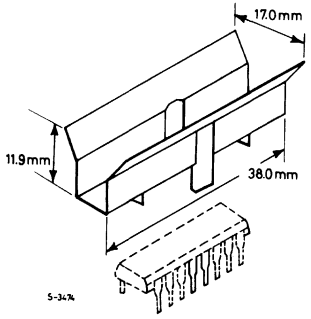


Fig. 13 - External heatsink mounting example (R_{th} = 30 °C/W)



L293D

PRELIMINARY DATA

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

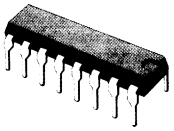
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON RE-PETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VILTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

The L293D is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

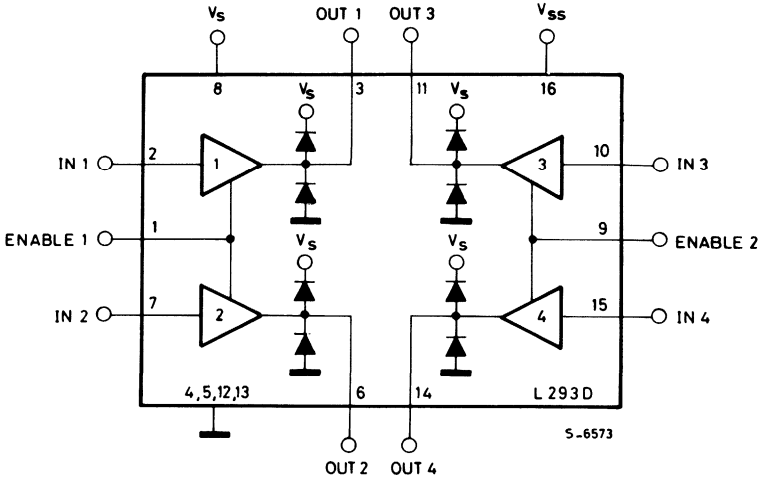
The L293D is assembled in a 16 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
12 + 2 + 2

ORDERING NUMBER: L293D

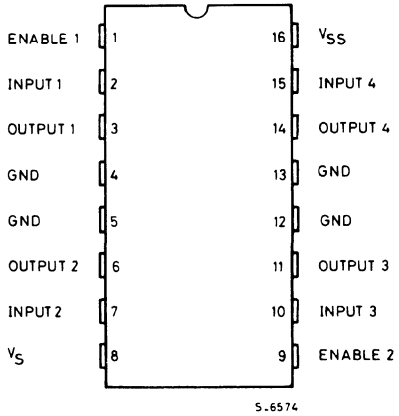
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	36	V
V_{SS}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{en}	Enable voltage	7	V
I_o	Peak output current (100μs non repetitive)	1.2	A
P_{tot}	Total power dissipation at $T_{ground-pins} = 80°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_s = 24V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 8)		V_{ss}		36	V
V_{ss}	Logic supply voltage (pin 16)		4.5		36	V
I_s	Total quiescent supply current (pin 8)	V_i = L I_o = 0 V_{en} = H		2	6	mA
		V_i = H I_o = 0 V_{en} = H		16	24	
		V_{en} = L			4	
I_{ss}	Total quiescent logic supply current (pin 16)	V_i = L I_o = 0 V_{en} = H		44	60	mA
		V_i = H I_o = 0 V_{en} = H		16	22	
		V_{en} = L		16	24	
V_{IL}	Input low voltage (pin 2, 7, 10, 15)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 7, 10, 15)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{IL}	Low voltage input current (pin 2, 7, 10, 15)	V_{IL} = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 7, 10, 15)	$2.3V \leq V_{IH} \leq V_{ss} - 0.6V$		30	100	μA
V_{enL}	Enable low voltage (pin 1, 9)		-0.3		1.5	V
V_{enH}	Enable high voltage (pin 1, 9)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{enL}	Low voltage enable current current (pin 1, 9)	V_{enL} = 1.5V		-30	-100	μA
i_{enH}	High voltage enable current (pin 1, 9)	$2.3V \leq V_{enH} \leq V_{ss} - 0.6V$			± 10	μA
V_{CEsatH}	Source output saturation voltage (pins 3, 6, 11, 14)	I_o = - 0.6A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage (pins 3, 6, 11, 14)	I_o = + 0.6A		1.2	1.8	V
V_F	Clamp diode forward voltage	I_o = 600 mA		1.3		V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

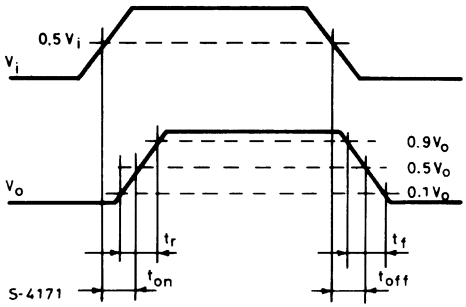
(*) See fig. 1

TRUTH TABLE (One channel)

INPUT	ENABLE (*)	OUTPUT
H	H	H
L	H	L
H	L	Z
L	L	Z

Z = High output impedance
(*) Relative to the considered channel

Fig. 1 - Switching Times



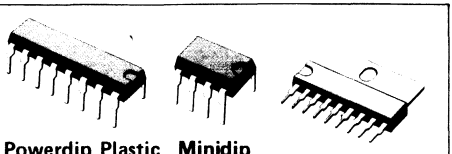
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip Plastic (8 + 8) | **Minidip Plastic** | **SIP-9**

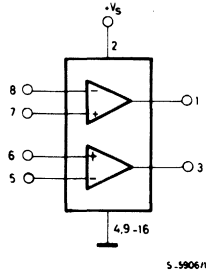
ORDERING NUMBERS:

L2720 L2722 L2724

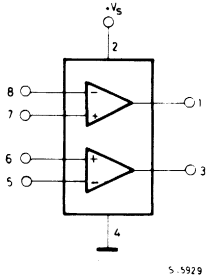
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (**L2720**), T_{amb} = 50°C (**L2722**)	1	W
	T_{case} = 75°C (**L2720**)	5	W
	T_{case} = 50°C (**L2724**)	10	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

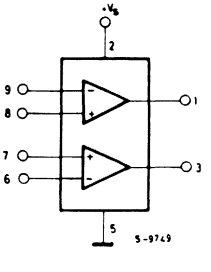
BLOCK DIAGRAMS



L2720



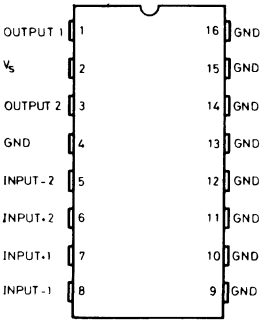
L2722



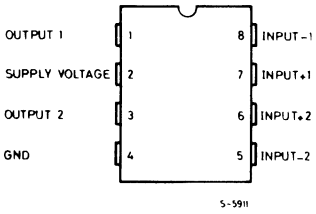
L2724

L2720 L2722 L2724

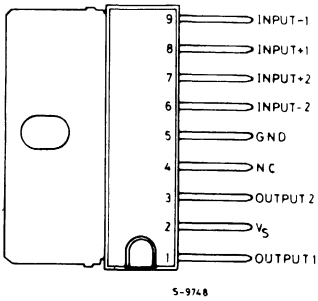
CONNECTION DIAGRAMS
(Top view)



L2720

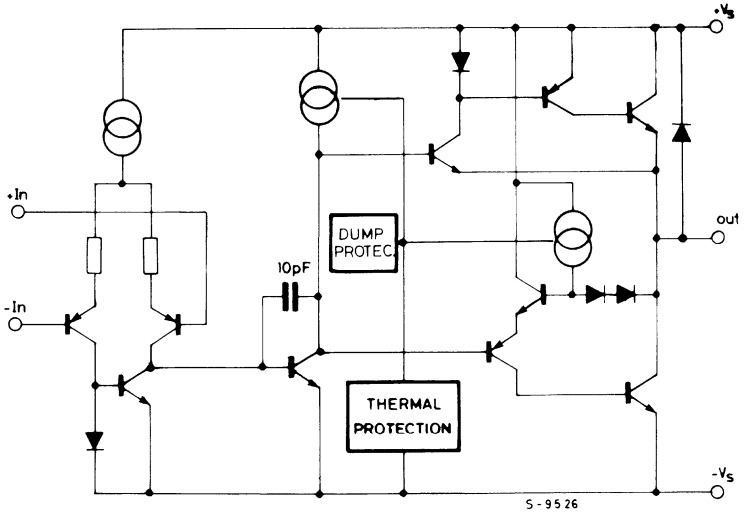


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

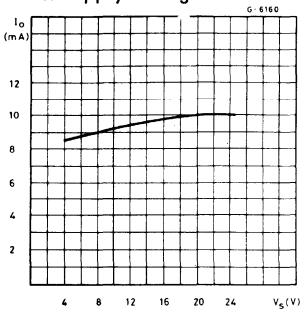


Fig. 2 - Open loop gain vs. frequency

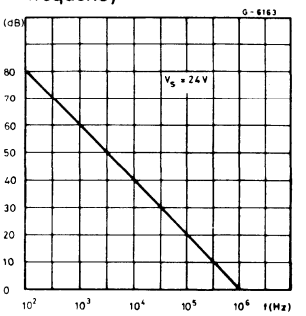


Fig. 3 - Common mode rejection vs. frequency

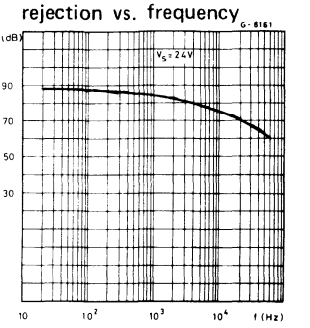


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

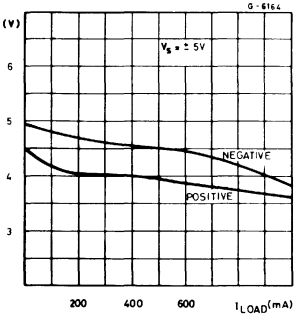


Fig. 5 - Output swing vs. load current (V_S = ± 12V)

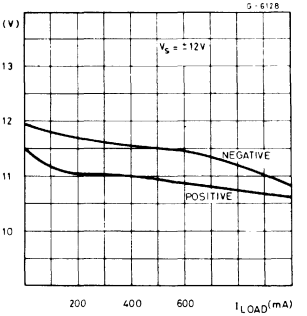


Fig. 6 - Supply voltage rejection vs. frequency

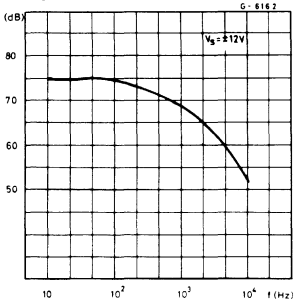
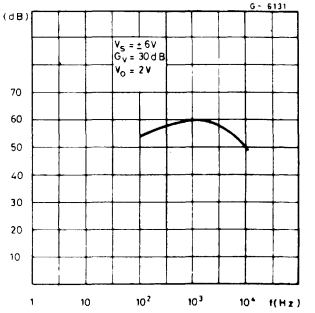


Fig. 7 - Channel separation vs. frequency

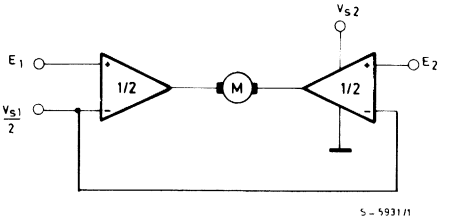


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

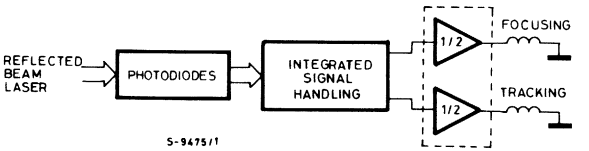


Fig. 10 - Capstan motor control in video recorders

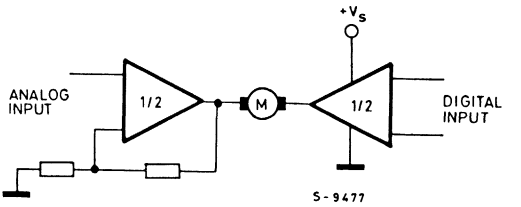
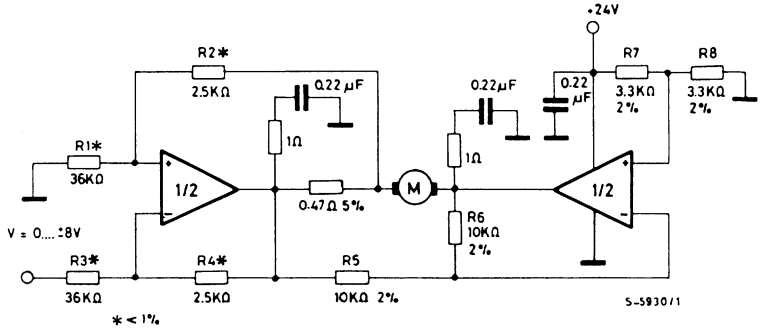


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \cdot R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 (V_I - \frac{V_s}{2}) + |R_o|. I_M$ where $|R_o| = \frac{2R \cdot R1}{R_X}$ and I_M is the motor current.

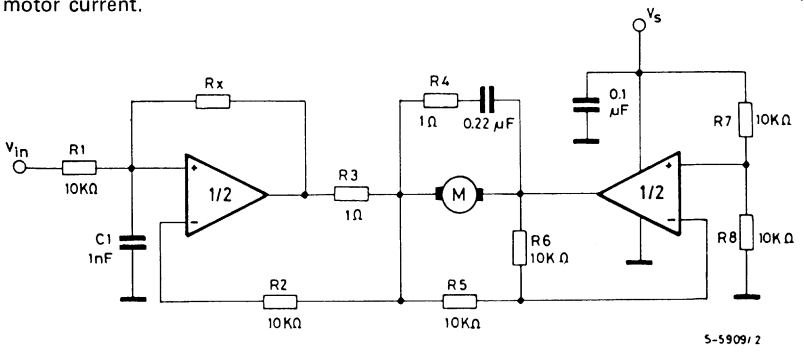
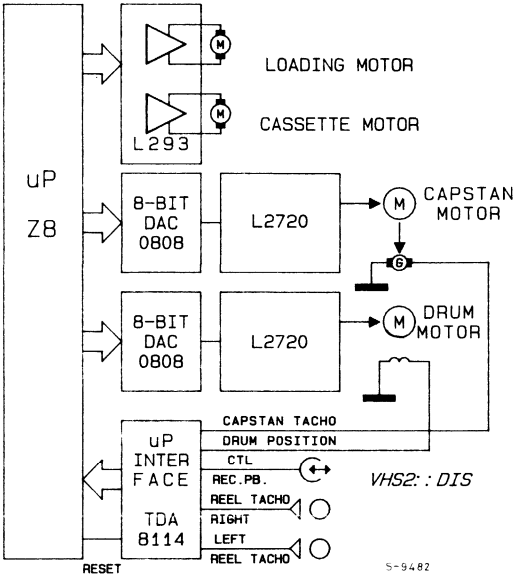


Fig. 13 - VHS-VCR Motor control circuit



PRINTER SOLENOID DRIVER

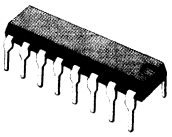
The L3654S is a printer solenoid driver containing ten open-collector driver outputs and a ten-bit serial-in, parallel-out register.

Data is clocked into the shift register serially and transferred to the open-collector outputs by an enable input. Serial input data is loaded by the rising edge of the clock. A serial output from the tenth bit is provided which changes at the falling edge of the clock. This output is not controlled by the enable input and remains active at all time.

The L3654S is pin to pin compatible with the standard L3654, but can work with V_s down to 4.75V.

Each output is rated at 250mA (sink) and is clamped to ground internally at 50V to dissipate stored energy in inductive loads.

The L3654S is supplied in a 16 lead dual in-line plastic package, and its main fields of application comprise thermal printers, cash registers and printing pocket calculators.



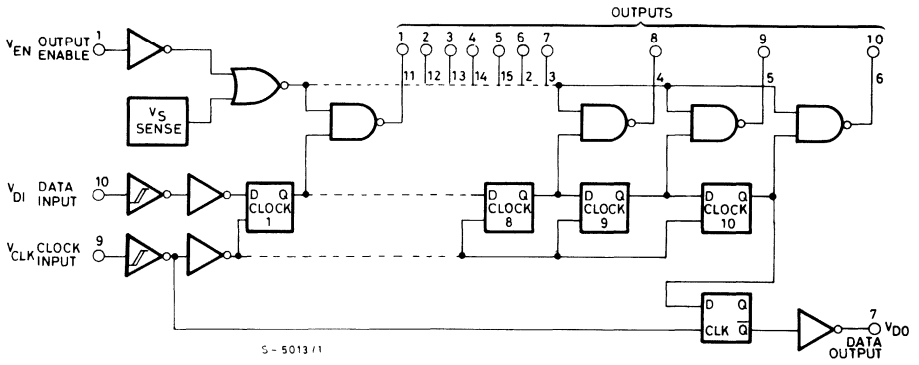
DIP-16 Plastic
(0.25)

ORDERING NUMBER: L3654S

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9.5	V
V_i	Input voltage	9.5	V
V_E	External supply voltage	45	V
I_o	Output current (single output)	0.4	A
I_g	Ground current	4.0	A
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(top view)

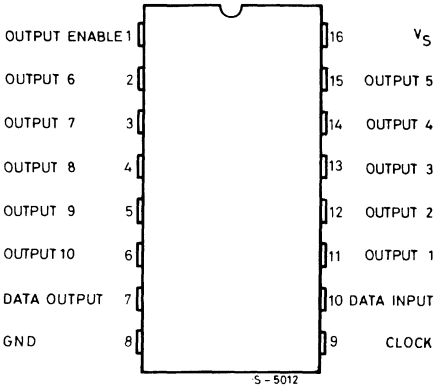
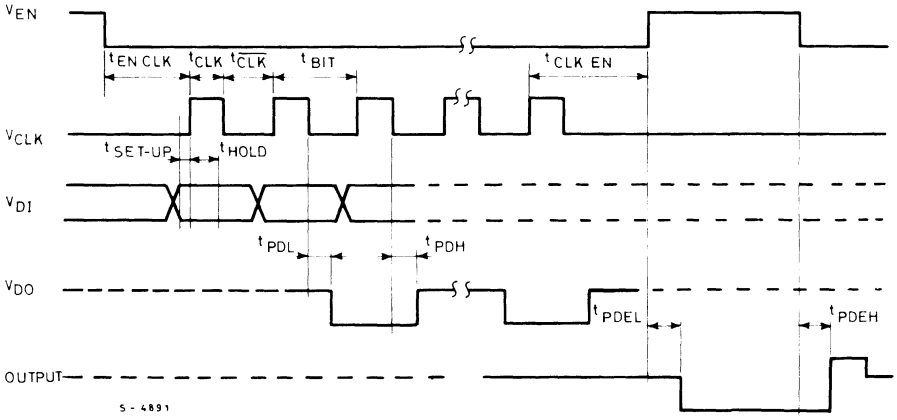


Fig. 1 - Timing diagram



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 5V, V_E = 30V, T_{amb} = 0° to 70°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4.75		9.5	V
I_S	Supply current	T_{amb} = 25°C	V_{EN} = 0V; V_{DO} = 0V		27	40	mA
		V_s = 9.5V	V_{EN} = 2.6V I_o = 250 mA (each bit)		55	70	mA
V_E	External operating supply voltage					40	V
I_{leak}	Output leakage current (each output)	V_E = 40V	V_{EN} = 0V			1	mA
V_z	Internal clamp voltage	I_z = 0.3A *	V_{EN} = 0V	45	50	65	V
$V_{CE\ sat}$	Output saturation voltage	I_o = 250 mA	V_{EN} = 2.6V			1.6	V
V_{DI} V_{CLK} V_{EN}	Input logic levels (pins 1, 9, 10)	Low State (L)				0.8	V
		High state (H)		2.6			
I_{DI}	Data input current	V_{DI} = 2.6V	T_{amb} = 70°C	0.3	0.57		mA
			T_{amb} = 0°C		0.57	0.75	
		V_{DI} = 1V	T_{amb} = 70°C		220		µA
I_{CLK}	Clock input current	V_{CLK} = 2.6V	T_{amb} = 70°C	0.2	0.33		mA
			T_{amb} = 0°C		0.33	0.5	
		V_{CLK} = 1V	T_{amb} = 70°C		125		µA
I_{EN}	Enable input current	V_{EN} = 2.6V	T_{amb} = 70°C	0.2	0.33		mA
			T_{amb} = 0°C		0.33	0.5	
		V_{EN} = 1V	T_{amb} = 70°C		125		µA
R_{IN}	Input pull-down resistance Clock input	T_{amb} = 25°C	$V_{CLK} < V_s$		8		KΩ
	Enable input	T_{amb} = 25°C	$V_{EN} < V_s$		8		
	Data input	T_{amb} = 25°C	$V_{DI} < V_s$		4.5		
V_{DO}	Output logic levels (pin 7)	Low state (L) V_{DI} = 0V	I_{DO}(pin 7) = 0		0.01	0.5	V
		High state (H) V_{DI} = 2.6V I_{DO} (pin 7) = -0.75 mA		2.6	3.4		V
R_{DO}	Output pull-down resistance (pin 7)	V_{DI} = 0V	V_{DO} = 1V		14		KΩ

* Pulsed: pulse duration = 300µs, duty cycle = 2%

ELECTRICAL CHARACTERISTICS (see fig. 1 and the section "definition of terms")

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Clock, data and enable input	t_{CLK}		4			μs
	$\overline{t_{CLK}}$		5.5			μs
	t_{SET-UP}		1			μs
	t_{HOLD}		3			μs
Clock to enable delay	$t_{CLK\ EN}$		2 t_{BIT}			
Enable to clock delay	$t_{EN\ CLK}$		t_{BIT}			
Data output delay	t_{PDH}, t_{PDL}	R_L= 5KΩ, $C_L \leq$ 10 pF		0.8	2.5	μs
Output delay	t_{PDEL}			3		μs
	t_{PDEH}			3.5		μs
Output rise time		R_L= 100 Ω, C_L < 100 pF		1.2		μs
Output fall time		R_L= 100 Ω, C_L < 100 pF		1.2		μs
V_{DO} rise time				0.4		μs
V_{DO} fall time				0.4		μs

DEFINITION OF TERMS

V_{ss} : External power supply voltage. The return for open-collector relay driver outputs.

V_{DI}, V_{CLK}, V_{EN} : The voltages at the data, clock and enable inputs respectively.

V_{DO} : The voltage at data output.

t_{BIT} : Period of the incoming clock.

t_{CLK} : The portion of t_{BIT} when $V_{CLK} \geq 2.6V$.

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leq 0.8V$.

t_{HOLD} : The time following the start of t_{CLK} required to transfer data within the shift register.

t_{SET-UP} : The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

L4901

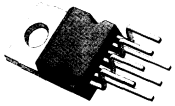
PRELIMINARY DATA

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



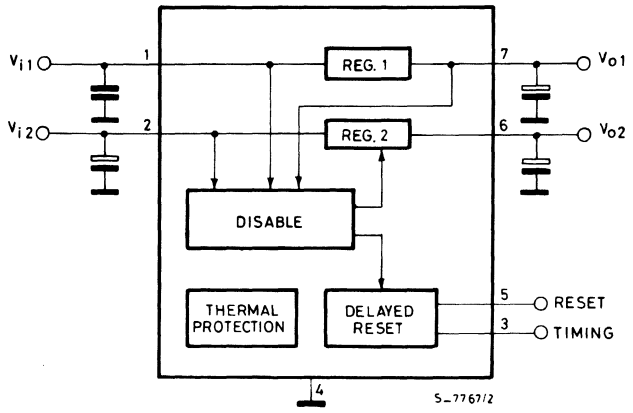
Heptawatt

ORDERING NUMBER: L4901

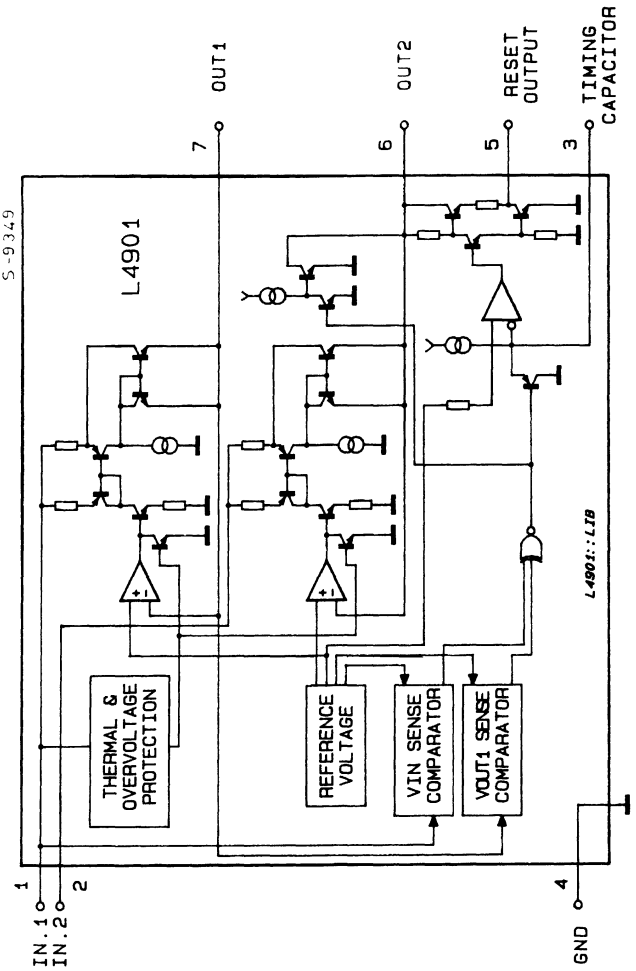
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

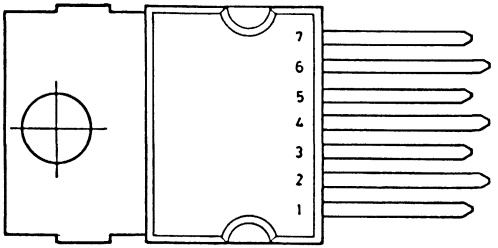
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



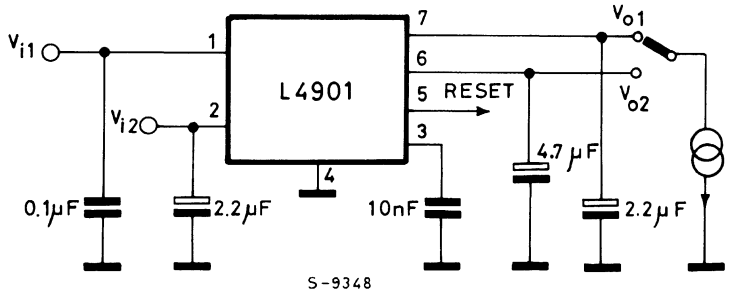
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 300mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4,95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.05	0.8 1 1.25	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.6	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

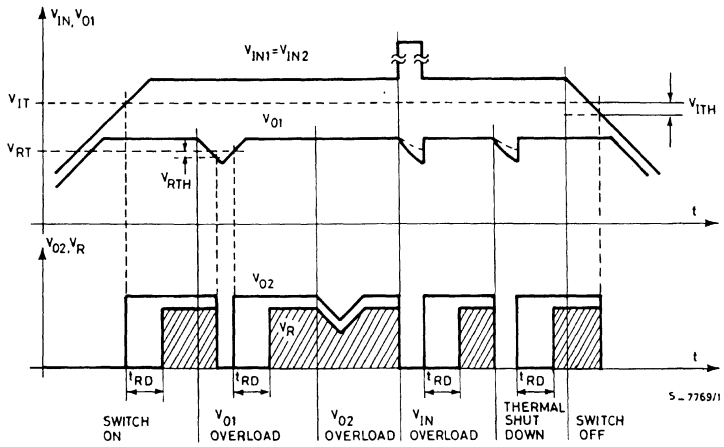
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901 is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901 is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_I occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

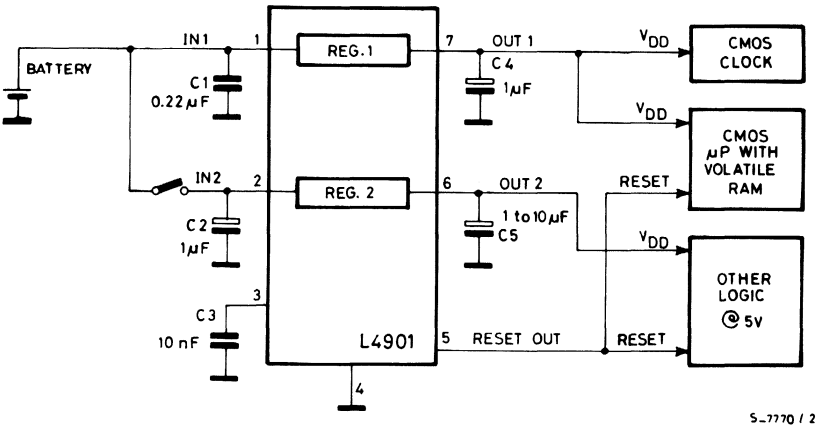
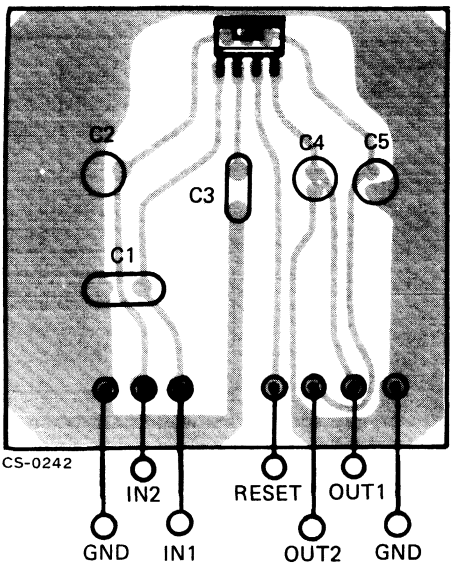


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

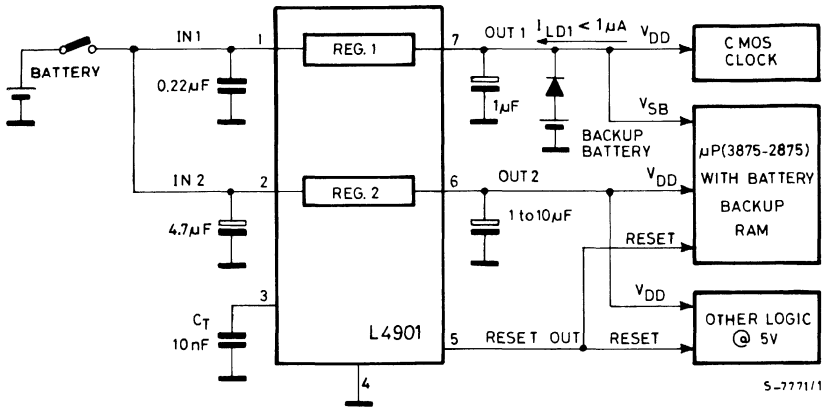
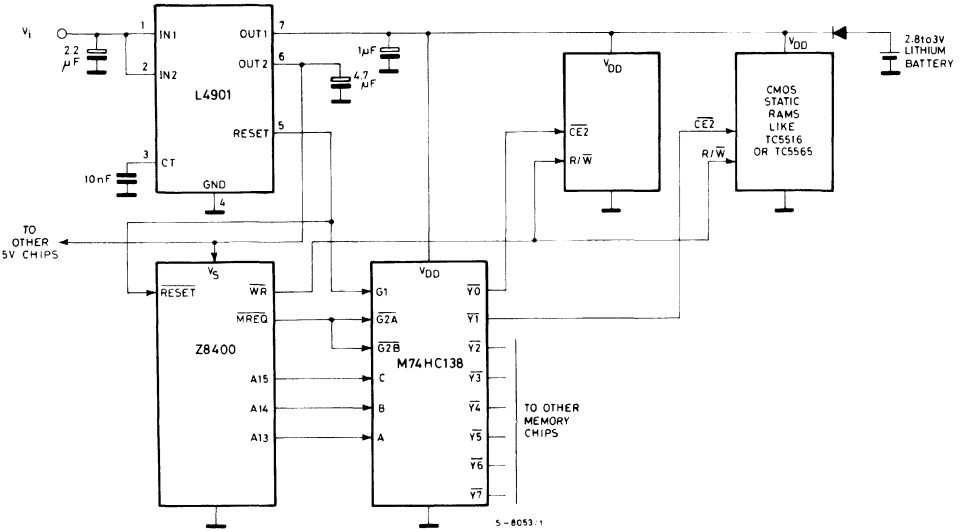


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

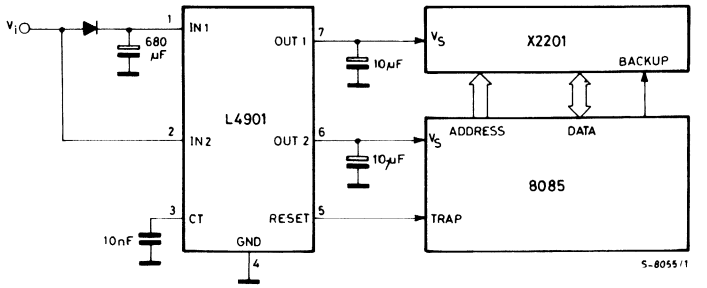


Fig. 7 - Quiescent current (Reg. 1) vs. output current

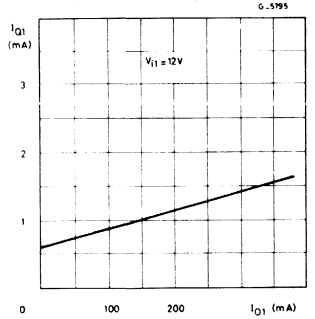


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

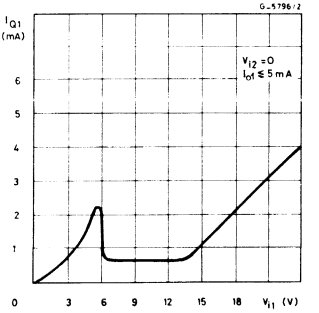


Fig. 9 - Total quiescent current vs. input voltage

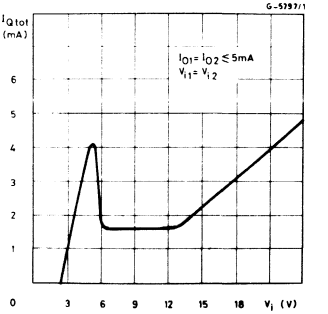


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

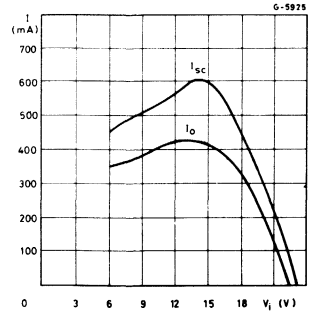


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

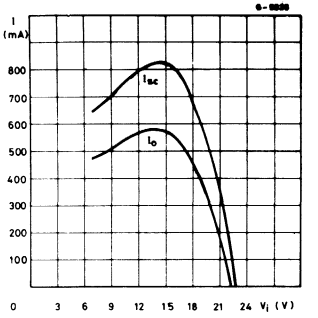
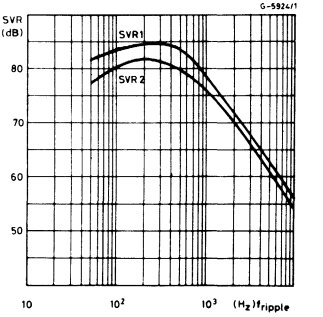


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



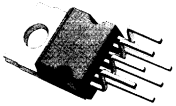
L4902

PRELIMINARY DATA

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



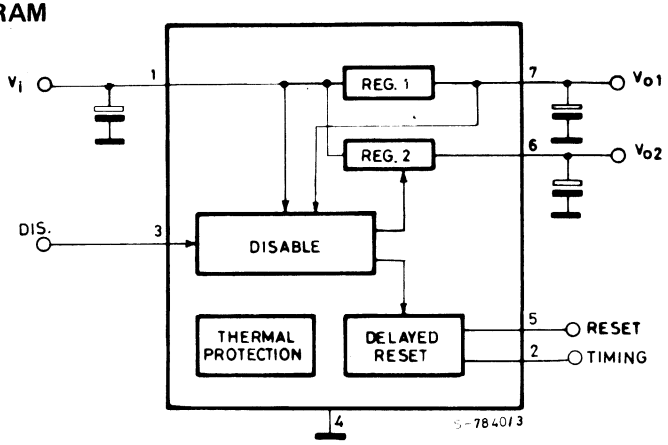
Heptawatt

ORDERING NUMBER: L4902

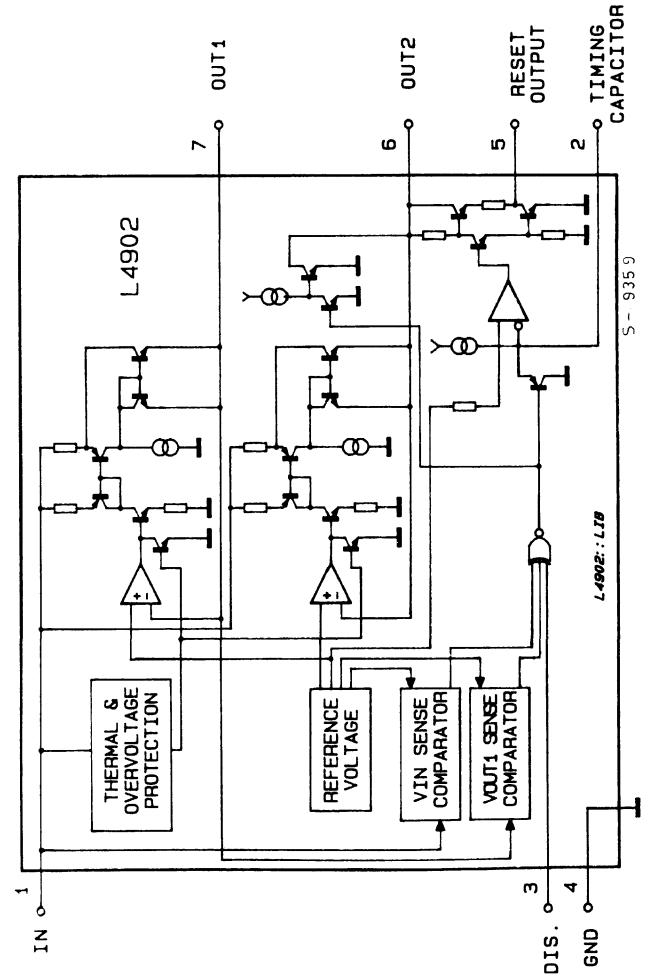
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



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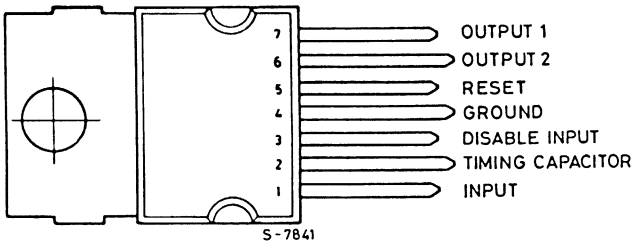
(Top view)



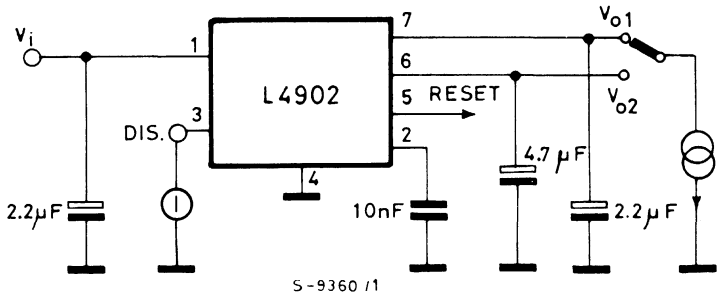
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.05	0.8 1 1.25	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.6	V
V_{iTH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V V_{02} LOW 6.3V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6 4 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	54	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

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In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

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When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

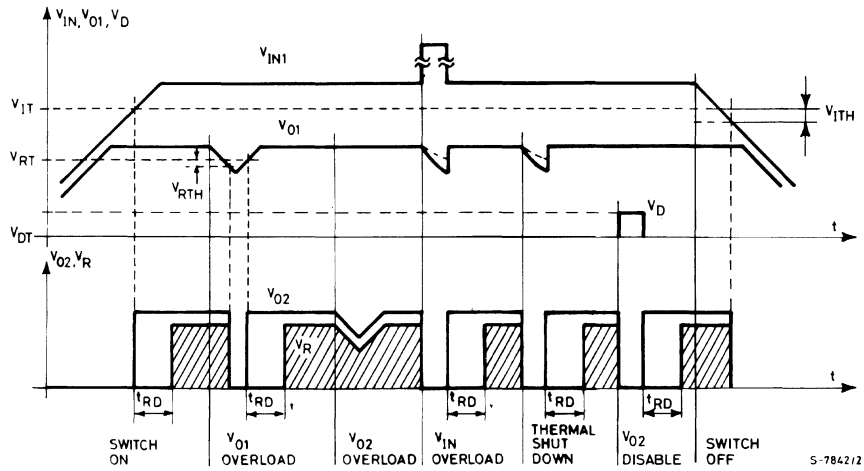
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrates how the L4902's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902 is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

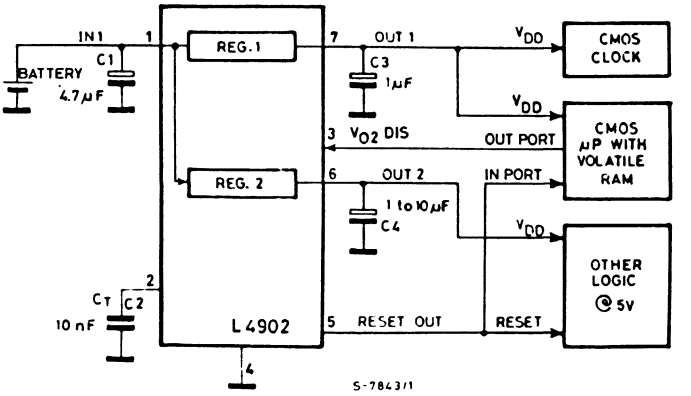
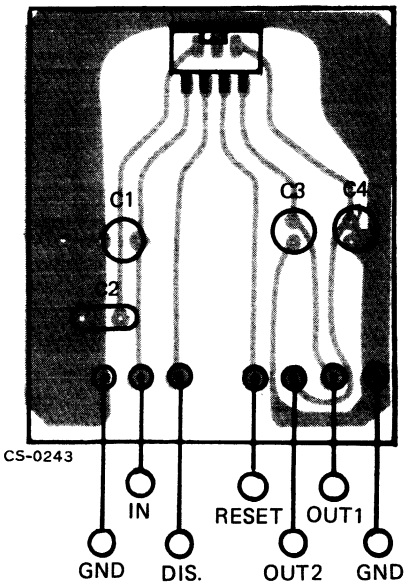


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

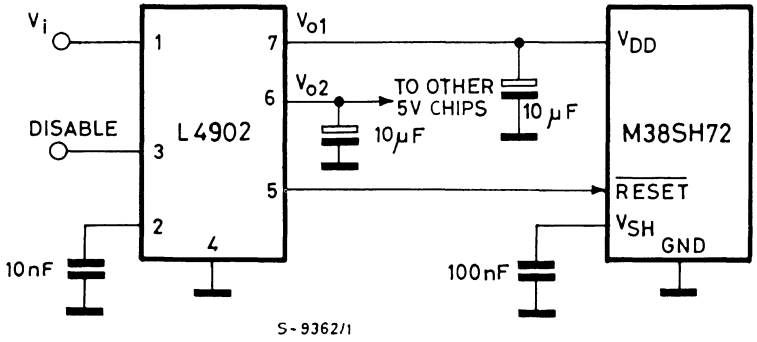
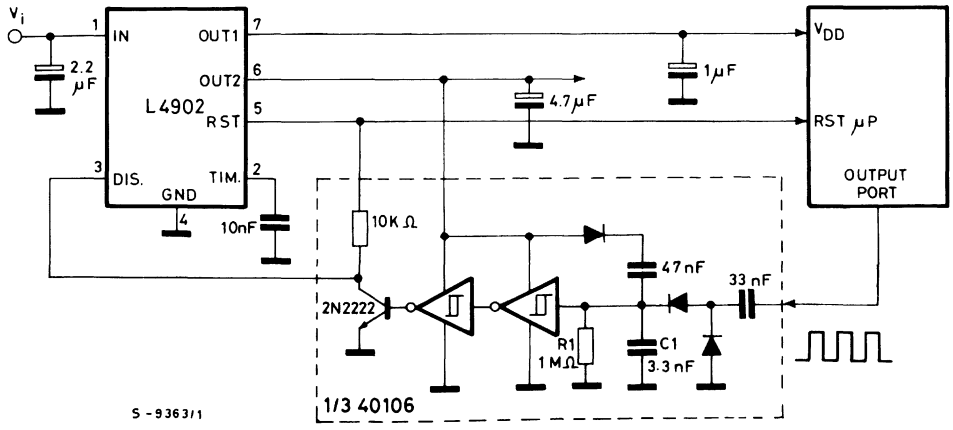


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

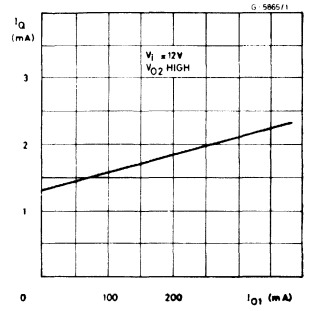


Fig. 7 - Quiescent current vs. input voltage

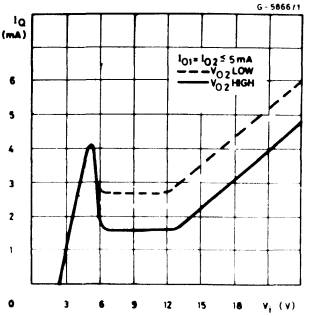


Fig. 8 - Regulator 1 output current and short circuit current vs. input voltage

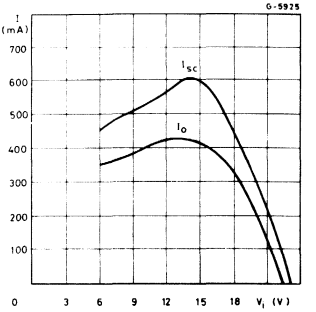


Fig. 9 - Regulator 2 output current and short circuit current vs. input voltage

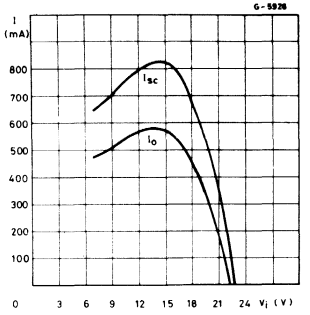
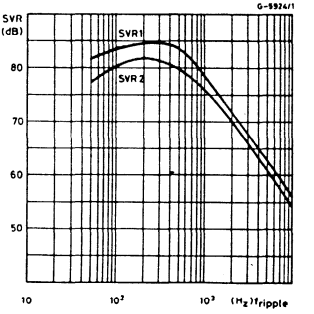


Fig. 10 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4903

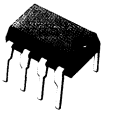
ADVANCE DATA

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ±2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



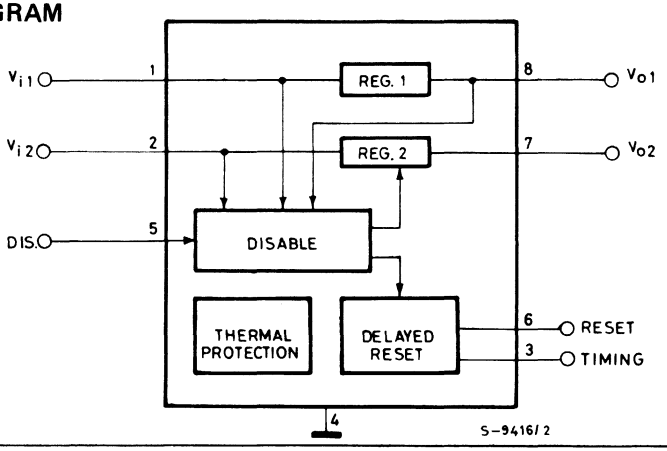
Minidip Plastic

ORDERING NUMBER: L4903

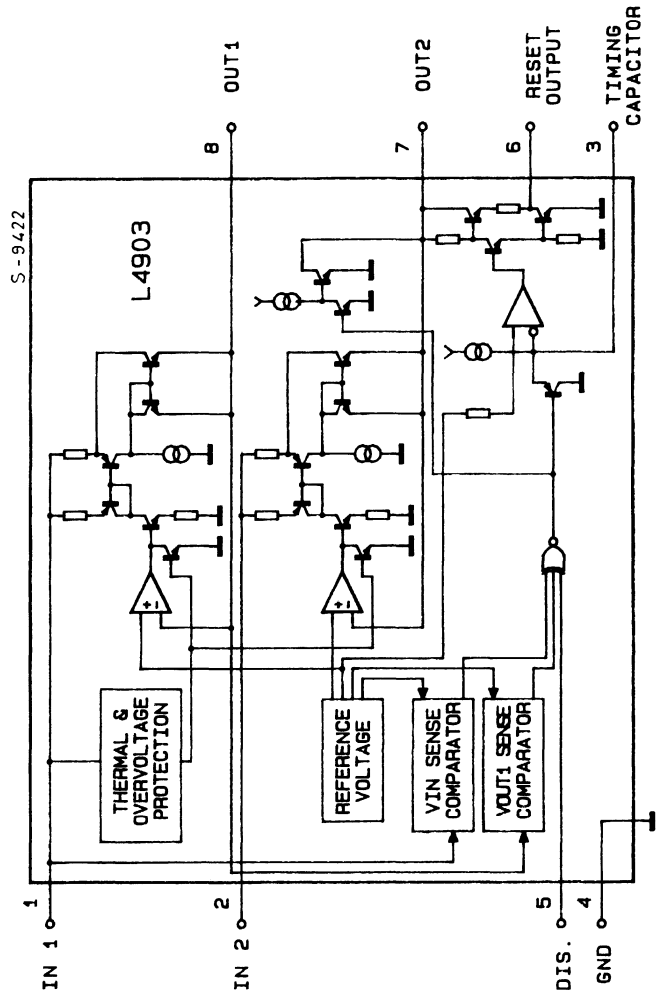
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

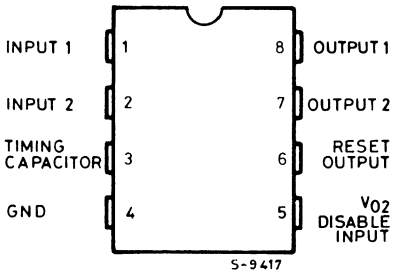
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



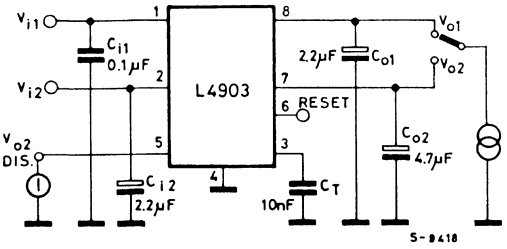
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

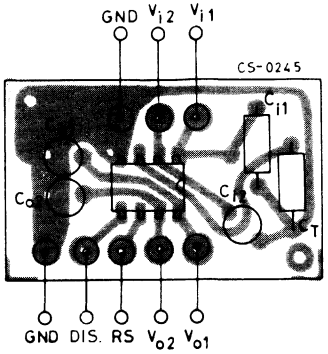
THERMAL DATA

$R_{th\ j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.6	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V V_{02} LOW 6.3V < V_{IN} < 13V V_{02} HIGH I_{01} = I_{02} ≤ 5mA		4.5 2.7 1.6	6 4 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	54	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

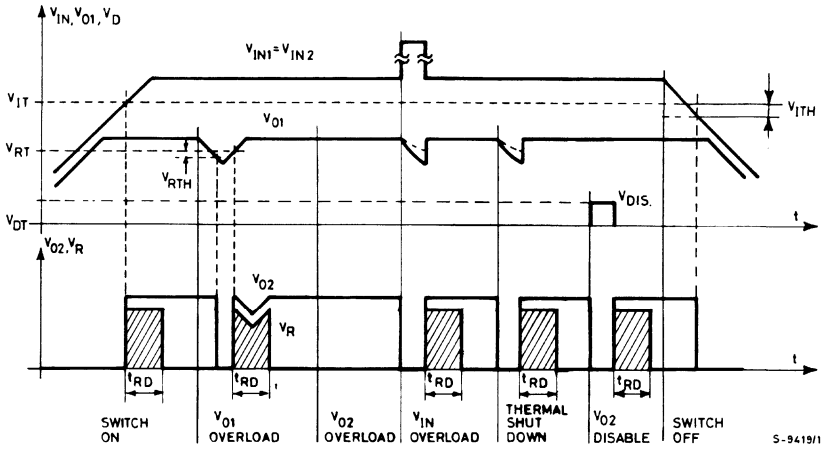
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2

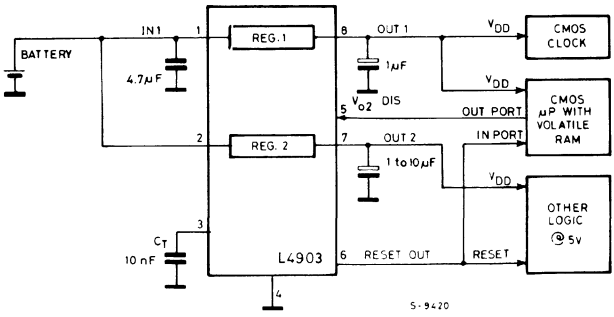


Fig. 3 - Quiescent current (Reg. 1) vs. output current

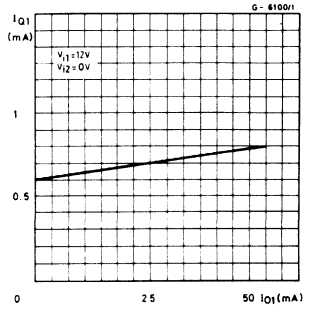


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

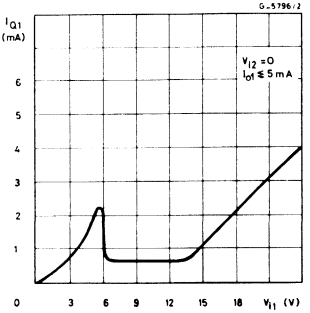


Fig. 5 - Total quiescent current vs. input voltage

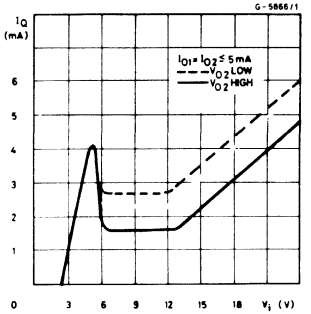
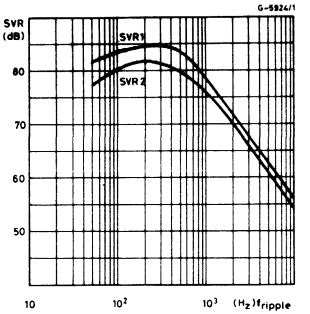


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4904

ADVANCE DATA

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

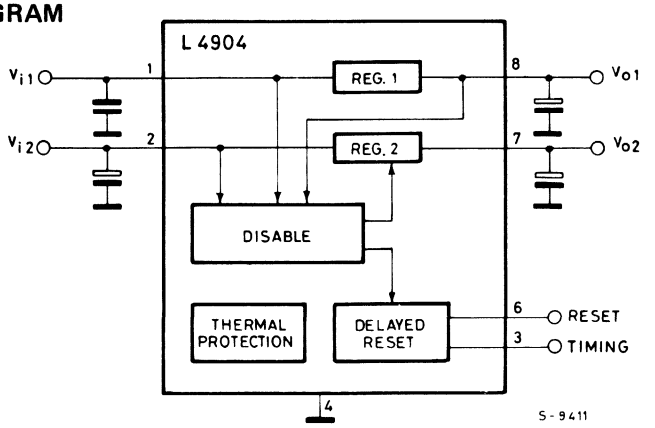
Minidip Plastic

ORDERING NUMBER: L4904

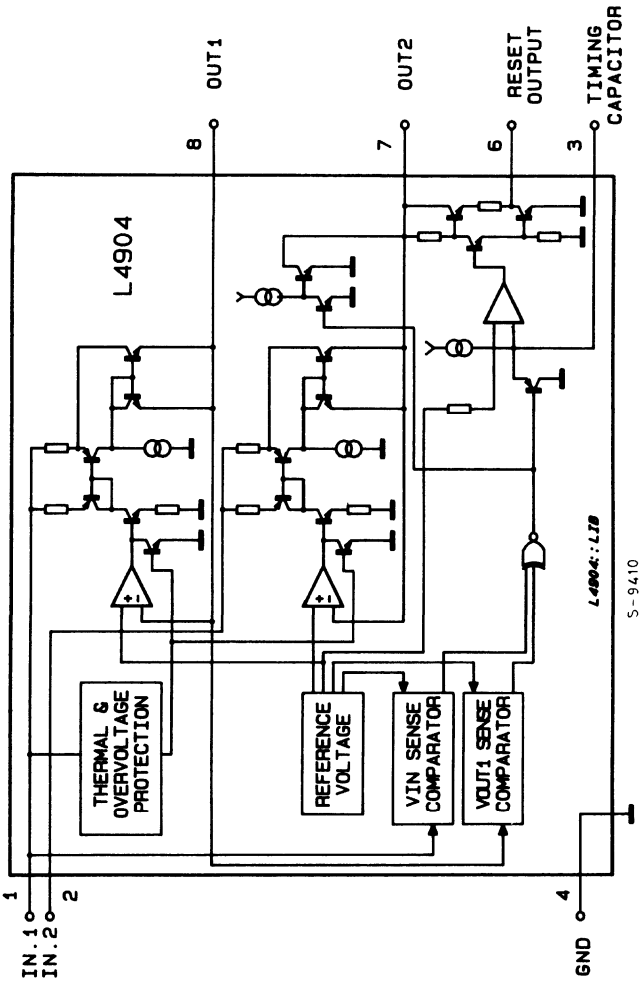
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

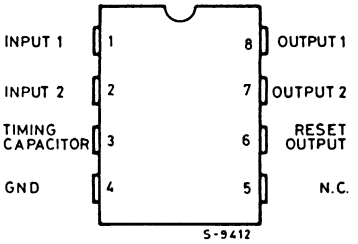
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



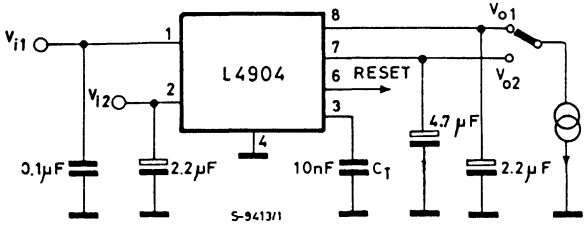
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN 2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

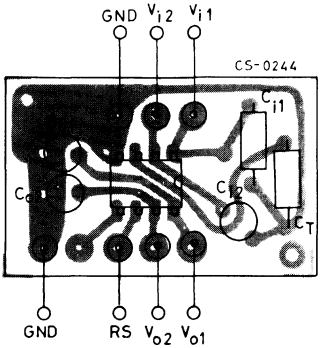
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	μA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.6	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 50mA	54	84		dB
SVR2	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904 makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

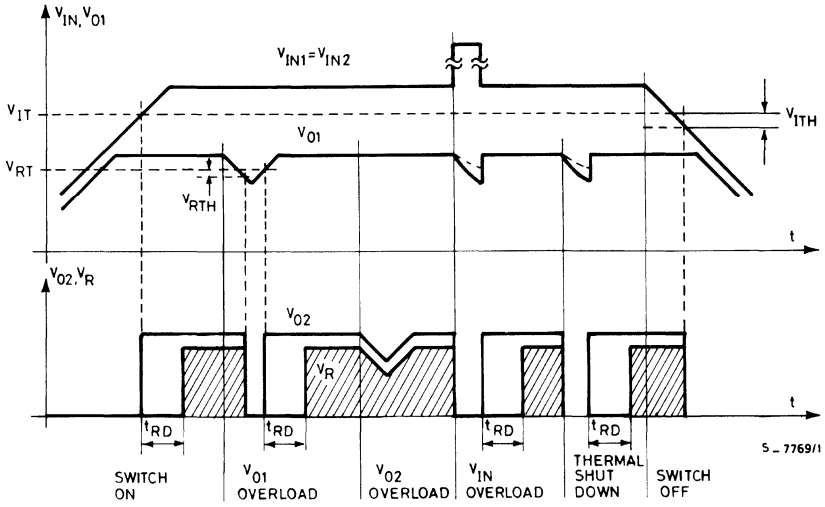
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

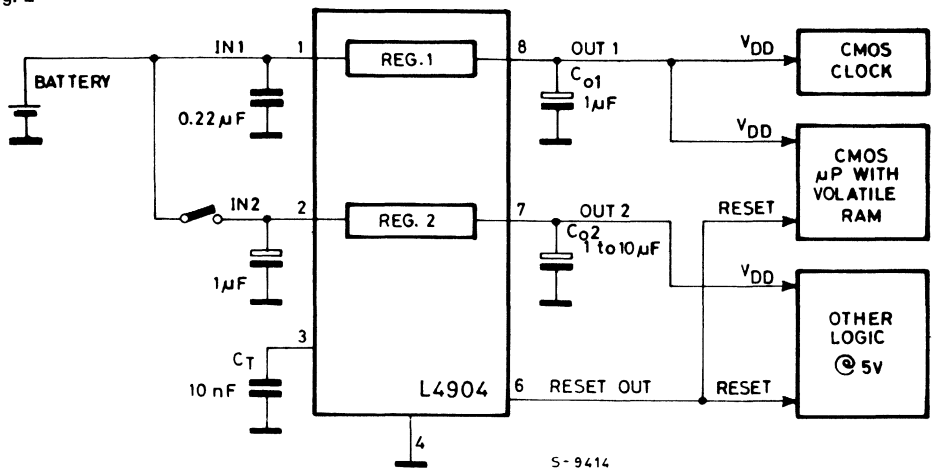
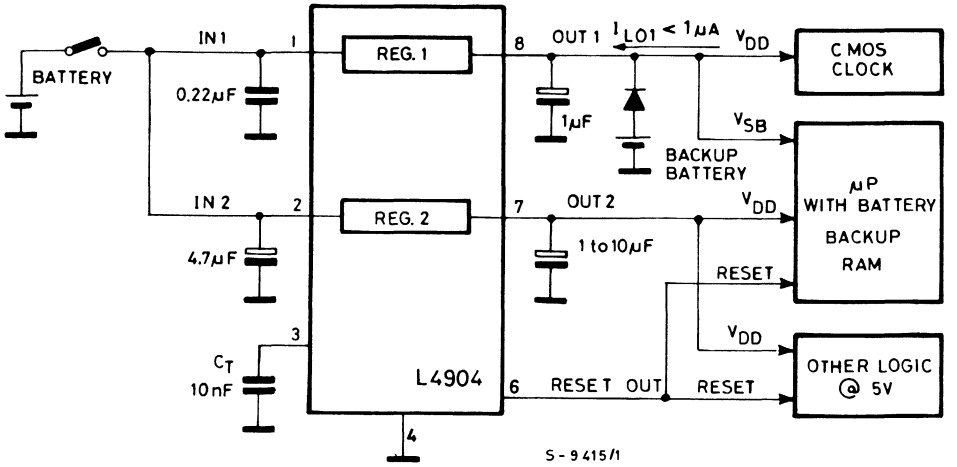


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

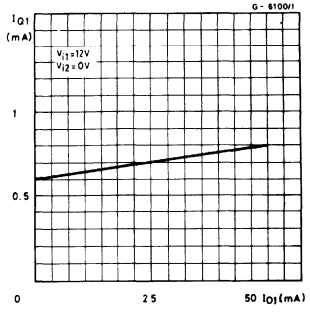


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

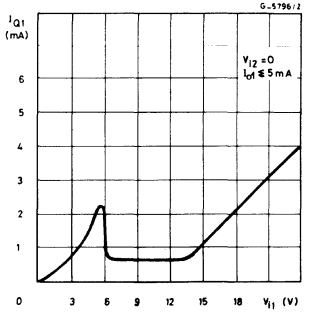


Fig. 6 - Total quiescent current vs. input voltage

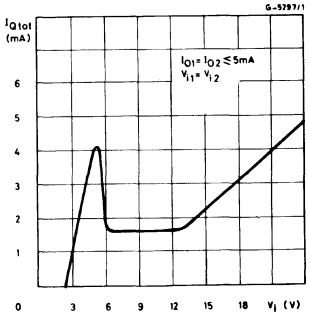
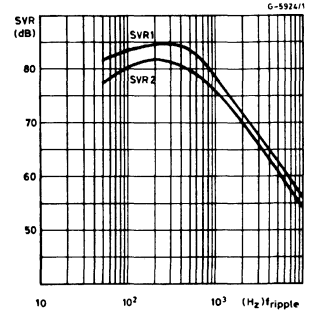


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4915

ADVANCE DATA

ADJUSTABLE VOLTAGE REGULATOR PLUS FILTER

- OUTPUT VOLTAGE ADJUSTABLE FROM 4 TO 11V
- HIGH OUTPUT CURRENT (UP TO 200mA)
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wide input voltage range.

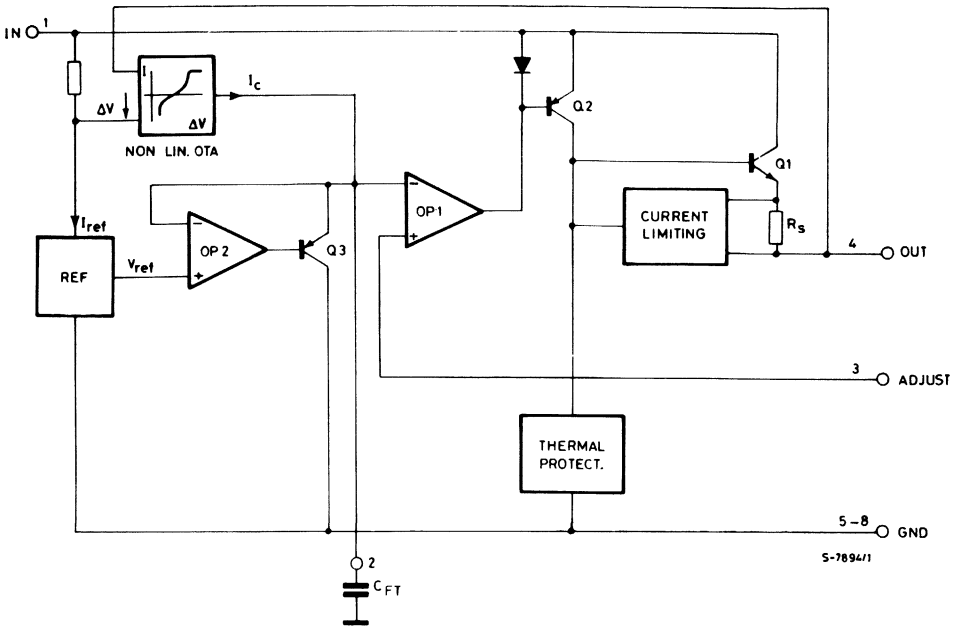
A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltage.

The non linear behaviour of this control circuitry allows a fast settling of the filter.

Power Minidip
(4 + 4)

ORDERING NUMBER: L4915

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_i	Peak input voltage (300ms)	40	V
V_i	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM

(Top view)

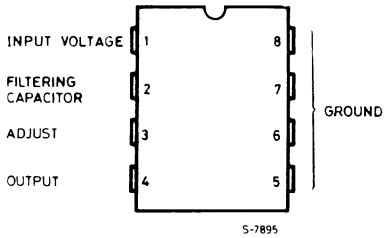
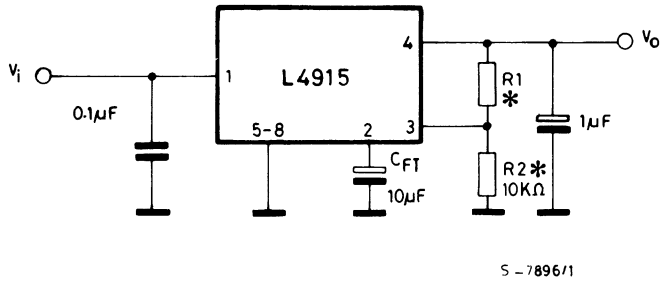


Fig. 1 - Application circuit



* OUTPUT VOLTAGE $V_o = \dfrac{2.5(R1 + R2)}{R2}$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, V_o = 8.5V, circuit of Fig. 1, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 6 to 18V I_o = 5 to 150mA	4		11	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	I_o = 5 to 150mA V_i = 6 to 10V		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ms		50	100	mV
ΔV_o	Load regulation (filter mode)	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ms		150	250	mV
V_{ref}	Internal voltage reference			2.5		V
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
I_{AD}	Adjust input current			40		nA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA Regulator		70		dB
		Filter mode		35 (*)		dB
I_{SC}	Short circuit current		200	300		mA
T_{on}	Switch on time	I_o = 150mA Filter mode		500 (*)		ms
		Regulator		300		ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 2).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\ (1 + \frac{R1}{R2}) =$$

$$V_{CFT}\ (1 + \frac{R1}{R2})$$

The ripple rejection is quite high (70dB) and independent to C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation and making it very sensible to every variation of the input voltage. On the contrary, a control loop on the L4915 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below ($V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The fipple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\ (jw) = \left| \frac{V_i\ (jw)}{V_{out}\ (jw)} \right| =$$

$$\left| 1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\ (1 + \frac{R1}{R2})} \right|$$

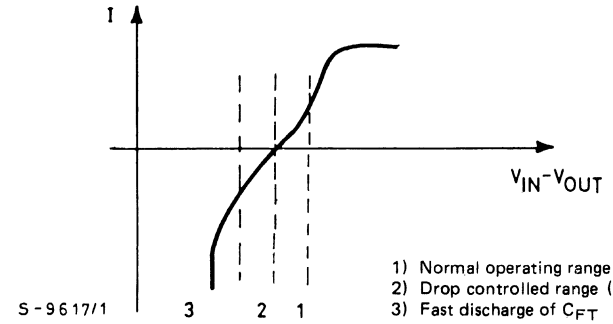
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With $C_{FT} = 10\mu F$; f = 100Hz; V_o = 8.5V a SVR of 35 is obtained.

Fig. 2 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Fig. 3 - Supply voltage rejection vs. input voltage

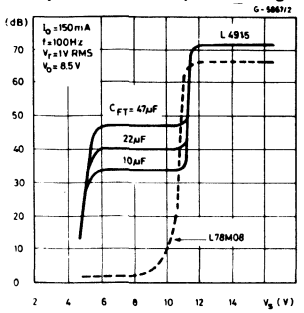


Fig. 4 - Supply voltage rejection vs. frequency

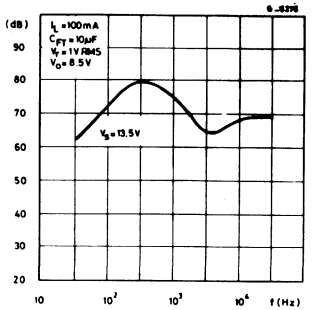


Fig. 5 - V_O vs. supply voltage (V_O = 8.5V)

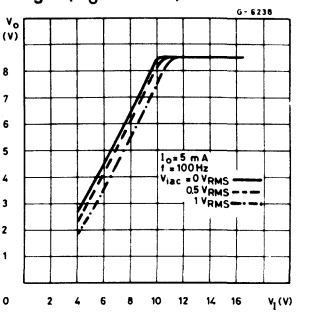


Fig. 6 - Quiescent current vs. input voltage (V_O = 8.5V)

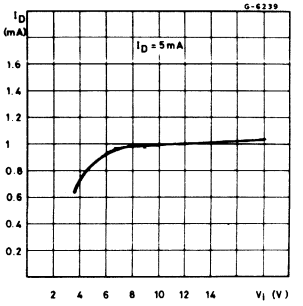
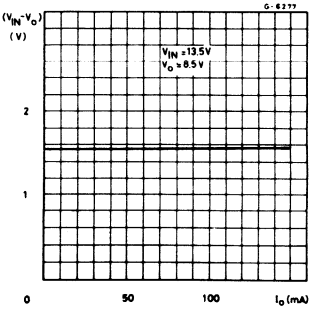


Fig. 7 - Dropout vs. load current



L4916

PRELIMINARY DATA

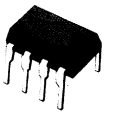
VOLTAGE REGULATOR PLUS FILTER

- FIXED OUTPUT VOLTAGE 8.5V
- 200mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

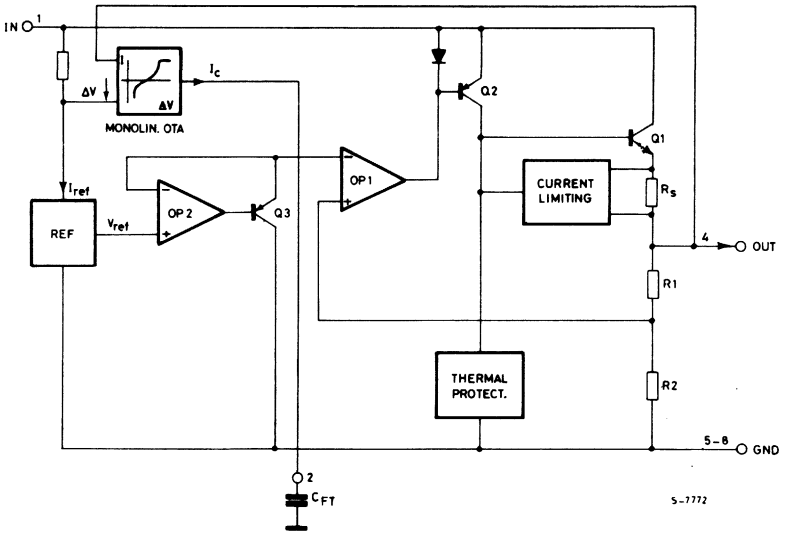
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDER CODE: L4916

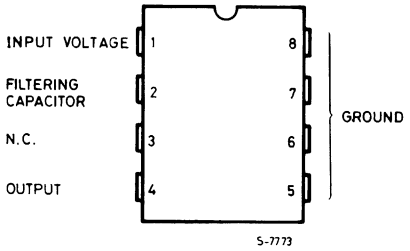
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_i	Peak input voltage (300 ms)	40	V
V_i	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, Test circuit of fig. 1, unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 12 to 18V I_o = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_i = 5 to 10V I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ms		50	100	mV
ΔV_o	Load regulation (filter mode)	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30μs,. t_{off} = ⩾ 1ms		150	250	mV
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		70 35 (*)		dB dB
I_{SC}	Short circuit current		200	300		mA
T_{on}	Switch on time	I_o = 150mA V_i = 5 to 11V V_i = 11 to 18V		500 (*) 300		ms ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

Fig. 1 - Test and Application Circuit

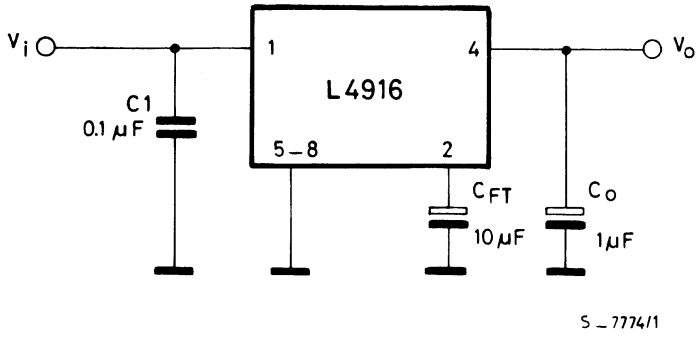
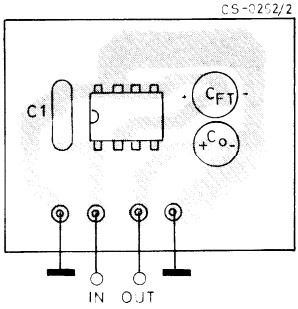


Fig. 2 - P.C. board and component layout of fig. 1 (1 : 1 scale)



PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 3).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\,(1 + \frac{R1}{R2}) =$$

$$V_{CFT}\,(1 + \frac{R1}{R2})$$

$$\frac{R1}{R2} = \text{INTERNALLY FIXED RATIO} = 2.4$$

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage.
On the contrary, a control loop on the L4916 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}.

So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The fipple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\,(jw) = \left|\frac{V_I\,(jw)}{V_{out}\,(jw)}\right| = \left|1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\,(1 + \frac{R1}{R2})}\right|$$

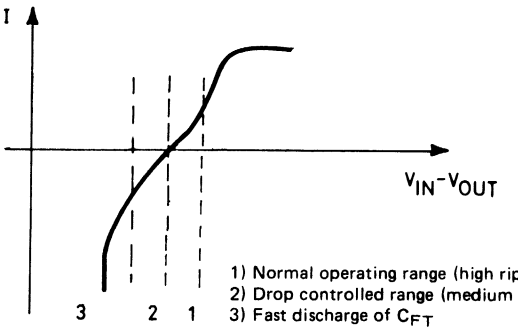
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}.
When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT}= 10 μF; f = 100 Hz a SVR of 35 is obtained.

Fig. 3 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

S-9617/1

Fig. 4 - Supply voltage rejection vs. input voltage

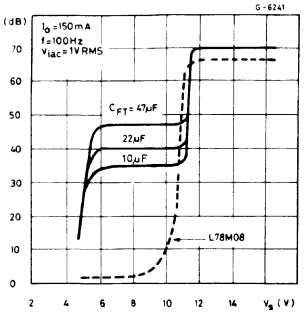


Fig. 5 - Supply voltage rejection vs. frequency

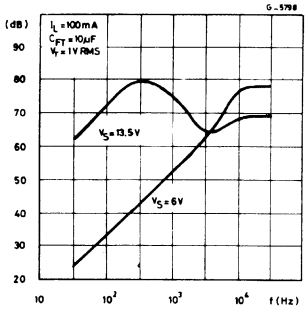


Fig. 6 - V_o vs. supply voltage

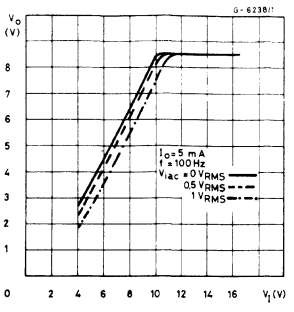


Fig. 7 - Quiescent current vs. input voltage

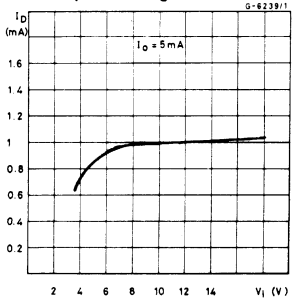


Fig. 8 - Dropout vs. load current

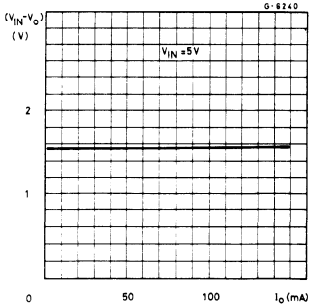
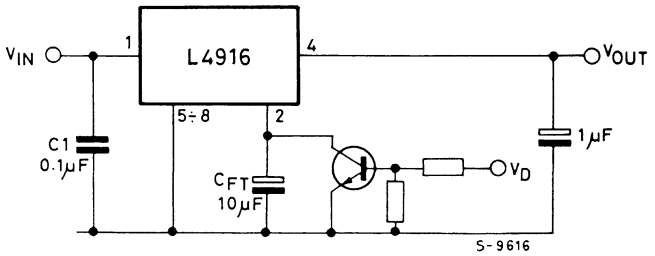


Fig. 9 - Inhibit function realized on C_{FT} pin.



L4918

ADVANCE DATA

VOLTAGE REGULATORS PLUS FILTER

- FIXED OUTPUT VOLTAGE 8.5V
- 250mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

The L4918 combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

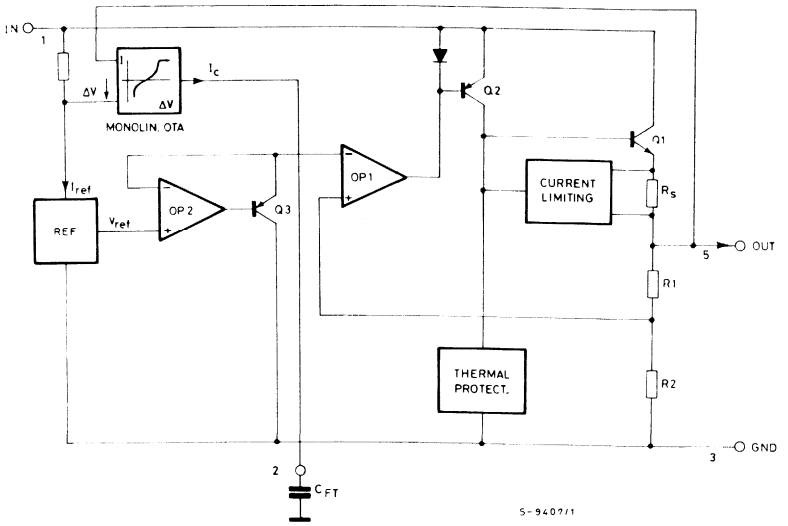
A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

The non linear behaviour of this control circuitry allows a fast setting of the filter.

Pentawatt®

ORDERING NUMBERS: L4918

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Peak input voltage (300ms)	40	V
V_s	DC voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

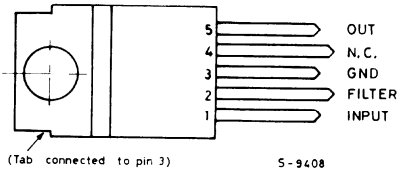
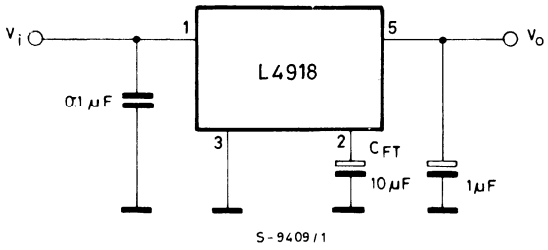


Fig. 1 - Application and test circuit



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_I = 13.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	Input voltage				20	V
V_O	Output voltage	V_I = 12 to 18V I_O = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_I = 5 to 10V I_O = 5 to 150mA		1.6	2.1	V
ΔV_O	Line regulation	V_I = 12 to 18V I_O = 10mA		1	20	mV
ΔV_O	Load regulation	I_O = 5 to 250mA t_{on} = 30μs t_{off} = ⩾ 1ns			100	mV
ΔV_O	Load regulation	V_I = 8.5V I_O = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ms		100	250	mV
I_q	Quiescent current	I_O = 5mA		1.0	2	mA
ΔI_q	Quiescent current change	V_I = 6 to 18V I_O = 5 to 150mA		0.05		mA
$\frac{\Delta V_O}{\Delta T}$	Output voltage drift	I_O = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_O = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		 70 35 (*)		 dB dB
I_{SC}	Short circuit current		250	300		mA
t_{on}	Switch on time	I_O = 150mA V_I = 5 to 11V V_I = 11 to 18V		 500 (*) 300		 ms ms
T_{JSD}	Thermal shut down			150		°C

(*) Depending of the C_{FT} capacitor

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through of OP2 and Q3, acting as an active zener diode of value V_{REF}.
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The output voltage is fixed to its nominal value:

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$$V_{CFT}\,(1 + \frac{R1}{R2})$$

$\frac{R1}{R2}$ = INTERNALLY FIXED RATIO = 2.4

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.
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Where:
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C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the tranconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
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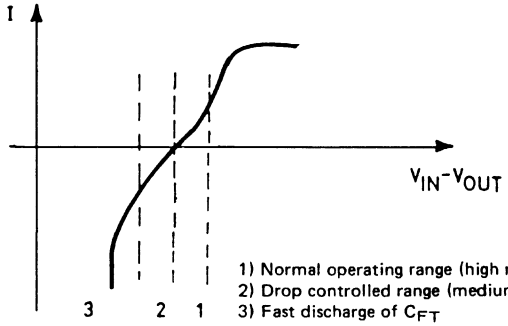
With C_{FT}= 10 μF; f = 100 Hz a SVR of 35 is obtained.

Fig. 2 - Nonliner transfer characteristic of the drop control unit



S-9617/1

1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Fig. 3 - Supply voltage rejection vs. frequency

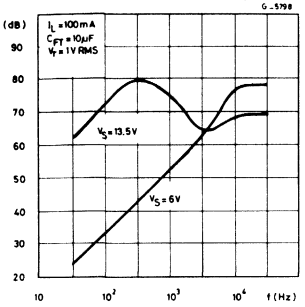


Fig. 4 - Supply voltage rejection vs. input voltage

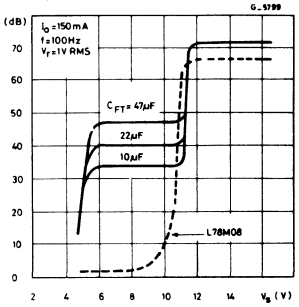
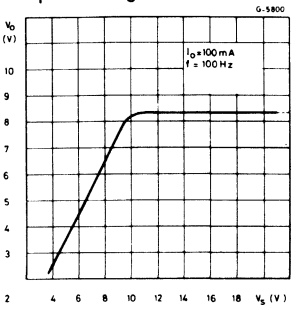


Fig. 5 - Output voltage vs input voltage



L4920
L4921

PRELIMINARY DATA

VERY LOW DROP ADJUSTABLE REGULATOR

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGES FROM 1.25V TO 20V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- +60/-60 TRANSIENT PEAK VOLTAGE
- SHORT CIRCUIT PROTECTION WITH FOLDBACK CHARACTERISTICS
- THERMAL SHUT-DOWN

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4V typ. at 0.4A), low quiescent current and comprehensive on-chip protection.

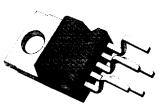
These devices are protected against load dump transients of ± 60V, input overvoltage, polarity reversal and over heating.

A foldback current limiter protects against load short circuits.

The output voltage is adjustable through an external divider from 1.25V to 20V. The minimum operating input voltage is 5.2V.

These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In battery backup and standby applications the low consumption of these devices extends battery life.



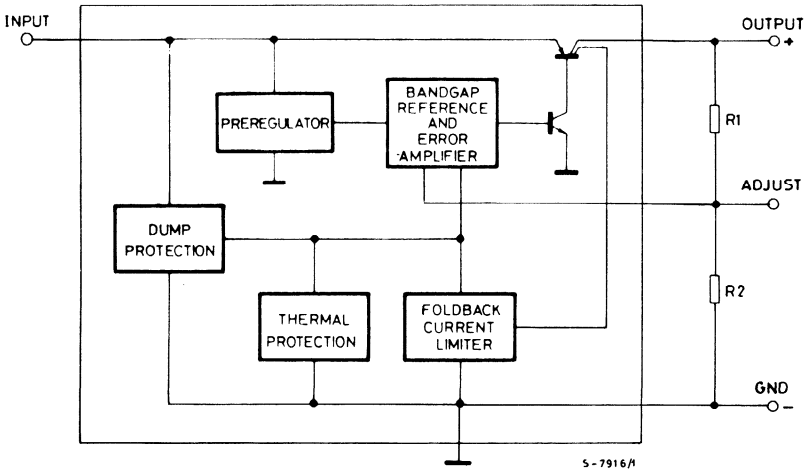
Pentawatt®

Minidip (4 + 4)

ORDERING NUMBERS:

L4920 L4921

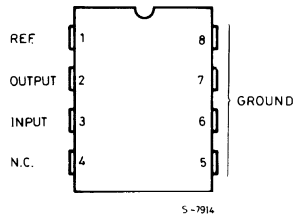
BLOCK DIAGRAM



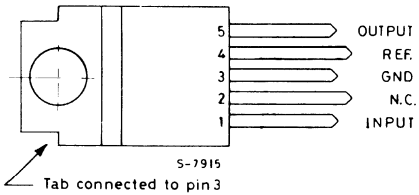
ABSOLUTE MAXIMUM RATINGS

V_i	DC input operating voltage	26	V
V_t	Positive transient peak voltage (t = 300ms 1% duty cycle)	+60	V
V_t	Negative transient peak voltage (t = 100ms 1% duty cycle)	-60	V
V_i	Reverse input voltage	-18	V
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature	-40 to 150	°C

CONNECTION DIAGRAMS (top view)

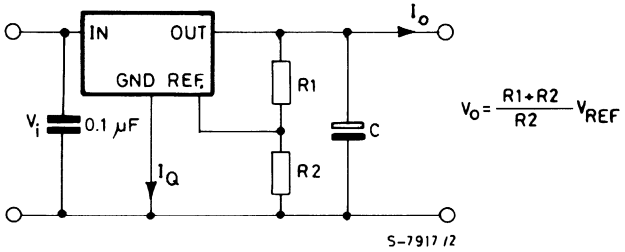


Minidip



Pentawatt

APPLICATION CIRCUIT



C = 100µF is required for stability (ESR ⩽ 3Ω over T range)
R2 = 6.2KΩ.

THERMAL DATA

			Minidip (4 + 4)	Pentawatt
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	80°C/W	60°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction pins	max	15°C/W	–
$R_{th\ j\text{-}case}$	Thermal resistance junction case	max	–	4°C/W

ELECTRICAL CHARACTERISTICS (For V_i = 14.4V V_o = 5V; T_j = 25°C; C = 100μF; R2 = 6.2KΩ unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating input voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o+0.7		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.2		26	V
V_{REF}	Reference voltage	$5.2V < V_i < 26V$ $I_o \leq 400mA$ (*)	1.20	1.25	1.30	V
ΔV_o	Line regulation	$V_o + 1V < V_i < 26V$ $V_o \geq 4.5V$ I_o = 5mA		1	10	mV/V_o
ΔV_o	Load regulation	$5mA < I_o < 400mA$ (*) $V_o \geq 4.5V$		3	15	mV/V_o
V_D	Dropout voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	 0.4 0.7	V V V
I_D	Quiescent current	I_o = 0mA $V_o + 1V < V_i < 26V$		0.8	3	mA
		I_o = 400mA (*) $V_o + 1V < V_i < 26V$		65	100	mA
I_o	Maximum output current			650	900	mA
I_{OSC}	Short circuit output current (*)		200	350	500	mA
V_R	Reverse polarity input voltage (DC)	$V_o \geq -1.5V$ $R_L \leq 500\Omega$			-18	V

(*) Foldback protection

Fig. 1 - Output voltage vs. temperature

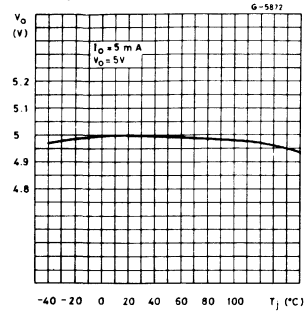


Fig. 2 - Foldback current limiting

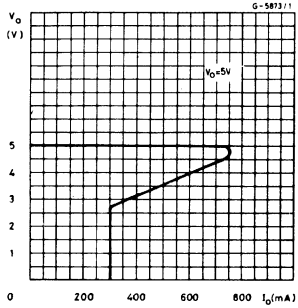
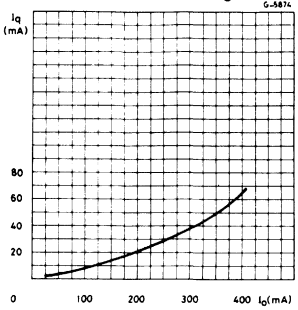


Fig. 3 - Quiescent current vs. output current (V_o = 5V)



APPLICATION INFORMATION

1) The L4920 and L4921 have $V_{REF} \cong 1.25V$. Then the output voltage can be set down to V_{REF} but V_i must be greater than 5.2V.
2) As the regulator reference voltage source works in closed loop, the reference voltage may change in foldback condition.
3) For applications with high V_i the total power dissipation of the device with respect to the thermal resistance of the package may be limiting the application. The total power dissipation is:

$$P_{tot} = V_i I_q + (V_i - V_o) I_o$$

A typical curve giving the quiescent current I_q as a function of the output current I_o is shown in fig. 3.

L4940

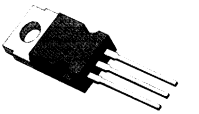
ADVANCE DATA

VERY LOW DROP 1.5A REGULATOR

- PRECISE 5V OUTPUT (± 2%)
- LOW DROPOUT VOLTAGE (400mV TYP. AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUT DOWN
- SHORT CIRCUIT CURRENT LIMITER
- OVERVOLTAGE PROTECTION
- REVERSE POLARITY PROTECTION

The L4940 is a very low input/output voltage drop, low quiescent current and high output current capability IC particularly useful in applications such as battery powered systems where power dissipation is a design constraint.

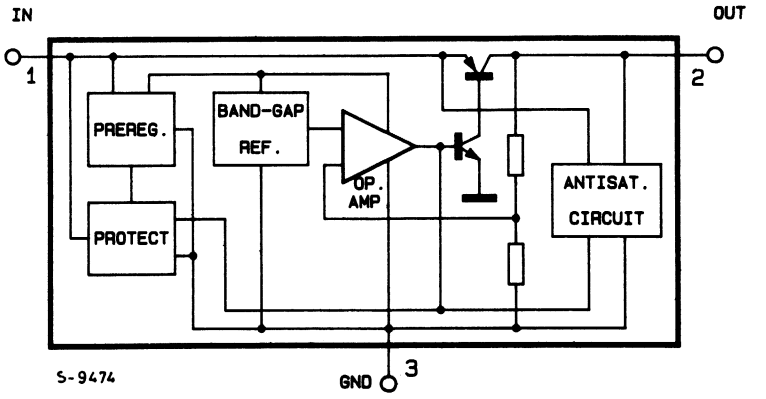
Standard regulator features such as thermal shut down, current limiter and overvoltage protection are also provided.



TO-220

ORDERING NUMBER: L4940BV

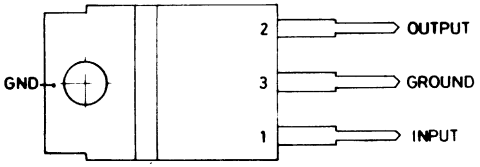
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

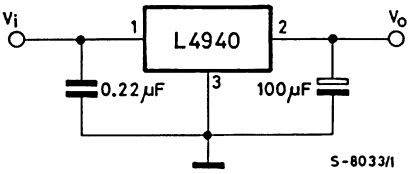
V_I	Forward input voltage (R_O = 100Ω)	40	V
V_i	Reverse input voltage (R_O = 100Ω)	-15	V
T_{op}	Operating junction temperature range	-40 to 125	°C
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to 150	°C

CONNECTION DIAGRAM (top view)



S-2568/1

TEST AND APPLICATION CIRCUIT



S-8033/1

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

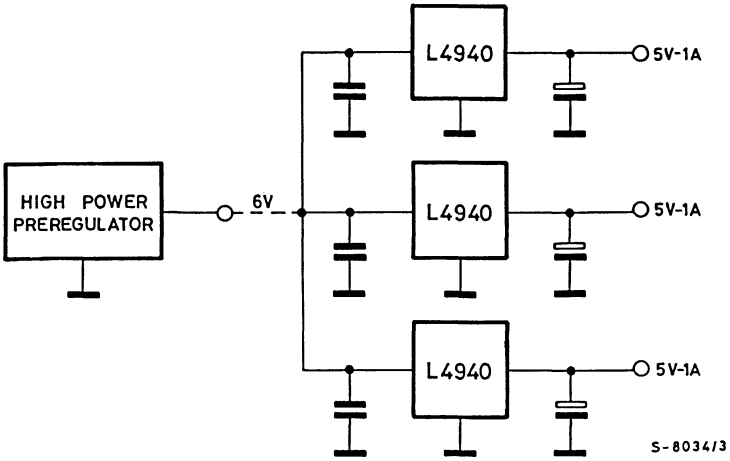
ELECTRICAL CHARACTERISTICS (V_I = 14V, T_j = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 5mA	4.9	5	5.1	V
V_O	Output voltage	V_I = 6V to 14V I_O = 5mA to 1A	4.8	5	5.2	V
V_i	Operating input voltage	(*) See note			18	V
V_O	Line regulation	6V ≤ V_i ≤ 18V I_O = 5mA		5		mV
V_O	Load regulation	I_O = 50mA to 1A		15		mV
I_d	Quiescent current	6V ≤ V_i ≤ 16V I_O = 5mA		5		mA
		I_O = 1A		50		
V_I-V_O	Dropout voltage	I_O = 1A		400		mV
		I_O = 100mA		100		
$\Delta V_O/\Delta T$	Output voltage drift			1		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_O = 0.5A		74		dB
I_O	Current limit			1.3		A
Z_O	Output impedance	I_O = 200mA f = 120Hz		30		mΩ
E_N	Output noise voltage	f = 100Hz to 100KHz I_O = 10mA		100		μV rms

(*) For a DC input voltage 16V < V_i < 40V the device is not operating

APPLICATION INFORMATION

Fig. 1 - Distributed supply with on-card L4940 low-drop regulators



Advantages of this application are:

- Card isolation
- Thermal and short-circuit protection
- High efficiency (80%), like switching regulators, but without radiation and intermodulation problems

L4941

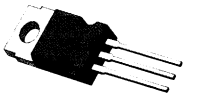
ADVANCE DATA

VERY LOW DROP 1A REGULATOR

- PRECISE 5V OUTPUT (± 2%)
- LOW DROPOUT VOLTAGE (450mV TYP. AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUT DOWN
- SHORT CIRCUIT CURRENT LIMITER
- OVERVOLTAGE PROTECTION
- REVERSE POLARITY PROTECTION

The L4941 is a very low input/output voltage drop, low quiescent current and high output current capability IC particularly useful in applications such as battery powered systems where power dissipation is a design constraint.

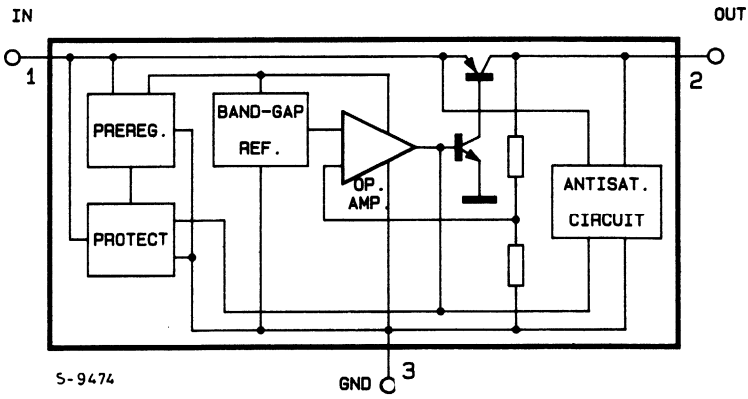
Standard regulator features such as thermal shut down, current limiter and overvoltage protection are also provided.



TO-220

ORDERING NUMBER: L4941BV

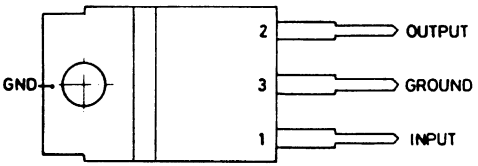
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

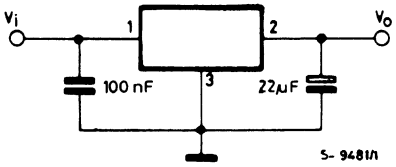
V_i	Forward input voltage (R_O = 100Ω)	40	V
V_i	Reverse input voltage (R_O = 100Ω)	-15	V
T_{op}	Operating junction temperature range	-40 to 125	°C
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to 150	°C

CONNECTION DIAGRAM
(Top view)



S-2568/1

TEST AND APPLICATION CIRCUIT



S-9481/1

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_I = 14V, T_j = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 5mA	4.9	5	5.1	V
V_O	Output voltage	V_i = 6V to 14V I_O = 5mA to 1A	4.8	5	5.2	V
V_i	Operating input voltage	(*) See note			16	V
V_O	Line regulation	6V ⩽ V_i ⩽ 16V I_O = 5mA		5	25	mV
V_O	Load regulation	I_O = 50mA to 1A		15	35	mV
I_d	Quiescent current	6V ⩽ V_i ⩽ 16V I_O = 5mA		3.5	10	mA
		I_O = 1A		20	50	
V_i-V_O	Dropout voltage	I_O = 1A		450	700	mV
		I_O = 100mA		150	250	
$\Delta V_O/\Delta T$	Output voltage drift			0.6		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_O = 0.5A	60			dB
I_O	Current limit			1.3		A
Z_O	Output impedance	I_O = 200mA f = 120Hz		30		mΩ
E_N	Output noise voltage	f = 100Hz to 100KHz I_O = 10mA		100		μV rms

(*) For a DC input voltage 16V < V_i < 40V the device is not operating

Fig. 1 - Dropout output voltage vs. current

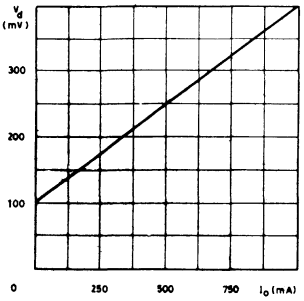


Fig. 2 - Quiescent current vs. output current

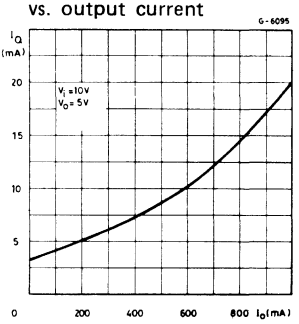


Fig. 3 - Quiescent current vs. load current

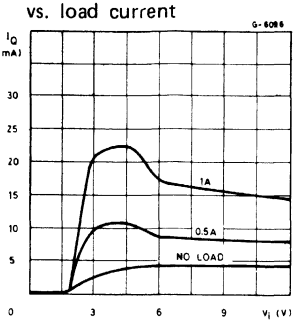


Fig. 4 - Low voltage behaviour

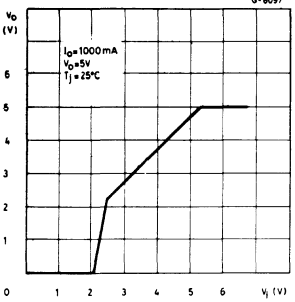


Fig. 5 - Output at voltage extremes

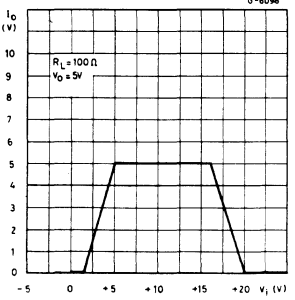


Fig. 6 - Line transient response

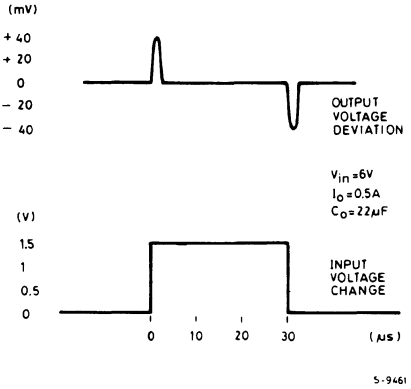
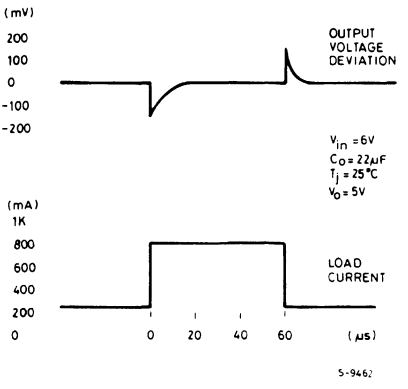
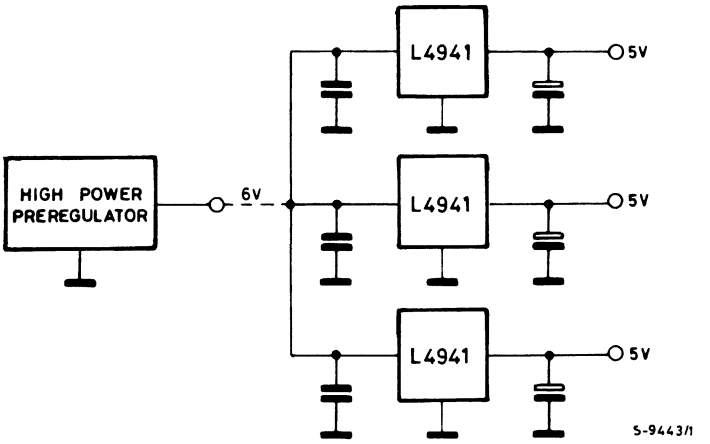


Fig. 7 - Load transient response



APPLICATION INFORMATION

Fig. 8 - Distributed supply with on-card L4941 low-drop regulators



Advantages of this application are:

- Card isolation
- Thermal and short-circuit protection
- High efficiency (80%), like switching regulators, but without radiation and intermodulation problems

L4960

PRELIMINARY DATA

2.5A POWER SWITCHING REGULATOR

- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration. Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.

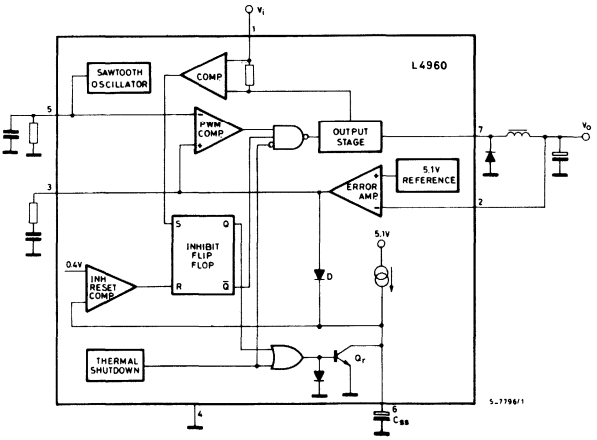
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

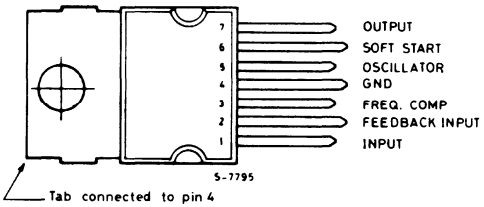
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	I_o = 2.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V	$V_o = V_{ref}$ I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	I_o = 0.5A to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	V_i = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 2A			1.4	3	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		2.5			A
I_{7L}	Current limiting threshold (pin 7)	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		3		4.5	A
I_{SH}	Input average current	V_i = 46V; output short-circuit			30	60	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		75		%
		I_o = 2A	V_o = 12V		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$	I_o = 1A	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	I_o = 2A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	uA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

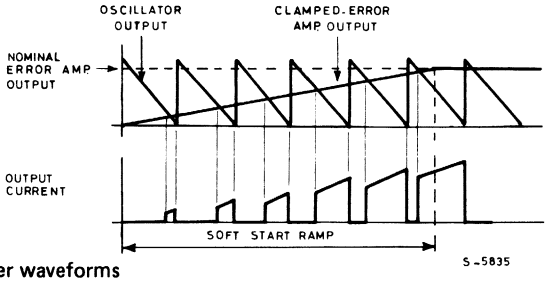


Fig. 2 - Current limiter waveforms

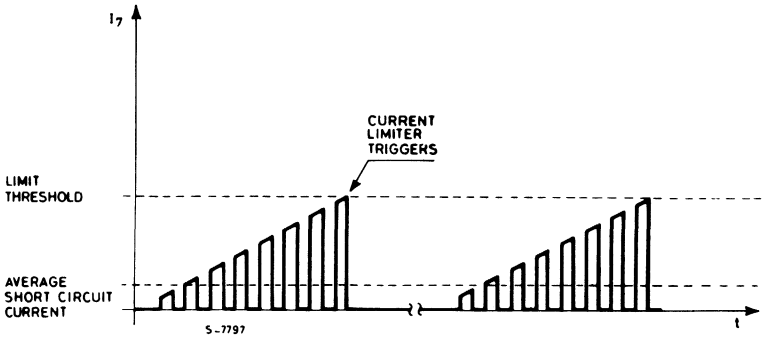
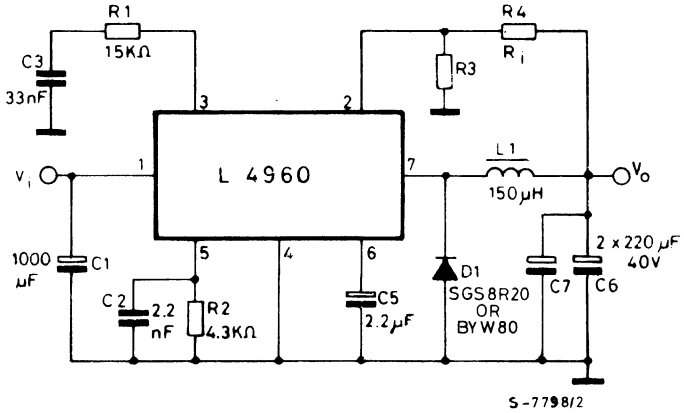


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150μH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

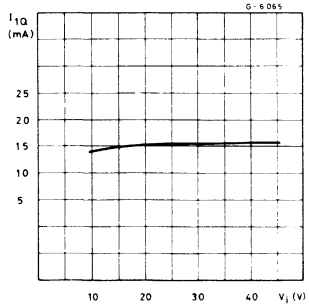


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

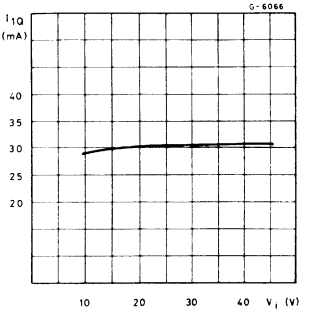


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

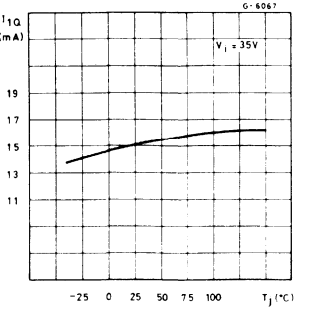


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

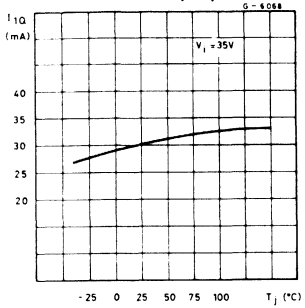


Fig. 8 - Reference voltage (pin 2) vs. V_i

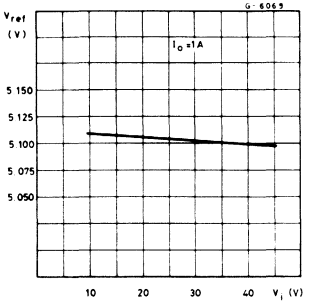


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

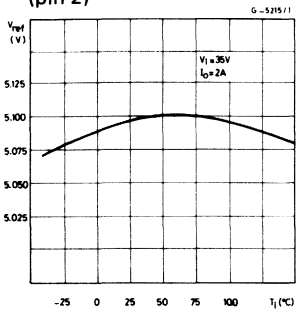


Fig. 10 - Open loop frequency and phase responde of error amplifier

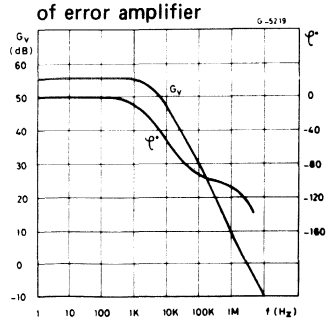


Fig. 11 - Switching frequency vs. input voltage

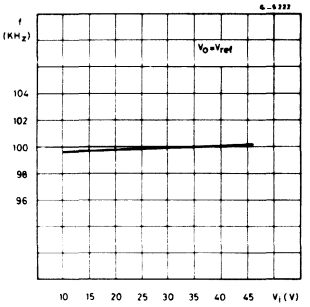


Fig. 12 - Switching frequency vs. junction temperature

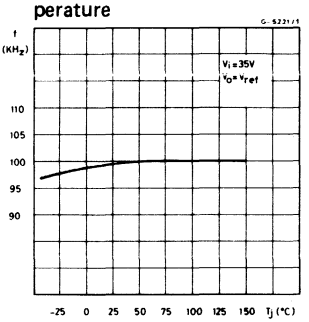


Fig. 13 - Switching frequency vs. R2 (see test circuit)

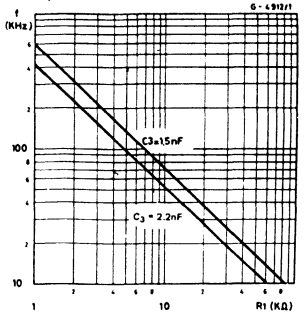


Fig. 14 - Line transient response

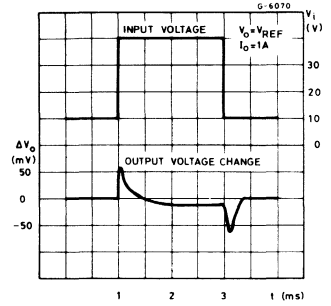


Fig. 15 - Load transient response

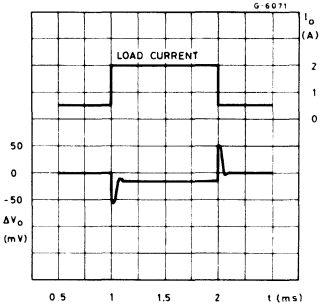


Fig. 16 - Supply voltage ripple rejection vs. frequency

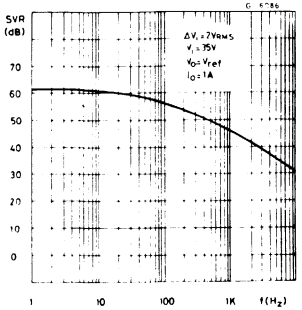


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

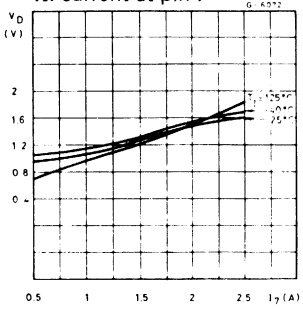


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

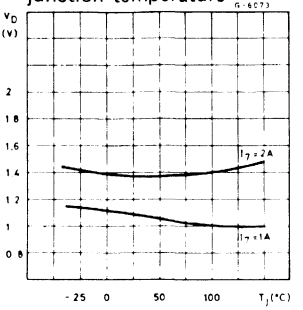


Fig. 19 - Power dissipation derating curve

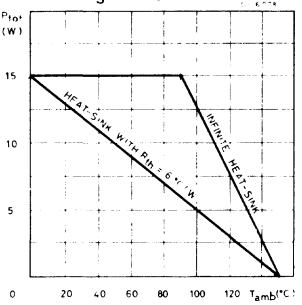


Fig. 20 - Efficiency vs. output current

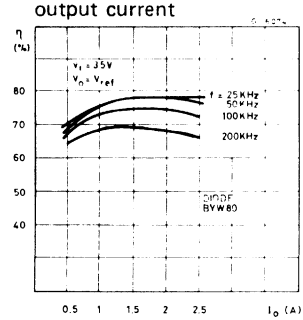


Fig. 21 - Efficiency vs. output current

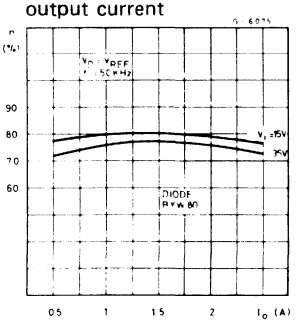


Fig. 22 - Efficiency vs. output current

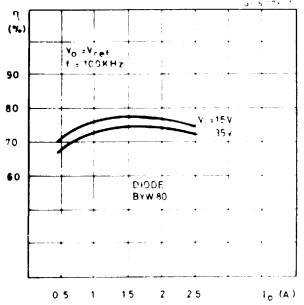
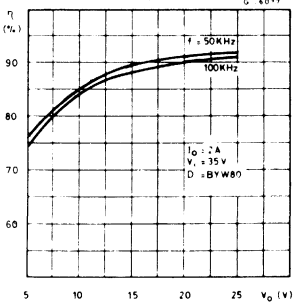
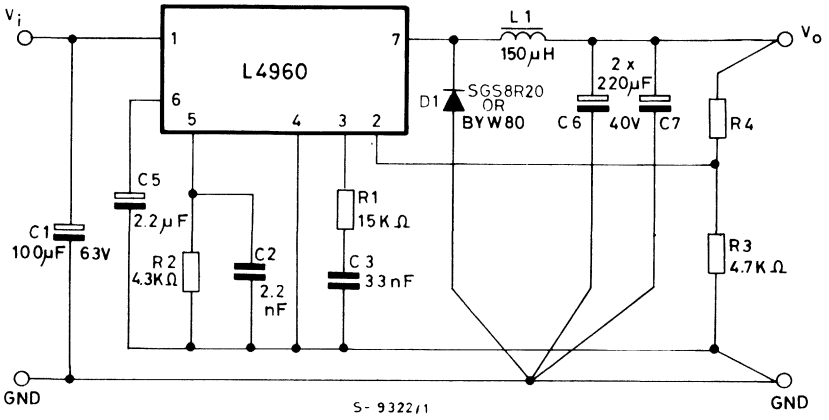


Fig. 23 - Efficiency vs. output voltage



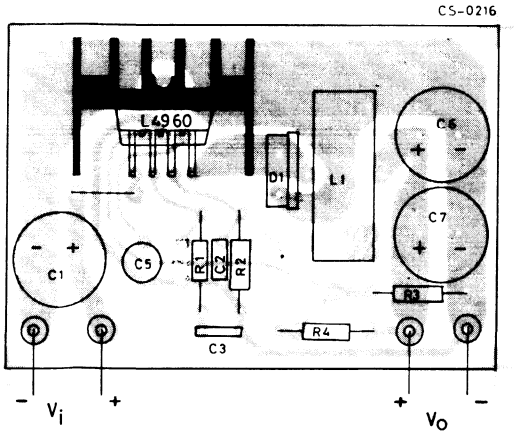
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required

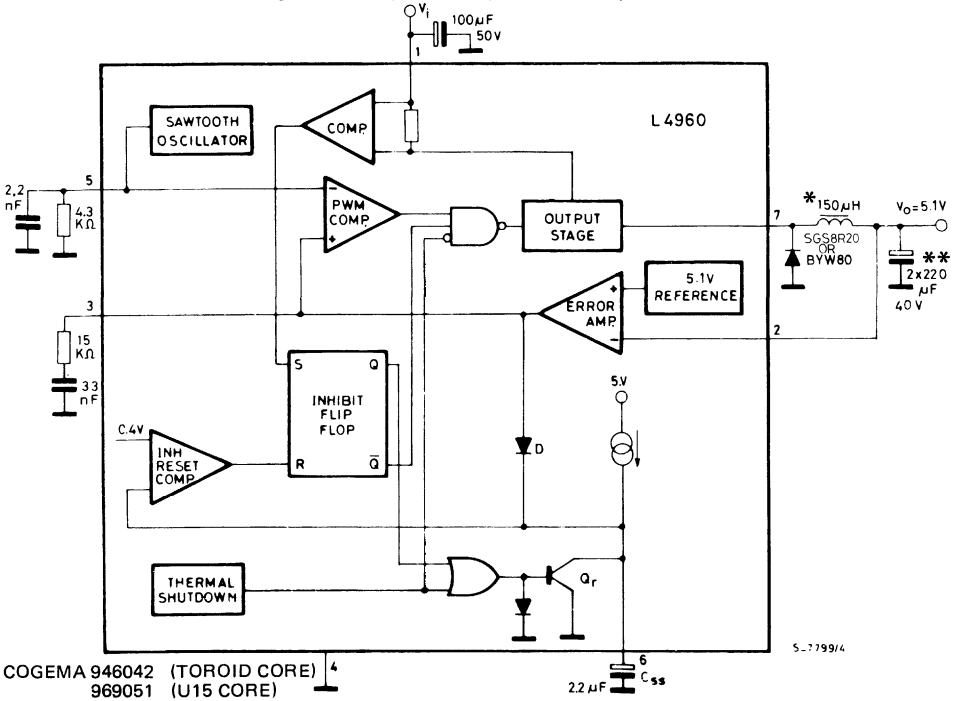
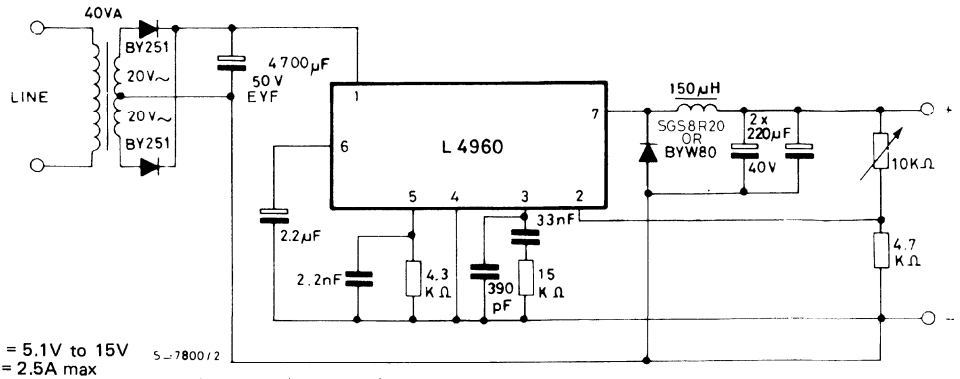


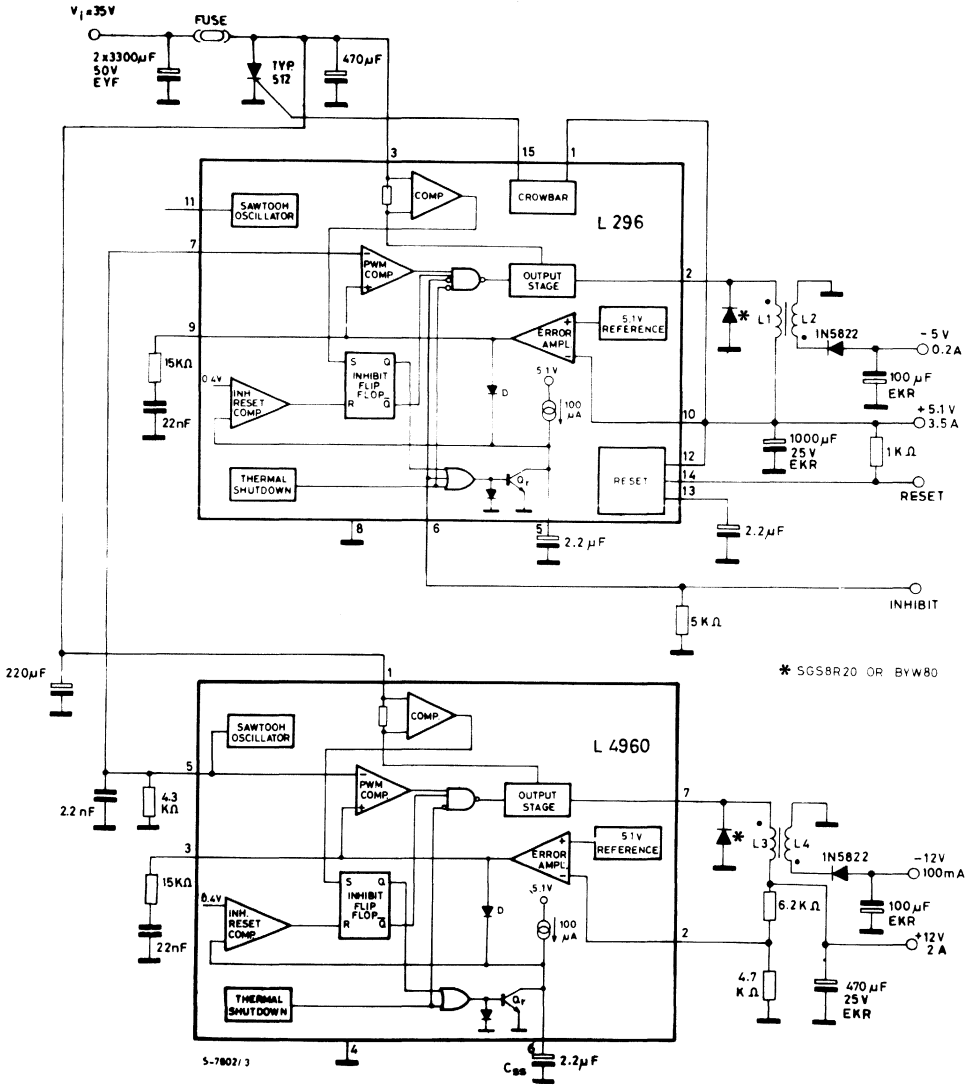
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

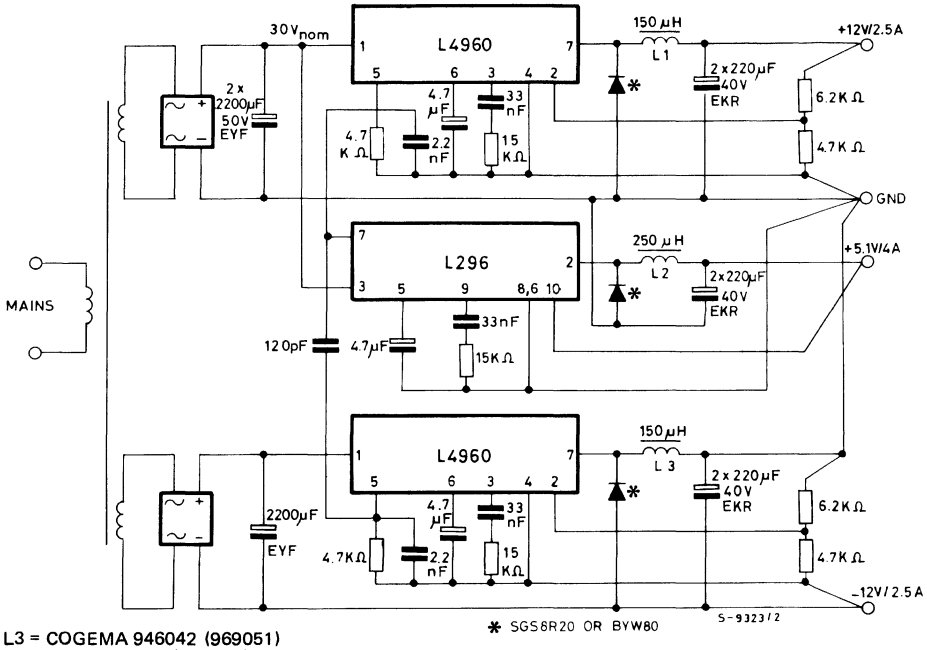
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



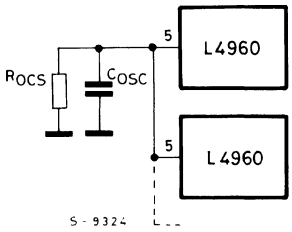
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



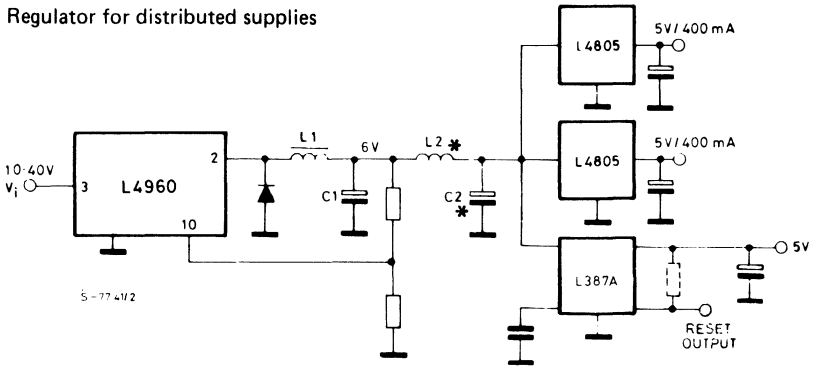
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D3 = SGS8R20 or BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

Fig. 31 - Regulator for distributed supplies

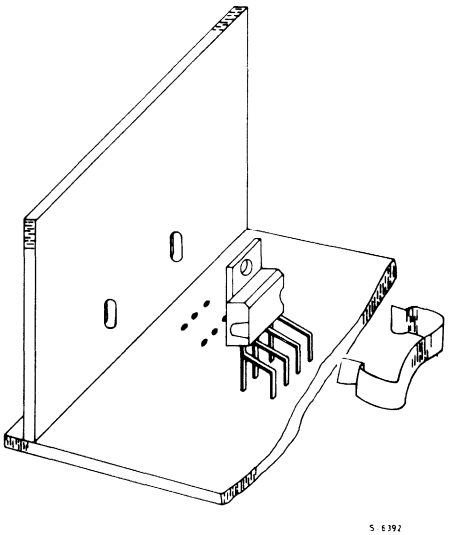


* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4960

MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



L4962

PRELIMINARY DATA

1.5A POWER SWITCHING REGULATOR

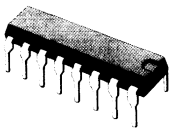
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

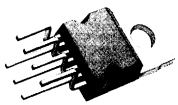
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

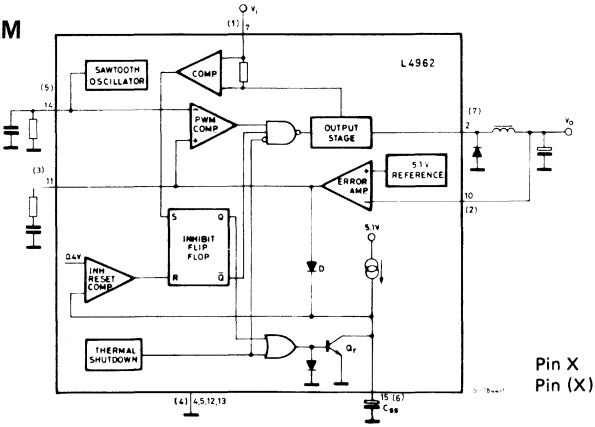
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leq 90°C$ (Powerdip)	4.3	W
	$T_{case} \leq 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

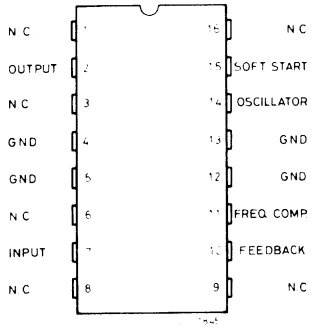
BLOCK DIAGRAM

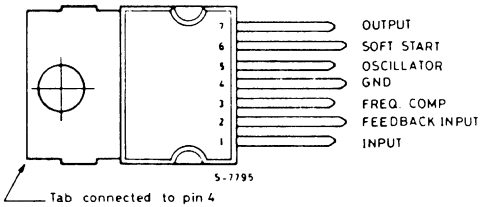


Pin X = Powerdip
Pin (X) = Heptawatt

CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	–
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	–	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V	$V_o = V_{ref}$ I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A			1.5	2	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		2		3.3	A
I_{SH}	Input average current	V_i = 46V; output short-circuit			15	30	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		70		%
		I_o = 1A	V_o = 12V		80		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$	I_o = 1A	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

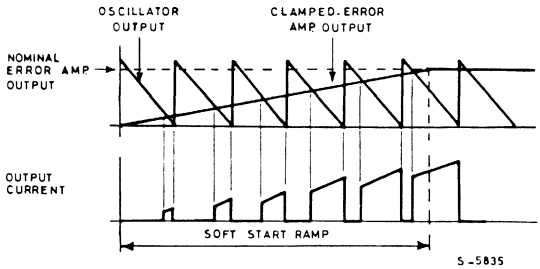


Fig. 2 - Current limiter waveforms

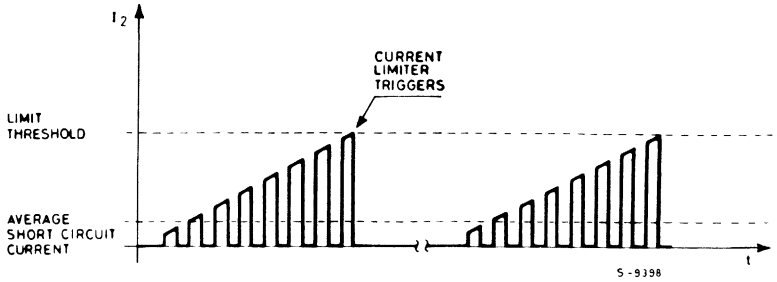
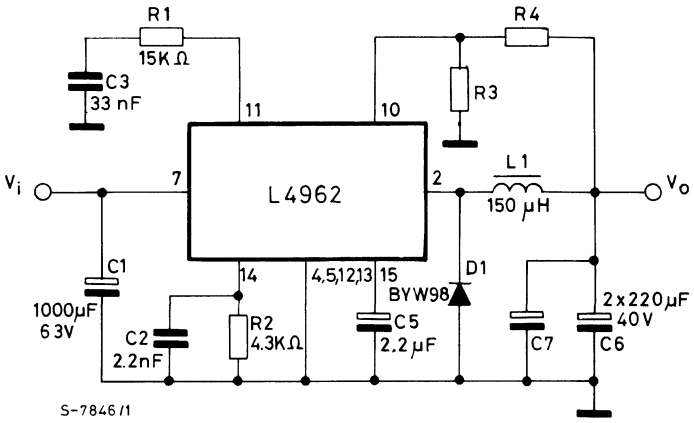


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

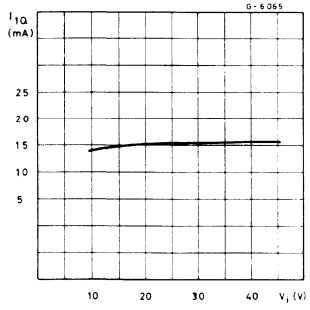


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

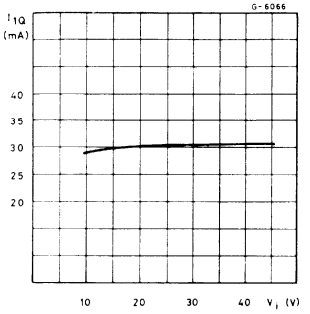


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

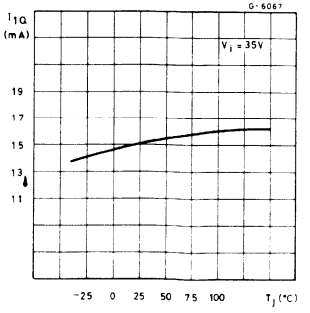


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

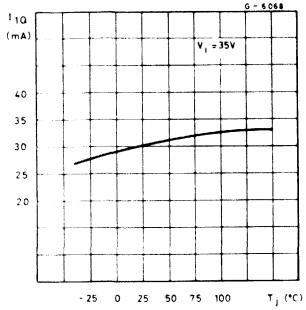


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

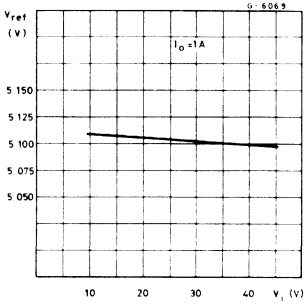


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

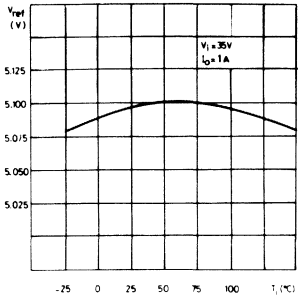


Fig. 10 - Open loop frequency and phase response of error amplifier

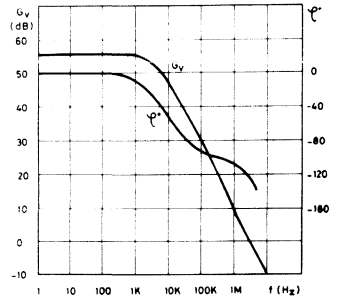


Fig. 11 - Switching frequency vs. input voltage

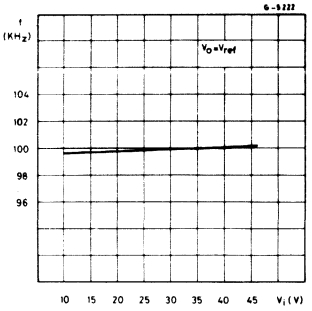


Fig. 12 - Switching frequency vs. junction temperature

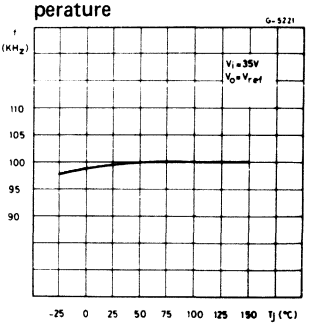


Fig. 13 - Switching frequency vs. R2 (see test circuit)

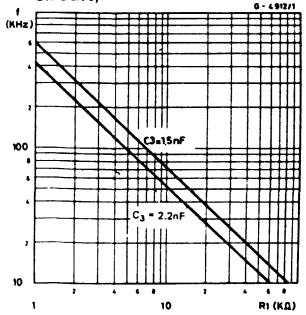


Fig. 14 - Line transient response

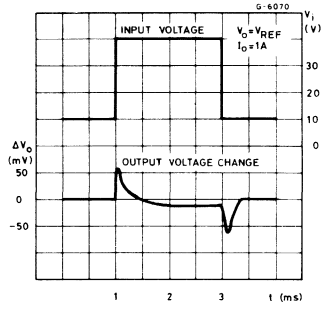


Fig. 15 - Load transient response

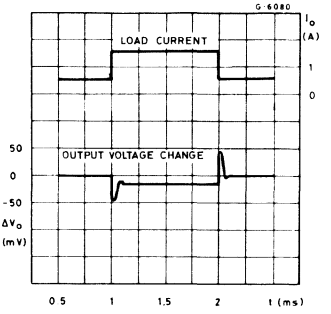


Fig. 16 - Supply voltage ripple rejection vs. frequency

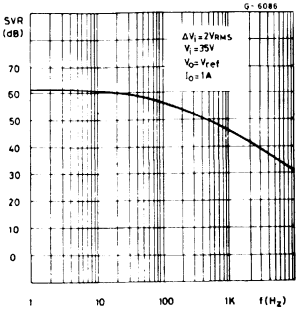


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

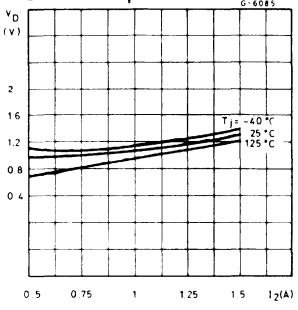


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

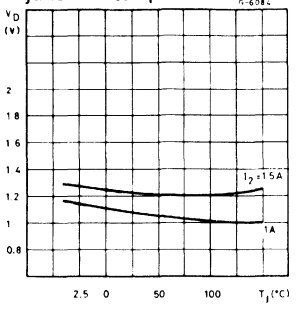


Fig. 19 - Efficiency vs. output current

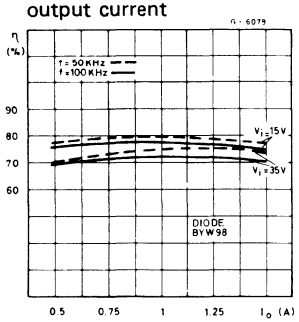


Fig. 20 - Efficiency vs. output current

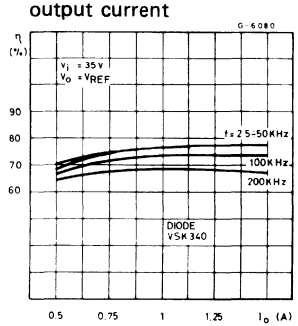


Fig. 21 - Efficiency vs. output current

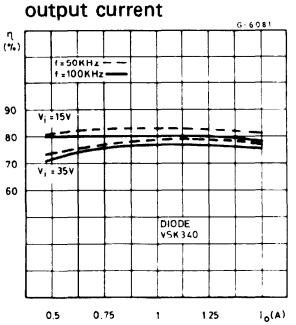


Fig. 22 - Efficiency vs. output voltage

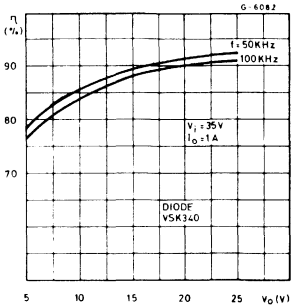


Fig. 23 - Efficiency vs. output voltage

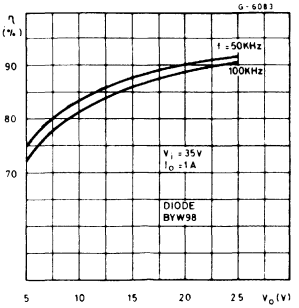
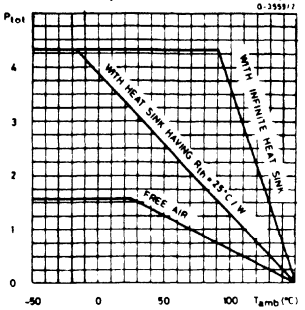
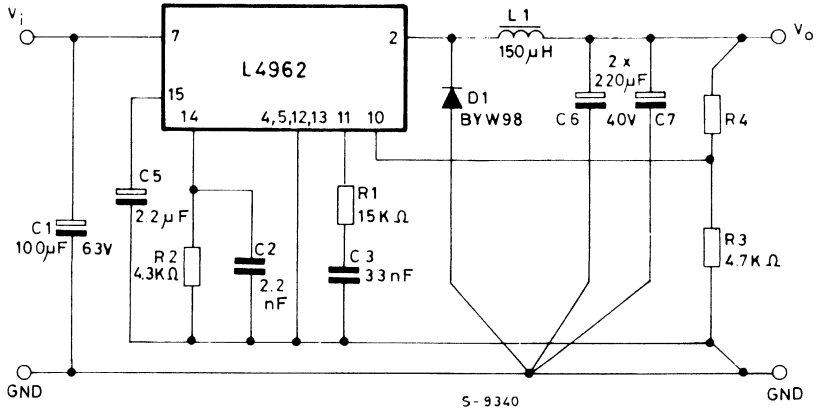


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



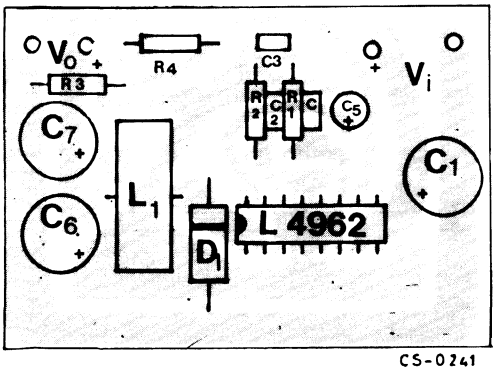
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

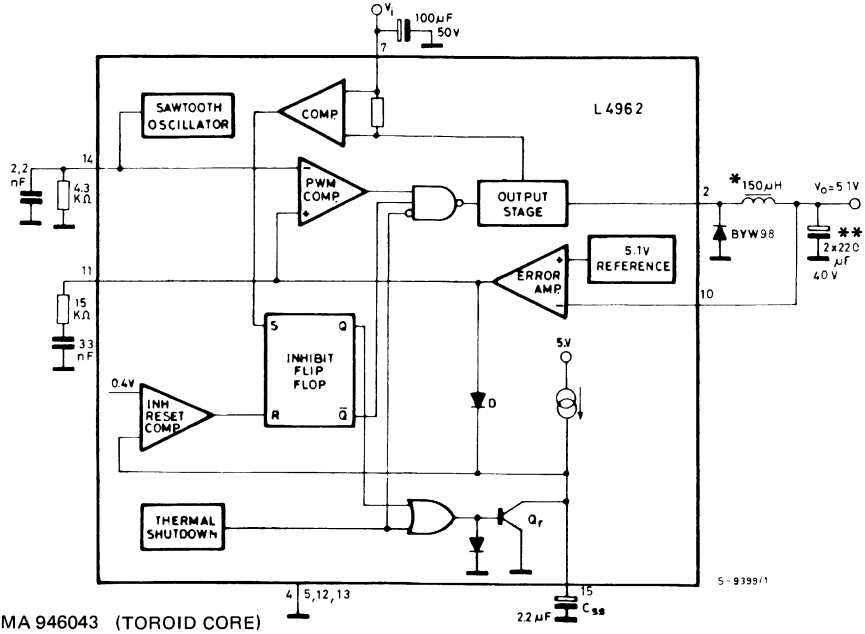
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

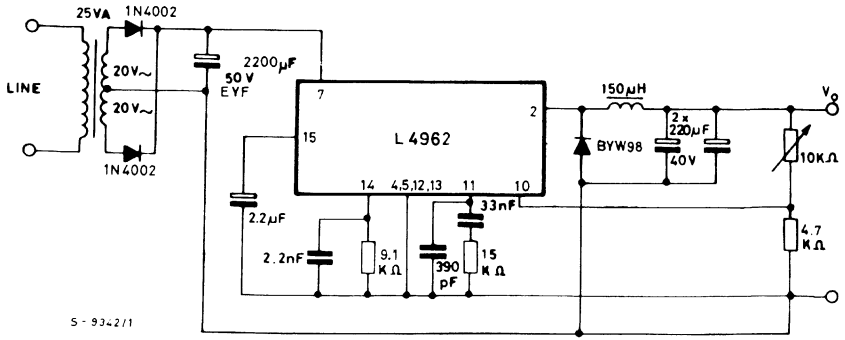
APPLICATION INFORMATION (continued)

Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)
** EKR (ROE)

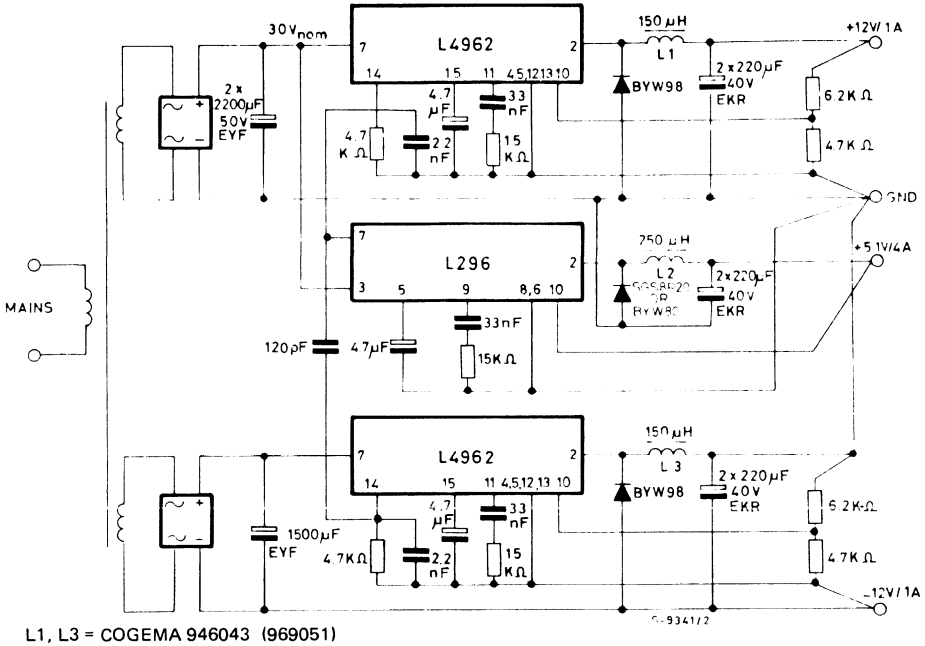
Fig. 27 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

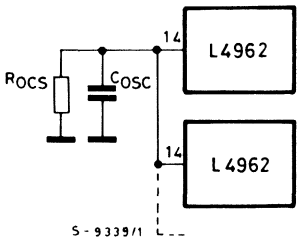
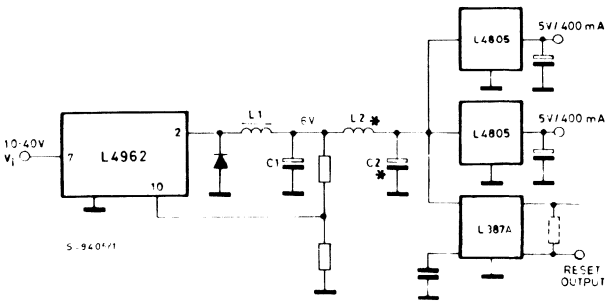


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

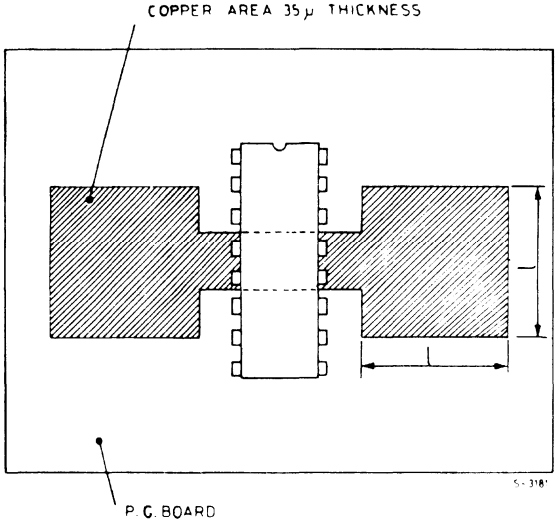
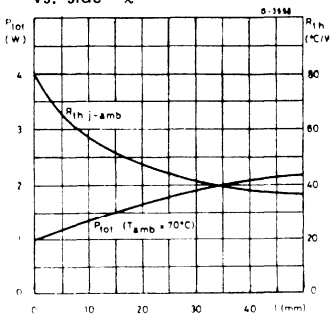


Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"



L6202

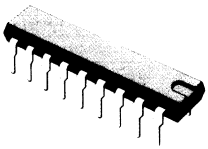
ADVANCE DATA

0.3Ω DMOS FULL BRIDGE DRIVER

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 1.5A
- $R_{DS\ (ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

The L6202 is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimise the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 1.5A RMS at motor supply voltages up to 48V and efficiently at high switching speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6202 is mounted in an 18-lead powerdip package and the six center pins are used to conduct heat to the PCB. Even at the full rated current and voltage no external heatsink is required at normal operating temperatures.

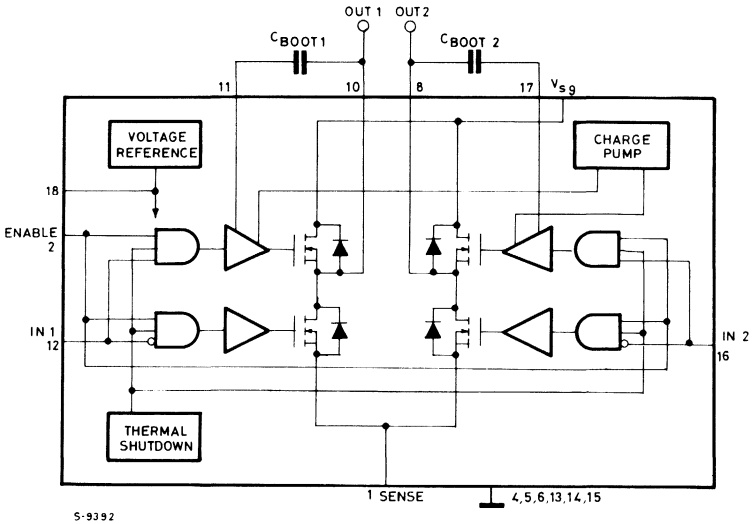
MultiPower BCD Technology



Powerdip 12+3+3

ORDERING NUMBER: L6202

BLOCK DIAGRAM

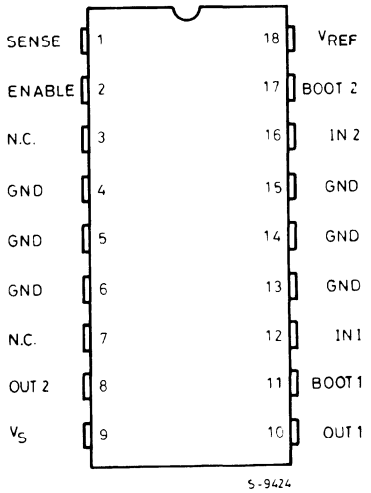


ABSOLUTE MAXIMUM RATINGS

V_s	Power supply (V_{EN} = Low)	60	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	Pulsed output current (note 1)	5	A
	- non repetitive (< 1ms)	10	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap supply	60	V
P_{tot}	Total power dissipation (T_{pins} = 90°C)	5	W
	(T_{amb} = 70°C no copper area on PCB)	1.3	W
	(T_{amb} = 70°C 4cm^2 copper area on PCB)	2	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (Fig. 21)	max	60	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control.
2	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	NO CONNECTION	
4	GND	Common ground terminal.
5	GND	Common ground terminal.
6	GND	Common ground terminal.
7	NO CONNECTION	
8	OUT2	Output of the half bridge.
9	V_s	Supply voltage.
10	OUT1	Output of the half bridge.
11	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
12	IN1	Digital input from the motor controller.
13	GND	Common ground terminal.
14	GND	Common ground terminal.
15	GND	Common ground terminal.
16	IN2	Digital input from the motor controller.
17	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
18	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive circuit.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 42V, unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			12		V
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11		100		μA
ON						
R_{DS}	On resistance			0.3		Ω
$R_{DS\,(ON)}$	Drain source voltage	I_{DS} = 1.2 A Fig. 9		0.36		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 1.2A EN = L		0.9		V
t_{rr}	Reverse recovery time	I_F = 1.2A $\frac{dif}{dt}$ = 25A/μs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
$V_{IN\,L}$, $V_{EN\,L}$	Input Low voltage		-0.3		0.8	V
$V_{IN\,L}$, $V_{EN\,H}$	Input High voltage		2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low current	V_{IN}, V_{EN} = L			-10	μA
$I_{IN\,H}$, $I_{EN\,H}$	Input High current	V_{IN}, V_{EN} = H		30		μA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

Fig. 1 - Typical I_s normalized vs. T_j

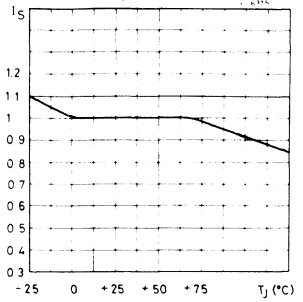


Fig. 2 - Quiescent current vs. frequency

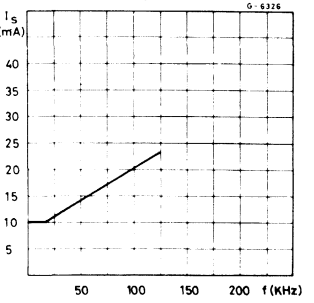


Fig. 3 - Typical I_s normalized vs. V_s

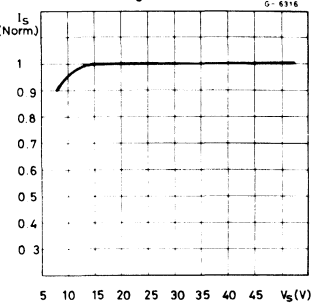


Fig. 4 - Typical diode behaviour in synchronous rectification

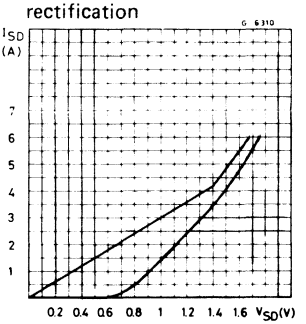


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

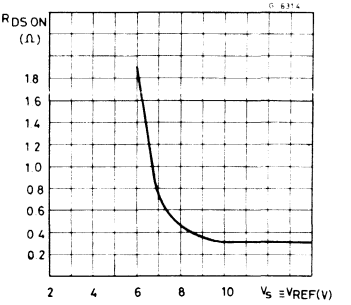


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

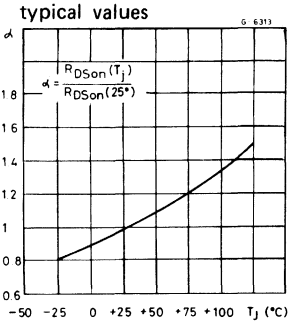


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

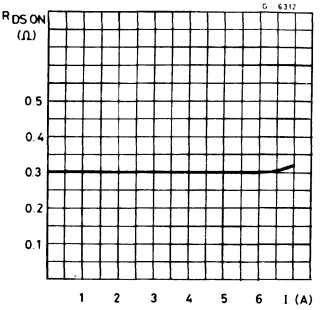


Fig. 8 - Typical power dissipation vs. I_L

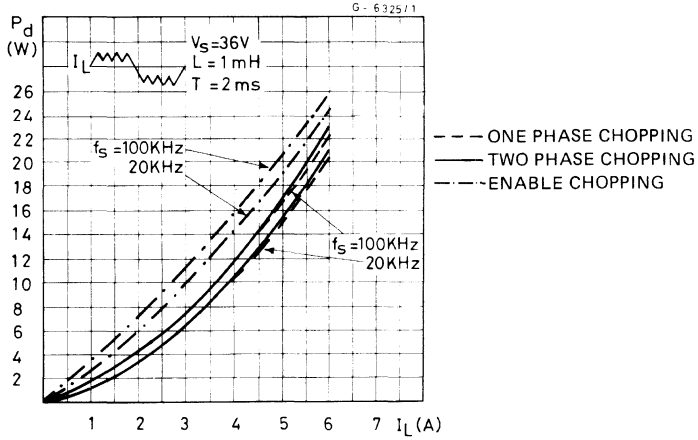


Fig. 8a - Two phase chopping

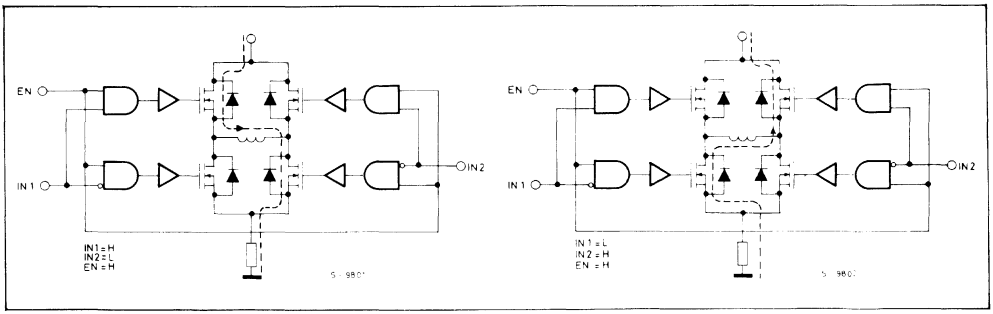


Fig. 8b - One phase chopping

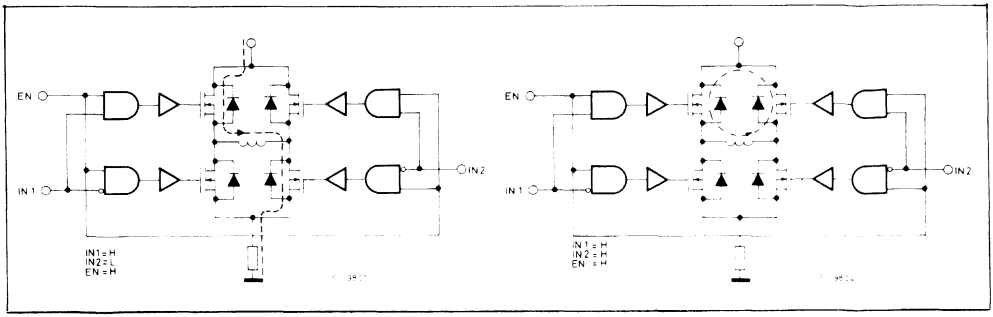
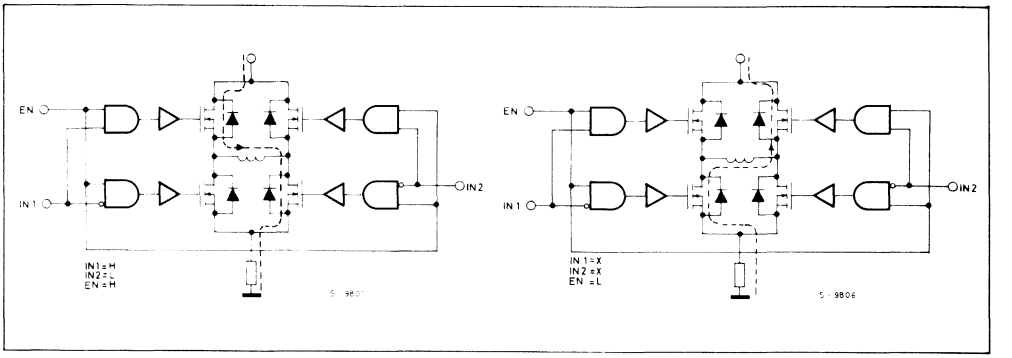


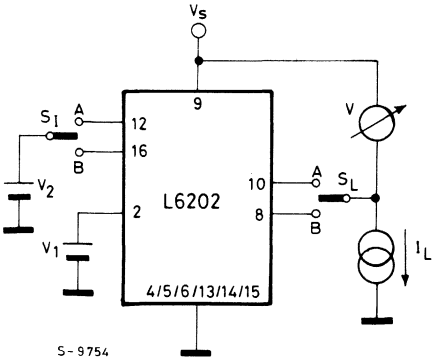
Fig. 8c - Enable chopping



TEST CIRCUITS

Fig. 9 - Saturation voltage

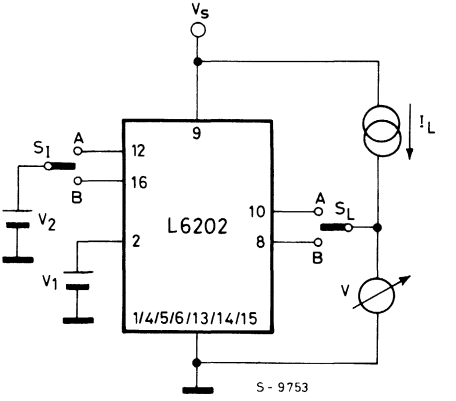
a) Source outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

b) Sink outputs



For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

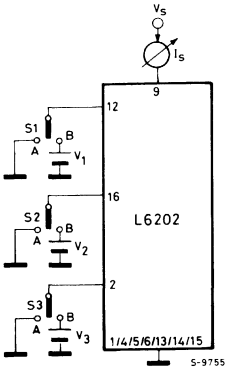
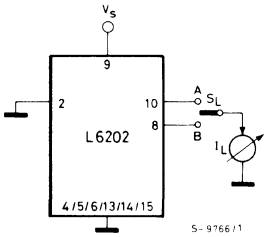
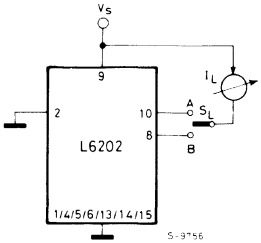


Fig. 11 - Leakage current

a) Source outputs



b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input or Enable chopper

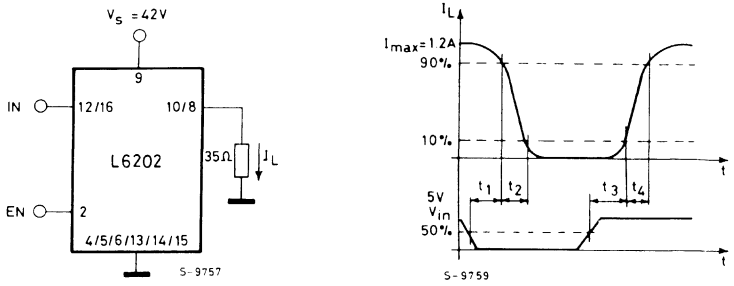
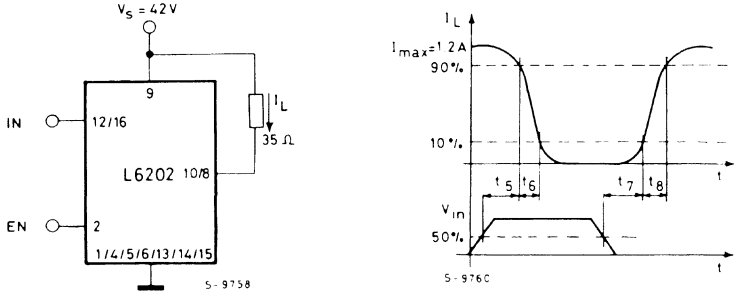


Fig. 13 - Sink current delay times vs. input or Enable chopper



CIRCUIT DESCRIPTION

The L6202 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned oFF

L = Low H = High X = Don't care

(*) Numbers referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER DMOS transistors

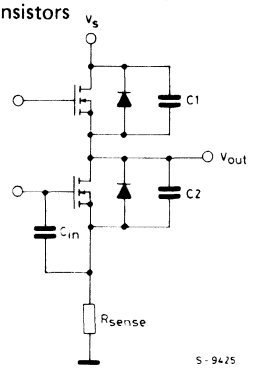
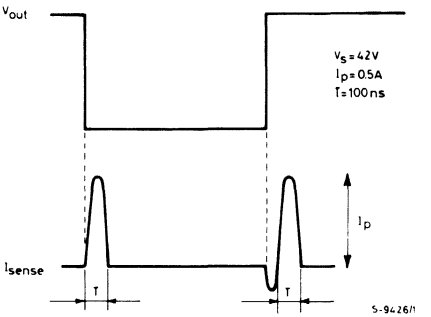


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6202 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\,(ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

If a 14V supply is available in the application it is possible to disable the voltage reference section and reduce even further the power dissipation. With 14V connected to the reference pin the bulk of the quiescent current can be supplied directly. Of course the power saving depends on the application, but for example at 36V at 20KHz a power saving of a least 240mW should be possible. This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6202 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\,(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN\text{-}ON} = T_{TURN\text{-}OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

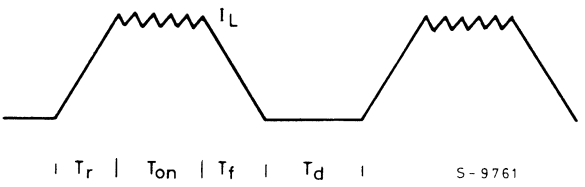
The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

Fig. 16

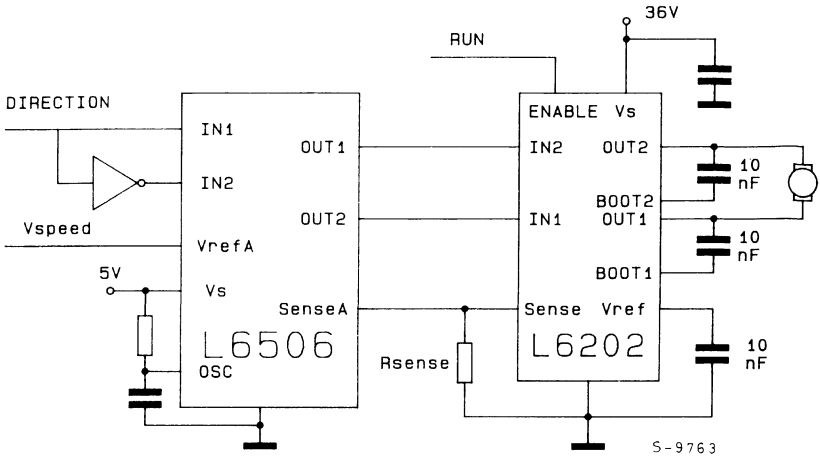


DC MOTOR SPEED CONTROL

Since the L6202 integrates a full H-Bridge in a single package it is idealy suited for controlling small DC motors. When used for DC motor control the L6202 provides the power stage required for both speed and direction control. The L6202 can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17. In this particular configuration only half of the L6506 is used and the other half of the device may be used to control a second motor.

In this configuration the L6506 sense the voltage across the sense resistor, R_{SENSE}, to monitor the motor current. The L6506 then compares the sensed voltage against the current control input and chops the input signals to the L6202 to control the motor current.

Fig. 17 - Bidirectional DC motor control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with an L297 or L6506, two L6202 bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface.

As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component requirements are minimal: an RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (pin 15 for L297, pin 10 and 15 for L6506). These solutions have a very high efficiency because of low power dissipation.

HIGH CURRENT MICROSTEP DRIVE FOR STEPPER MOTORS

The L6202 can by used in conjunction with the L6217 to (figure 20) implement a high current microstepping controller for stepper motors. In this application the L6217 is used as a control circuit and its outputs are used only to drive the inputs of the L6202. The application allows easy interface to a microprocessor since the L6217 may be connected directly to the microprocessor bus.

In the circuit shown in Figure 20, the L6217 senses the motor current by monitoring the voltage across the sense resistors, R_{SENSE}, and compares this value to the output of a 6 bit (7 bit if the L6217A is used) D to A Converter. The L6217 controls the current using a frequency modulated, constant off time, switching controller. The off time of each coil may be set using and external resistor and capacitor connected to PTA and PTB.

In this configuration the microprocessor simply loads the appropriate value for the direction of current flow through the coil and the data for the DAC into the L6217. The L6217 and L6202 then forms the complete interface between the micro and the motor.

Fig. 18 - Two phase Bipolar stepper motor control circuit with chopper current control

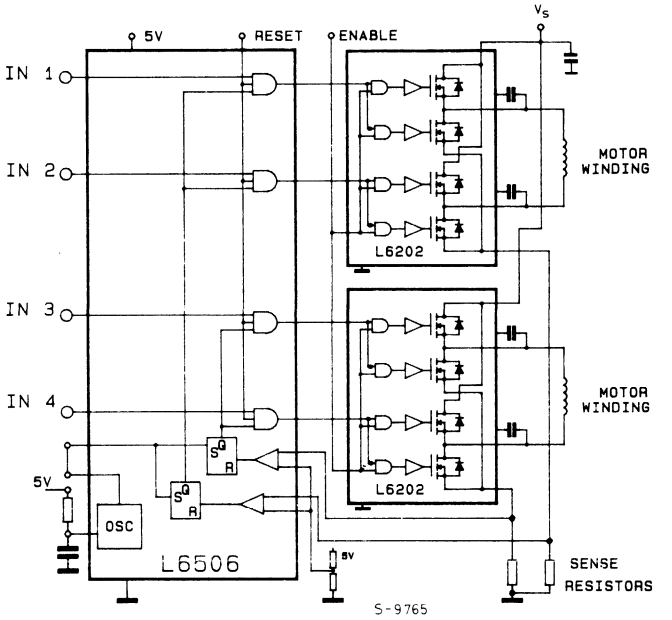


Fig. 19 - Two phase Bipolar stepper motor control circuit with chopper current control and translator

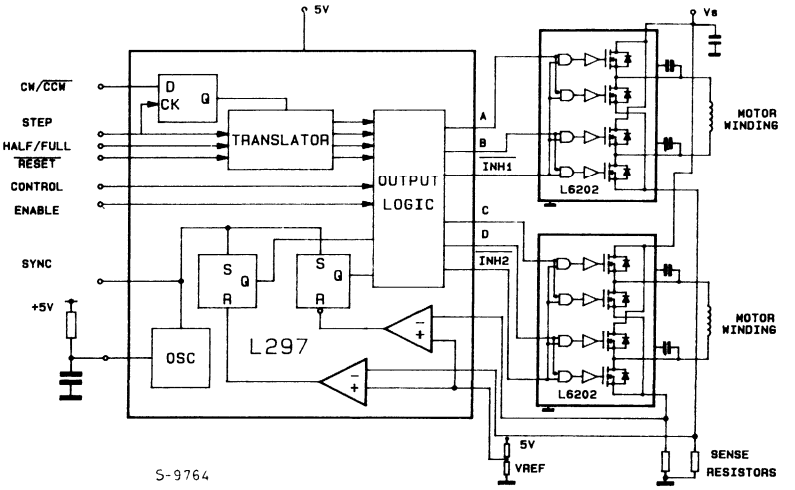
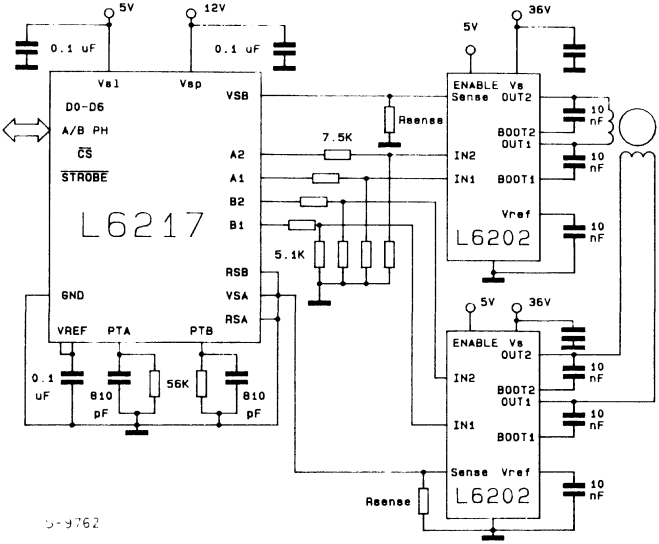


Fig. 20 - High current microstepping controller for stepper motors



THERMAL CHARACTERISTICS

Fig. 21 - R_{th} with two "on board" square heatsink vs. side ℓ

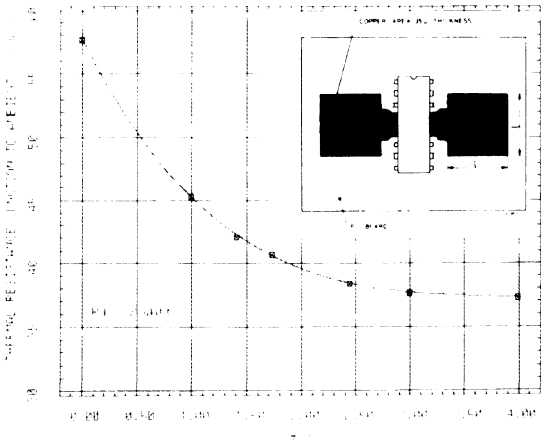


Fig. 22 - Transient thermal resistance for single pulses

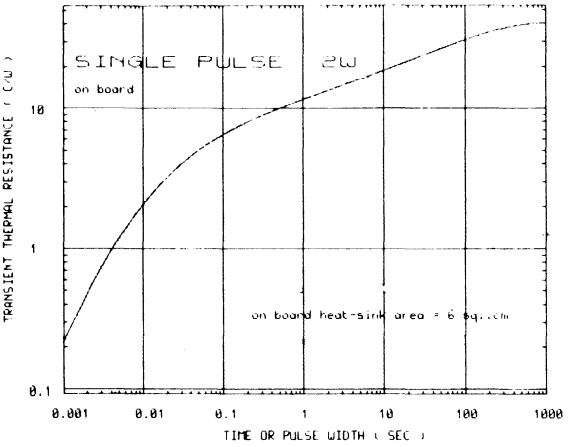
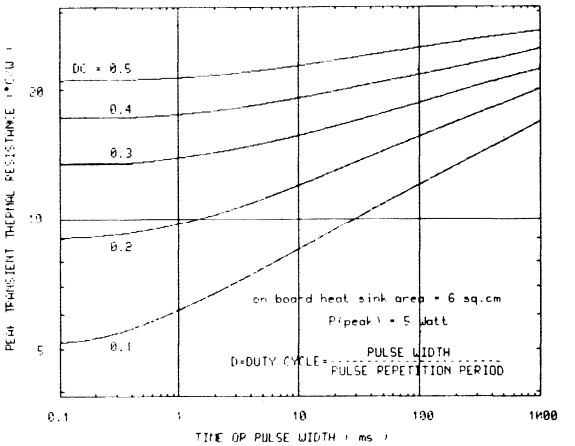


Fig. 23 - Peak transient R_{th} vs. pulse width and duty cycle



L6203

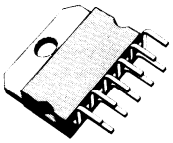
ADVANCE DATA

0.3Ω DMOS FULL BRIDGE DRIVER

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 4A
- $R_{DS\,(ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

The L6203 is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimise the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 4A RMS at motor supply voltages up to 48V and efficiently at high switch speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6203 is mounted in a 11-lead Multiwatt package.

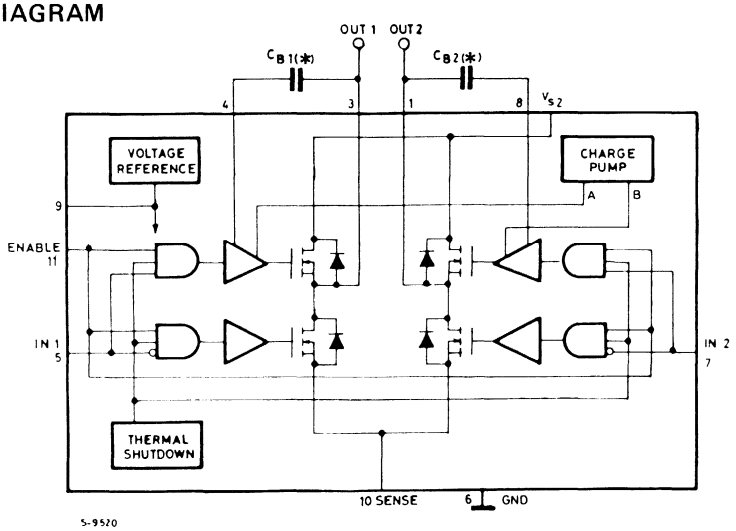
MultiPower BCD Technology



Multiwatt-11

ORDERING NUMBER: L6203

BLOCK DIAGRAM



(*) Suggested value for C_{BOOT1} and C_{BOOT2}: 10nF

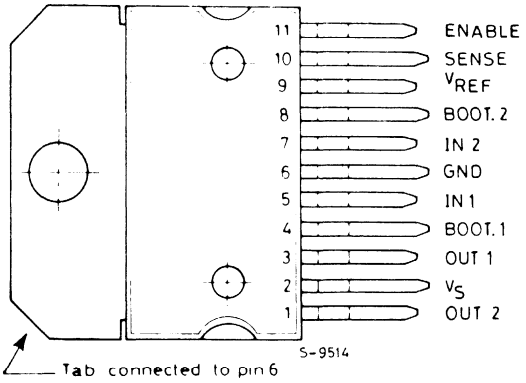
ABSOLUTE MAXIMUM RATINGS

V_s	Power supply (V_{EN} = Low)	60	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	Pulsed output current (note 1)	5	A
	- non repetitive (< 1ms)	10	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap supply	60	V
P_{tot}	Total power dissipation (T_{case} = 90°C)	20	W
	(T_{amb} = 70°C free air)	2.3	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM

(Top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	OUT2	Output of the half bridge.
2	V_s	Supply voltage.
3	OUT1	Output of the half bridge.
4	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
5	IN1	Digital input from the motor controller.
6	GND	Common ground terminal.
7	IN2	Digital input from the motor controller.
8	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
9	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive cricuit.
10	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control.
11	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 42V, unless otherwise stated)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			12		V
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11		100		μA
ON						
R_{DS}	On resistance			0.3		Ω
$V_{DS\ (ON)}$	Drain source voltage	I_{DS} = 3A		0.9		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 3A EN = L		1.35		V
t_{rr}	Reverse recovery time	I_F = 3A $\frac{dif}{dt}$ = 25A/μs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
$V_{IN\,L}$, $V_{EN\,L}$	Input Low voltage		-0.3		0.8	V
$V_{IN\,H}$, $V_{EN\,H}$	Input High voltage		2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low current	V_{IN}, V_{EN} = L			-10	μA
$I_{IN\,H}$, $I_{EN\,H}$	Input High current	V_{IN}, V_{EN} = H		30		μA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

Fig. 1 - Typical I_s normalized vs. T_j

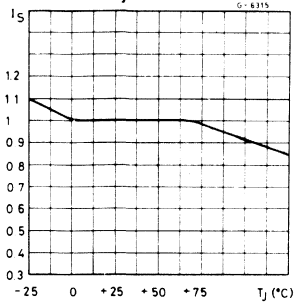


Fig. 2 - Quiescent current vs. frequency

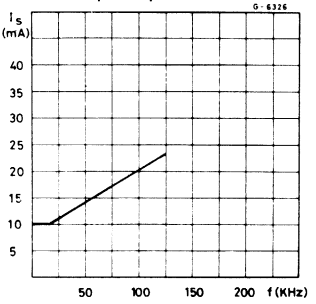


Fig. 3 - Typical I_s normalized vs. V_s

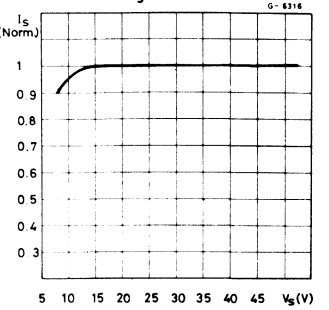


Fig. 4 - Typical diode behaviour in synchronous rectification

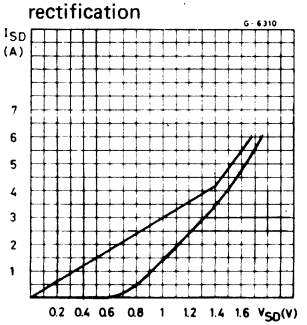


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

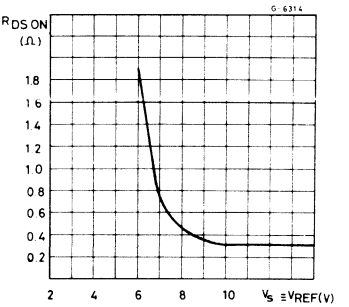


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

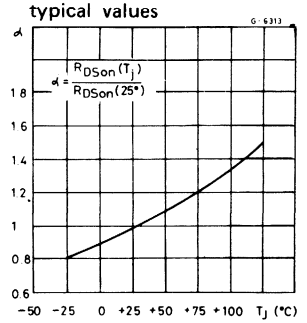


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

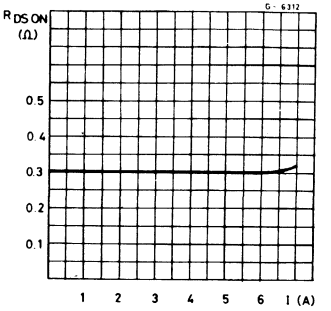


Fig. 8 - Typical power dissipation vs. I_L

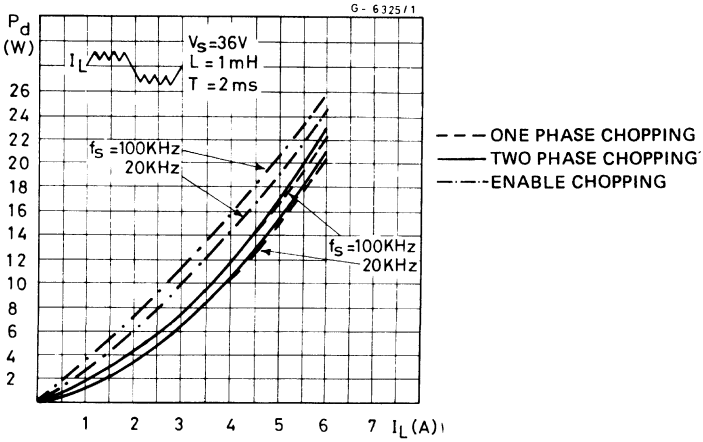


Fig. 8a - Two phase chopping

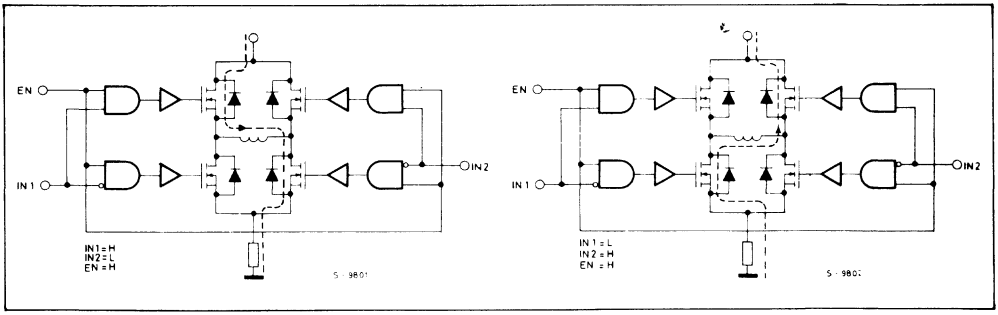


Fig. 8b - One phase chopping

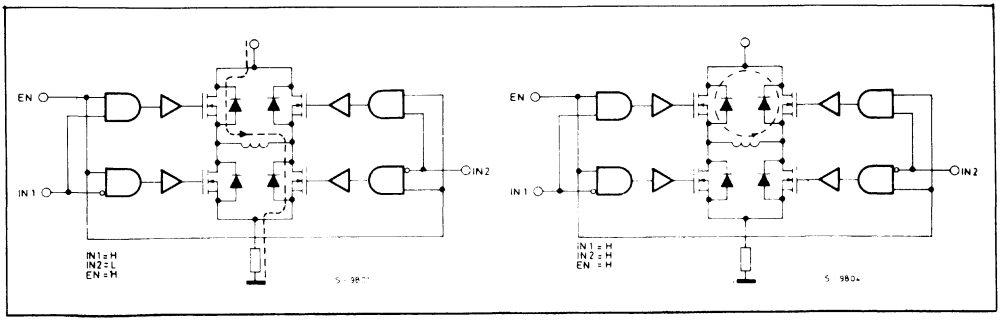
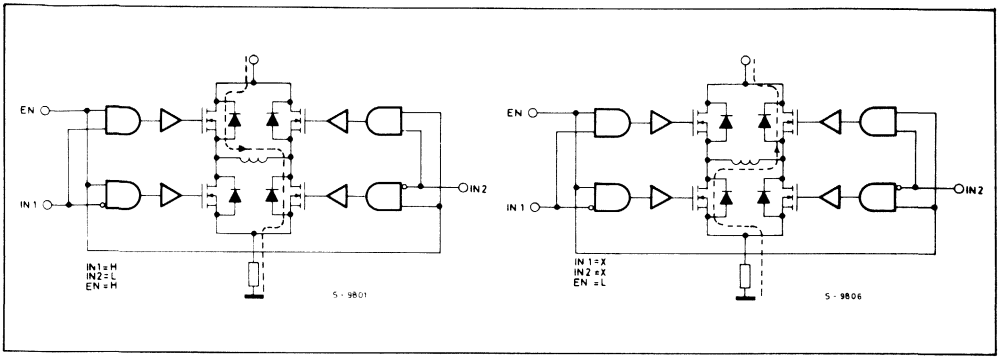


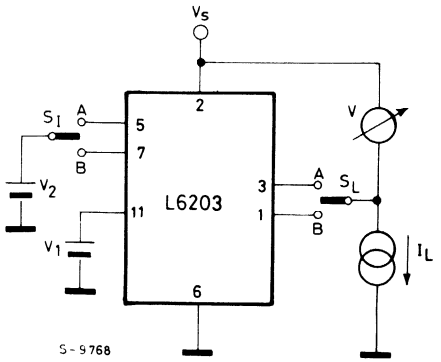
Fig. 8c - Enable chopping



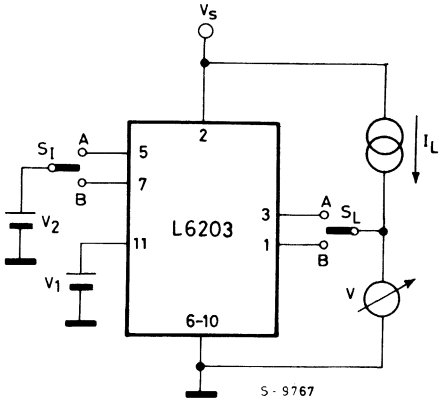
TEST CIRCUITS

Fig. 9 - Saturation voltage

a) Source outputs



b) Sink outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

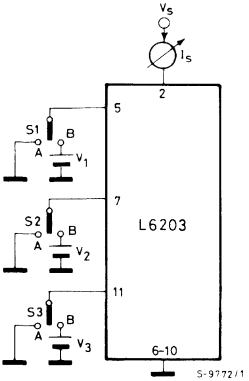
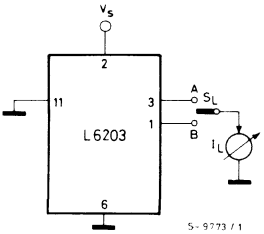
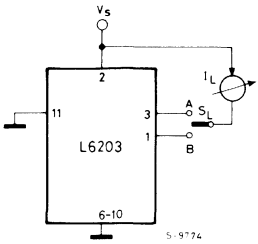


Fig. 11 - Leakage current

a) Source outputs

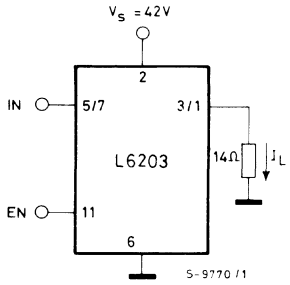


b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input or Enable chopper



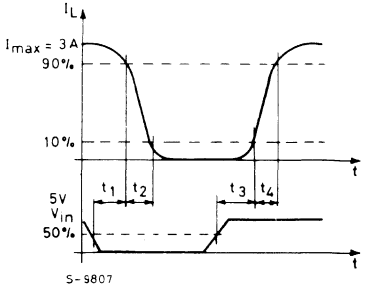
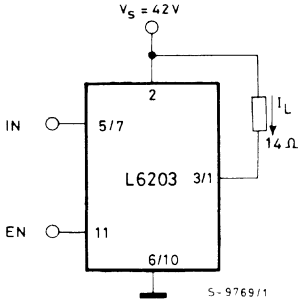
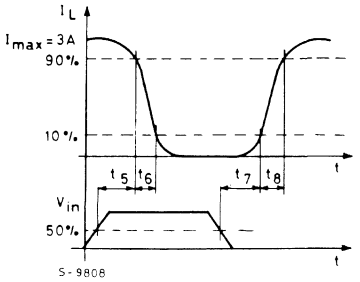


Fig. 13 - Sink current delay times vs. input or Enable chopper





CIRCUIT DESCRIPTION

The L6203 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned oFF

L = Low H = High X = Don't care

(*) Members referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER MOS transistors

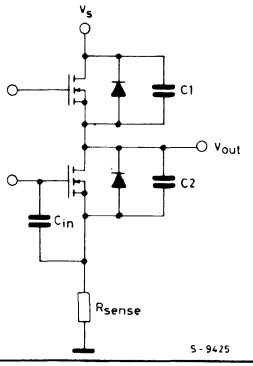
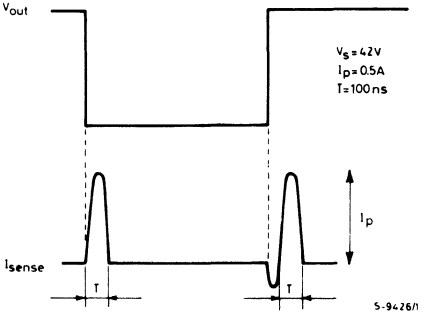


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6203 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\,(ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

If a 14V supply is available in the application it is possible to disable the voltage reference section and reduce even further the power dissipation. With 14V connected to the reference pin the bulk of the quiescent current can be supplied directly. Of course the power saving depends on the application, but for example at 36V at 20KHz a power saving of a least 240mW should be possible. This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6203 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\,(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN\text{-}ON} = T_{TURN\text{-}OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

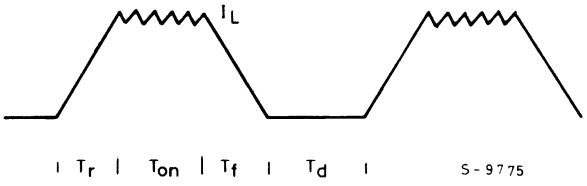
The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

Fig. 16

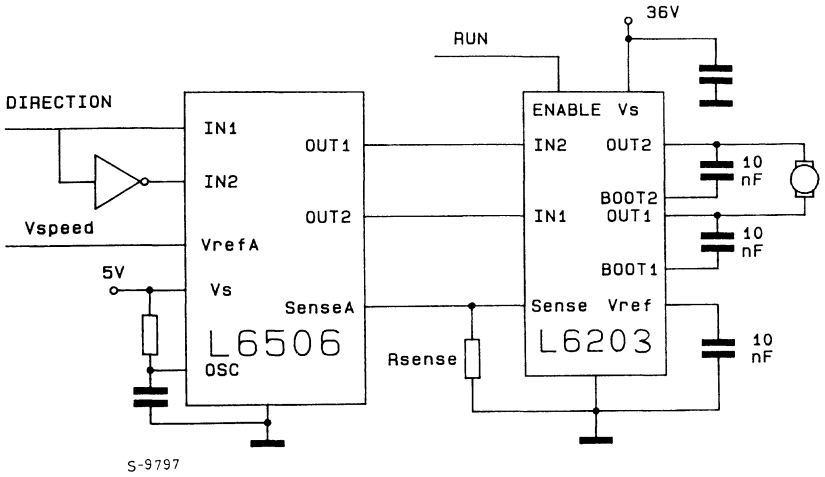


DC MOTOR SPEED CONTROL

Since the L6203 integrates a full H-Bridge in a single package it si idealy suited for controlling small DC motors. When used for DC motor control the L6203 provides the power stage required for both speed and direction control. The L6203 can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17. In this particular configuration only half of the L6506 is used and the other half of the device may be used to control a second motor.

In this configuration the L6506 sense the voltage across the sense resistor, R_{SENSE}, to monitor the motor current. The L6506 then compares the sensed voltage against the current control input and chops the input signals to the L6203 to control the motor current.

Fig. 17 - Bidirectional DC motor control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with an L297 or L6506, two L6203 bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface.

As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component requirements are minimal: an RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (pin 15 for L297, pin 10 and 15 for L6506). These solutions have a very high efficiency because of low power dissipation.

HIGH CURRENT MICROSTEP DRIVE FOR STEPPER MOTORS

The L6203 can by used in conjunction with the L6217 to (figure 20) implement a high current microstepping controller for stepper motors. In this application the L6217 is used as a control circuit and its outputs are used only to drive the inputs of the L6203. The application allows easy interface to a microprocessor since the L6217 may be connected directly to the microprocessor bus.

In the circuit shown in Figure 20, the L6217 senses the motor current by monitoring the voltage across the sense resistors, R_{SENSE}, and compares this value to the output of a 6 bit (7 bit if the L6217A is used) D to A Converter. The L6217 controls the current using a frequency modulated, constant off time, switching controller. The off time of each coil may be set using and external resistor and capacitor connected to PTA and PTB.

In this configuration the microprocessor simply loads the appropriate value for the direction of current flow through the coil and the data for the DAC into the L6217. The L6217 and L6203 then forms the complete interface between the micro and the motor.

Fig. 18 - Two phase Bipolar stepper motor control circuit with chopper current control

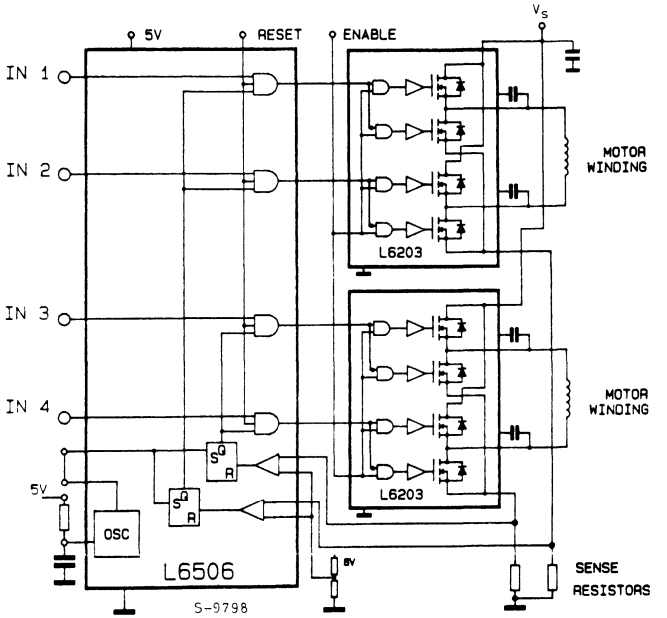


Fig. 19 - Two phase Bipolar stepper motor control circuit with chopper current control and translator

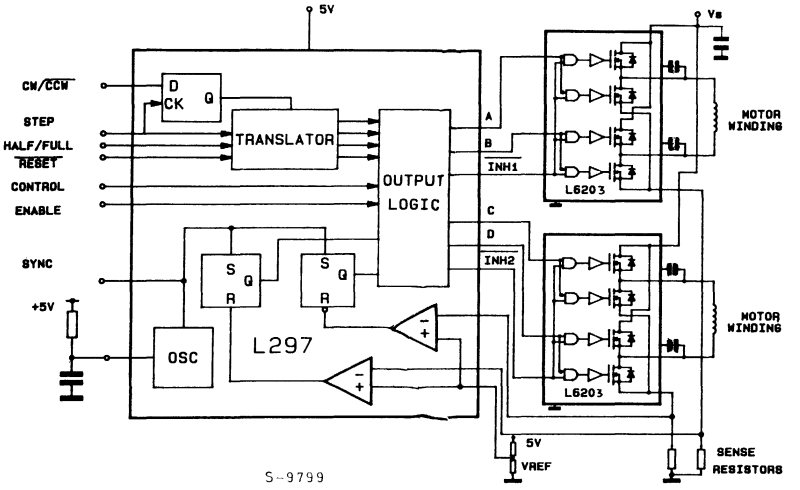
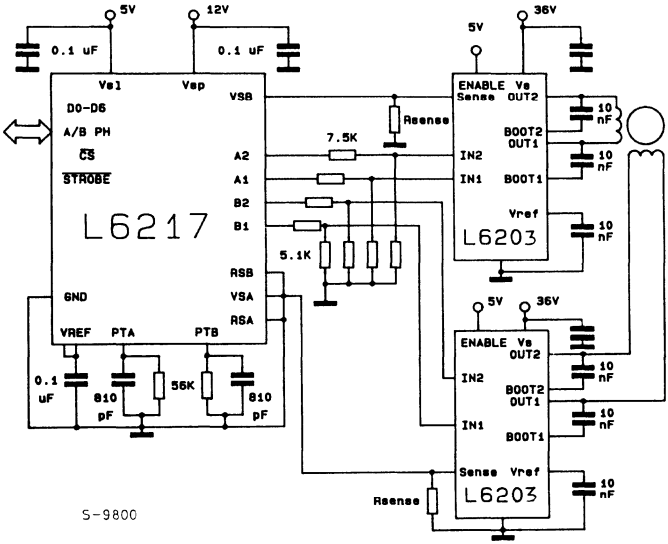


Fig. 20 - High current microstepping controller for stepper motors



THERMAL CHARACTERISTICS

Fig. 21 - $R_{th\ j\text{-}amb}$ of Multiwatt package vs. dissipated power

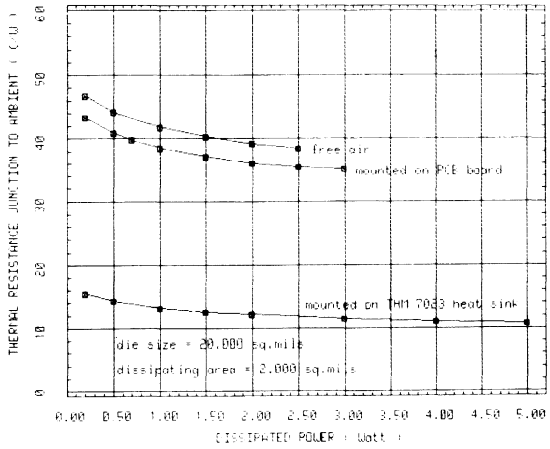
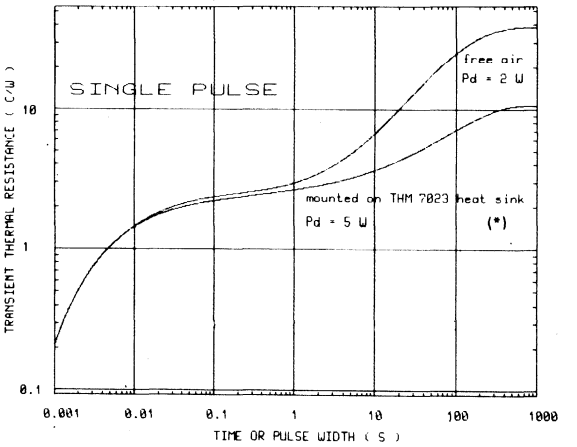
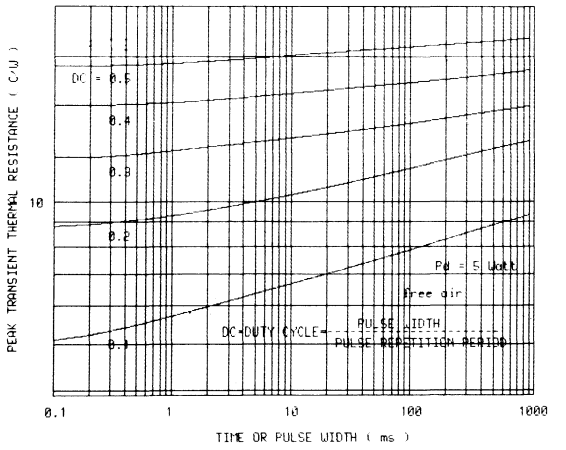


Fig. 22 - Comparison of transient R_{th} for single pulses with and without heatsink



(*) $R_{th} \cong 9°C/W$

Fig. 23 - Peak transient R_{th} vs. pulse width and duty cycle



ADVANCE DATA

DUAL SCHOTTKY DIODE BRIDGE

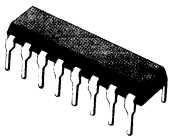
- MONOLITHIC ARRAY OF EIGHT SCHOTTKY DIODES
- HIGH EFFICIENCY
- 4A PEAK CURRENT
- LOW FORWARD VOLTAGE
- FAST RECOVERY TIME
- TWO SEPARATED DIODE BRIDGES

The L6210 is a monolithic IC containing eight Schottky diodes arranged as two separated diode bridges.

This diodes connection makes this device versatile in many applications.

They are used particular in bipolar stepper motor applications, where high efficient operation, due to low forward voltage drop and fast reverse recovery time, are required.

The L6210 is available in a 16 Pin Powerdip Package (12+2+2) designed for the 0 to 70°C ambient temperature range.



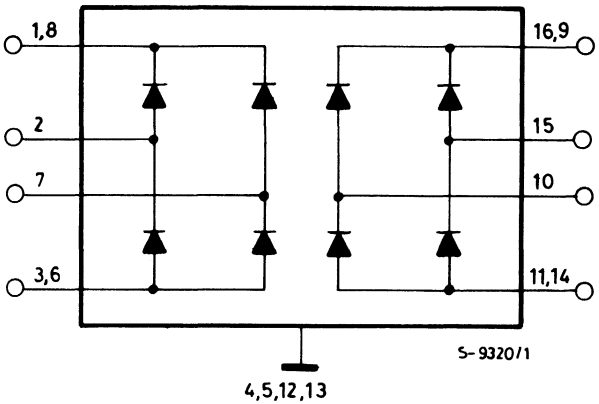
Powerdip 12+2+2

ORDERING NUMBER: L6210

ABSOLUTE MAXIMUM RATINGS

I_f	Repetitive forward current peak	2	A
V_r	Peak reverse voltage (per diode)	50	V
T_{amb}	Operating ambient temperature	70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

BLOCK DIAGRAM

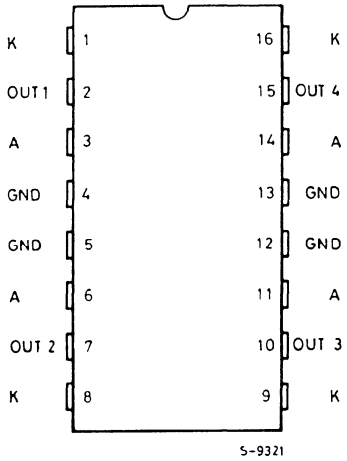


THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal impedance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal impedance junction-ambient without external heatsink	max	65	°C/W

CONNECTION DIAGRAM

(Top view)



ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Forward voltage drop	I_f = 500mA		0.8	1	V
		I_f = 1A		1	1.2	V
t_{rr}	Reverse recovery time	0.5A forward to 0.5A reverse		15	60	ns
t_{fr}	Forward recovery time	1A forward to 1.1V recovery		30	90	ns
I_L	Leakage current	V_R = 40V T_{amb} = 25°C			100	μA

NOTE: At forward currents of greater than 1A, a parasitic current of approximately 1mA may be collected by adiacent diodes.

Fig. 1 - Reverse current vs. voltage

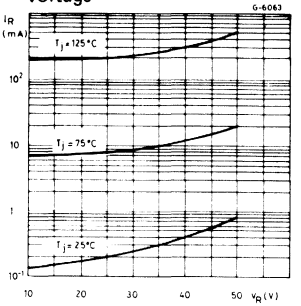
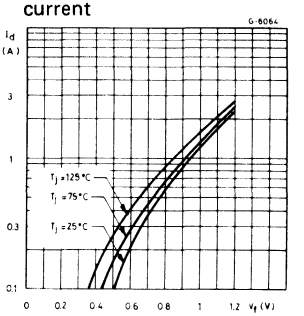


Fig. 2 - Forward voltage vs. current



MOUNTING INSTRUCTIONS

The $R_{th\,j\text{-}amb}$ of the L6210 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 3 or to an external heatsink (Figure 4).

During soldering the pin temperature must not exceed 260°C and the soldering time must not be longer then 12s. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 3 - Example of P.C. board copper area which is used as heatsink

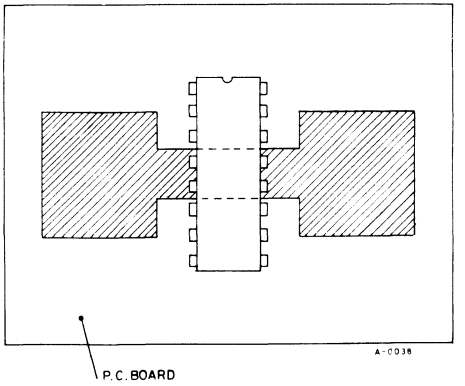
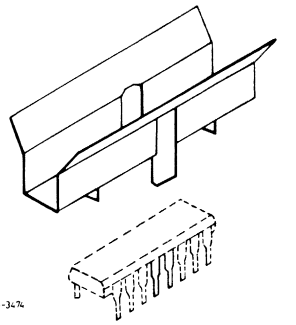


Fig. 4 - Example of an external heatsink



L6217

ADVANCE DATA

STEPPER MOTOR DRIVER

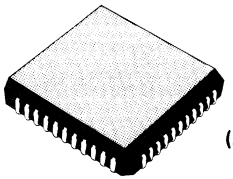
- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 6 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

The L6217 is a monolithic IC that controls and drives both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 6 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current recirculation. To maintain the degree of accuracy required for micro-stepping, the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by and RC network sets the motor current decay time.

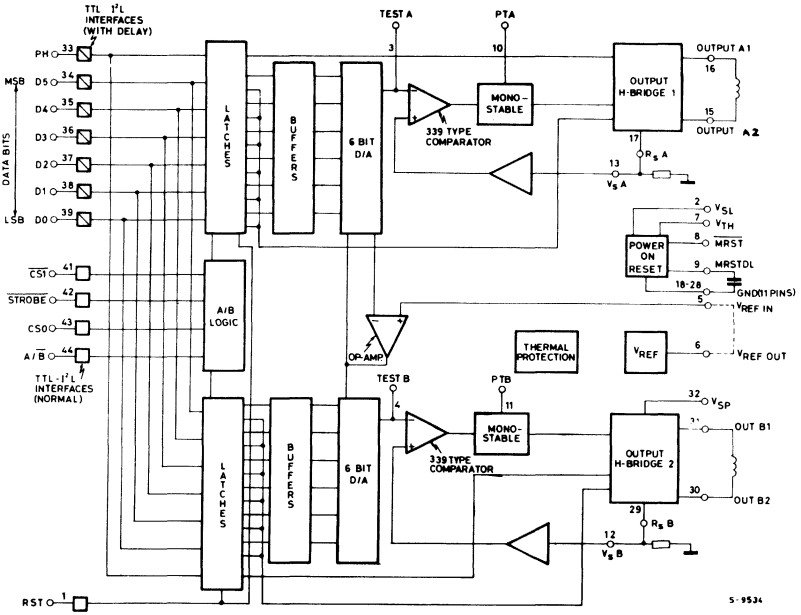
The L6217 is supplied in a 44 pin PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDERING NUMBER: L6217

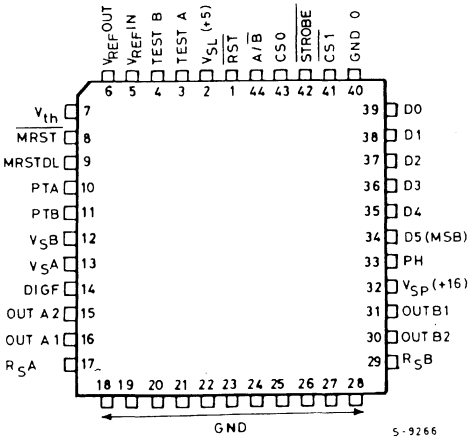
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{sl}	Logic supply voltage	7	V
V_{sp}	Motor supply voltage	18	V
V_I	Logic input voltage	6	V
V_{ref}	Reference input voltage	V_{sl}	V
I_o	Output peak current	500	mA
T_j	Operating junction temperature	150	°C
T_{stg}	Storage temperature	-55 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal impedance junction-case	max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal impedance junction-ambient	max	80	°C/W

PIN FUNCTION DESCRIPTION

N°	NAME	FUNCTION
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
38, 39	D0 - D5	Data inputs for the D/A converter. (D0 = LSB) For a data input of 00, the corresponding outputs are held in the off state.
44	A/B	Channel select for input data. Pin A/$\overline{B}$ selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{\text{Strobe}}$	Active low input latches input data (D0 - D5 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula: $t_d = (0.35)\ (C)\ 10^6$
8	$\overline{\text{MRST}}$	Power-on reset circuit output. (Micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P_tA	Pulse time A, an external parallel RC network tied to ground defines t_{off} time for channel A. (t_{off} = 0.69 R2C2).
11	P_tB	Pulse time B, an external parallel RC network tied to ground defines toll time for channel B. (t_{off} = 0.69 R3C3).
5	$V_{ref\ in}$	Voltage applied to this point sets the reference for the D/A converter and threfore sets the maximum output current. (See equation 1, next two pages).
18 to 28	Gnd	Ground connection and also conducts heat to the P.C. board.
40	Gnd 0	Pin must be connected to ground.
2	V_{sl}	Logic supply voltage
32	V_{sp}	Motor supply voltage

PIN FUNCTION DESCRIPTION (continued)

N°	NAME	FUNCTION
16, 15 31, 30	Out A1-A2 B1-B2	H-Bridge outputs.
43, 41	CS0, $\overline{CS1}$	Chip select inputs CS0 is active high, $\overline{CS1}$ is active low.
17, 29	R_sA - R_sB	Sense resistor from this pin to ground set the peak output current.
13, 12	V_sA - V_sB	Analog inputs for sensing motor current, Separate inputs are provides to allow filtering of the sense voltage if required.
3, 4	Test A & B	These pins are for testing of D/A outputs.
6	$V_{ref\ out}$	2.5V band gap reference.
7	V_{th}	Reset threshold voltage
14	DIGF	Can be used to modify the internal comparator lockout time. In the typical application this pin is left open.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_j = 25°C unless otherwise specified noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{sp}	Motor supply voltage		8		16	V
V_{sl}	Logic supply voltage		4.75		5.25	V
LOGIC INPUTS (D0 - D5, CS0, CS1, Reset and A/B)						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2		V_{sl}	V
I_{IL}	Input low current	V_I = 0.4V			-400	µA
I_{IH}	Input high current	V_I = 2.4V			10	µA
CURRENT CONTROL AND D TO A SECTION						
V_{ref}	Reference voltage	V_{CC} = 5.0V	2.45	2.50	2.55	V
V_{rin}	Reference input range		2.0		3.0	V
	Monotonicity of D to A		-0.5		+0.5	LSB
	Linearity of D to A		-1		+1	LSB
I_{op}	Peak Output Current (Gain of current loop)	V_{ref} = 2.40V R_{sense} = 2Ω Data = 3F (Hex)	225	252	277	mA
I_o	Output matching	V_{ref} = 2.40V			5	%

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
MONOSTABLE						
t_{off}	Cutoff time	R_t = 56KΩ C_t = 820pF	27		37	μs
t_d	Turn-off delay				2	μs
I_{off}	Output leakage current	Data = 00 (Hex)			100	μA
RESET CIRCUITRY						
V_{th}	Reset threshold voltage		3.9	4.1	4.3	V
	Reset threshold hysteresis		70	100		mV
I_{so}	Delay capacitor charging current	V_C = 2.5V	7	10	14	μA
I_{sl}	Delay capacitor discharge current	V_C = 2.5V	10			mA
V_{dth}	Delay threshold voltage		3.25	3.5	3.75	V
V_{dhys}	Hysteresis voltage on delay threshold		70	100		mV
I_{ol}	Output leakage current	V_O = 5V			200	μA
V_{sat}	Output saturation of reset out	I_O = 2mA			0.4	V
SOURCE DIODE-TRANSISTOR PAIRS						
V_{sat}	Saturation voltage	I_O = 400mA		1.3	1.8	V
V_f	Diode forward voltage	I_O = 400mA		0.8	1.2	V
SINK DIODE-TRANSISTOR PAIRS						
V_{sat}	Saturation voltage	I_O = 400mA		1.1	1.5	V
V_f	Diode Forward voltage	I_O = 400mA		0.6	1.0	V
AC CHARACTERISTICS						
t_s	Set-up time				100	ns
t_h	Hold time				500	ns
t_w	Minimum input pulse width				600	ns

CIRCUIT OPERATION

The current control section of the L6217 is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation:

$$I_{op} = \frac{V_{ref}}{4.69 \cdot R_{sense}} \cdot \frac{D}{64}$$

D = Input data (0 - 63)

When the input data is 00, the output stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_sA, R_sB) and the corresponding input (V_sA, V_sB), by disabling the comparator sensing during the lockout time. This time is typically 2.5ms.

Fig. 1 - Typical application

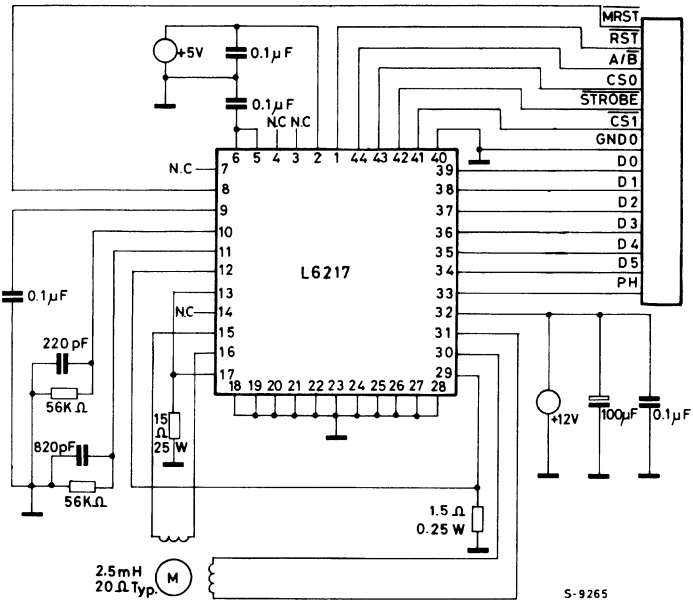


Fig. 2 - Microcomputer interface timing

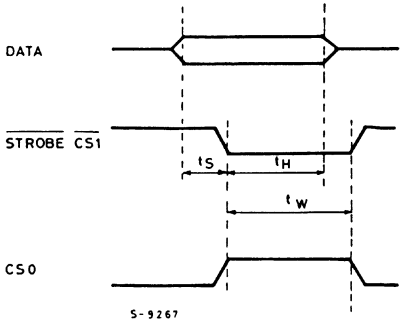


Fig. 3 - t_{off} DELAY

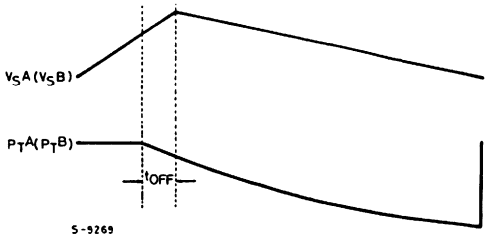


Fig. 4 - Motor current (half step mode)

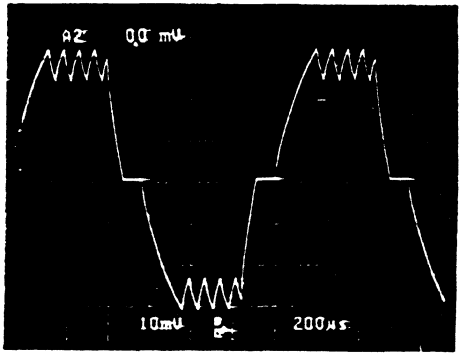


Fig. 5 - Monostable voltage and motor current repetitive steps.

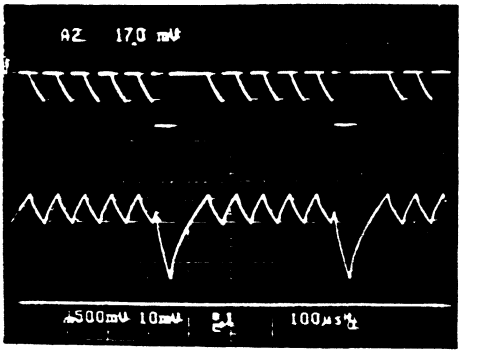
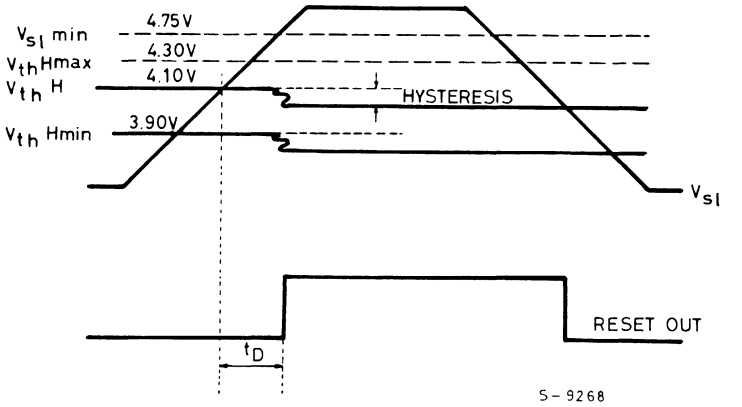


Fig. 6 - Reset waveforms



L6233

ADVANCE DATA

PHASE LOCKED FREQUENCY CONTROLLER

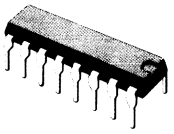
- PRECISION PHASE LOCKED FREQUENCY CONTROL SYSTEM
- XTAL OSCILLATOR
- PROGRAMMABLE REFERENCE FREQUENCY DIVIDERS
- PHASE DETECTOR WITH ABSOLUTE FREQUENCY STEERING
- DIGITAL LOCK INDICATOR
- DOUBLE EDGE OPTION ON THE FREQUENCY FEEDBACK SENSE AMPLIFIER
- TWO HIGH CURRENT OP-AMPS
- 5V REFERENCE OUTPUT

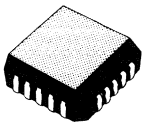
The L6233 is designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these device is universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuit compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error and a 5V reference output allows DC operating levels to be accurately set.



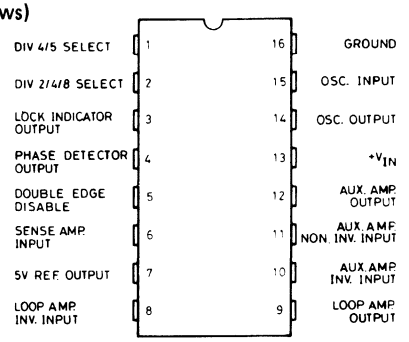


DIP-16 Plastic (0.25) **20 PLCC**

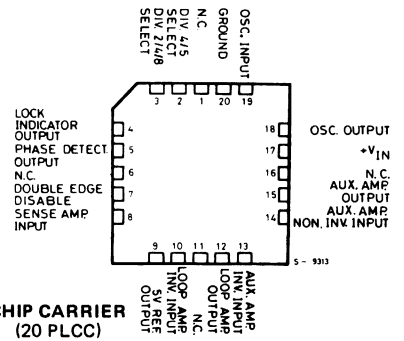
ORDERING NUMBERS: L6233 (DIP-16)
L6233P (20 PLCC)

CONNECTION DIAGRAMS

(Top views)



DIP-16



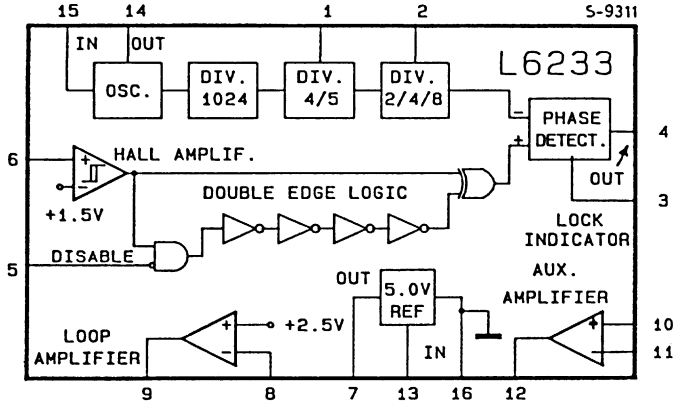
CHIP CARRIER (20 PLCC)

ABSOLUTE MAXIMUM RATINGS

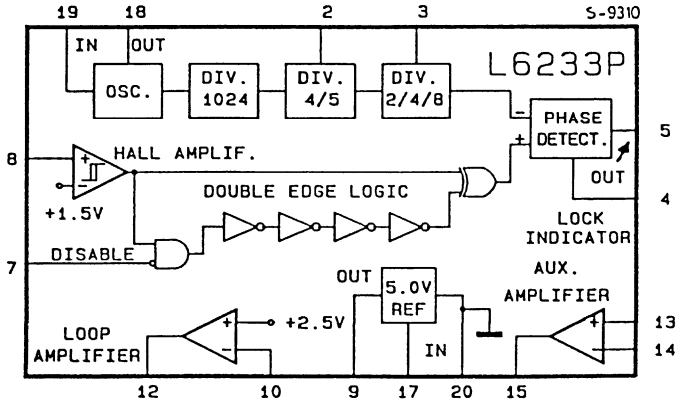
V_s	Supply voltage	14	V
P_{tot}	Power dissipation ($T_{amb} \leqslant 70°C$)	1	W
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

BLOCK DIAGRAMS

(DIP-16)



(PLCC PACKAGE)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_{amb} = 0°C to +70°C; $+V_{IN}$ = 12V)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply current			20		mA
REFERENCE						
V_{REF}	Output voltage		4.75	5.0	5.25	V
ΔV_{REF}	Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
ΔV_{REF}	Line regulation	$+V_{IN}$ = 8 to 12V		2.0	20	mV
I_{SC}	Short circuit current	V_{OUT} = 0V		35		mA
OSCILLATOR						
G_V	DC voltage gain	Oscillator input to oscillator output		16		dB
V_{IB}	Input DC level	Oscillator input pin open, T_j = 25°C		1.3		V
Z_{IN} *	Input impedance	$V_{IN} = V_{IB} \pm 0.5V$, T_j = 25°C		1.6		KΩ
V_o	Output DC level	Oscillator input pin open T_j = 25°C		1.4		V
f_{oMAX}	Maximum operating frequency		10			MHz
DIVIDERS						
f_{oMAX}	Maximum input frequency	Input = $1V_{PP}$ at oscillator input	10			MHz
	Div. 4/5 input current	Input = 5V (Div. by 4)		150	500	μA
		Input = 0V (Div. by 5)	-5.0	0.0	5.0	μA
V_{TH}	Div. 4/5 threshold		0.5	1.6	2.2	V
	Div. 2/4/8 input current	Input = 5V (Div. by 8)		150	500	μA
		Input = 0V (Div. by 2)	-500	-150		μA
	Div. 2/4/8 open circuit voltage	Input current = 0μA (Div. by 4)	1.5	2.5	3.5	V
	Div. by 2 threshold		0.35	0.8		V
	Div. by 4 threshold		1.5		3.5	V
	Div. by 8 threshold	Volts below V_{REF}	0.35	0.8		V
SENSE AMPLIFIER						
V_T	Threshold voltage	Percent of V_{REF}		30		%
H_T	Threshold hysteresis			10		mV
I_b	Input bias current	Input = 1.5V		-0.2		μA
DOUBLE EDGE DISABLE INPUT						
V_I	Input current	Input = 5V (Disabled)		150	500	μA
		Input = 0V (Enabled)	-5.0	0.0	5.0	μA
V_T	Threshold voltage		0.5	1.6	2.2	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
PHASE DETECTOR						
V_{OH}	High output level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
V_{OL}	Low output level	Negative Phase/Freq. Error		0.2	0.5	V
V_{OM}	Mid output level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
	High level maximum source current	V_{OUT} = 4.3V	2.0	8.0		mA
	Low level maximum sink curr.	V_{OUT} = 0.7V	2.0	5.0		mA
	Mid level output impedance (Note 2)	I_{OUT} = -200 to +200μA T_j = 25°C		6.0		KΩ
LOCK INDICATOR OUTPUT						
V_{sat}	Saturation voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
	Leakage current	Zero Freq. Error V_{OUT} = 12V		0.1	1.0	μA
LOOP AMPLIFIER						
	NON INV. reference voltage	Percent of V_{REF}	47	50	53	%
I_b	Input bias current	Input = 2.5V	-0.8	-0.2		μA
G_v	Open loop gain		60	75		dB
SVR	Supply voltage rejection	+V_{IN} = 8 to 12V	70	100		dB
I_{SH}	Short circuit current	Source, V_{OUT} = 0V	16	35		mA
		Sink, V_{OUT} = 5V	16	30		mA
AUXILIARY OP-AMP						
V_{OS}	Input offset voltage	V_{CM} = 2.5V			8	mV
I_b	Input bias current	V_{CM} = 2.5V		200		mA
I_{os}	Input offset current	V_{CM} = 2.5V		10		mA
G_v	Open loop gain		70	120		dB
SVR	Supply voltage rejection	+V_{IN} = 8 to 12V	70	100		dB
CMR	Common mode rejection	V_{CM} = 0 to 10V	70	100		dB
I_{SH}	Short circuit current	Source, V_{OUT} = 0V		35		mA
		Sink, V_{OUT} = 5V		30		mA

* These impedance levels will vary with T_j at about 1700ppm/°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

APPLICATION INFORMATION

Determining the Oscillator Frequency

The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

$$f_{osc}(Hz) = (\text{Divide Ratio}) \cdot (\text{Motor RPM}) \cdot (1/60\ \text{SEC/MIN}) \cdot (\text{No. of Rotor Poles}/2) \cdot (\times 2 \text{ if Pin 5 Low})$$

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

Fig. 1 - Recommended Oscillator Configuration Using AT Cut Quartz XTAL

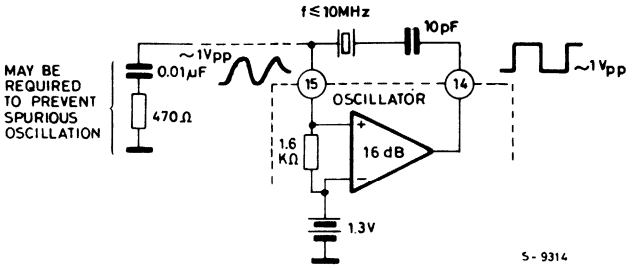


Fig. 2 - External Reference Frequency Input

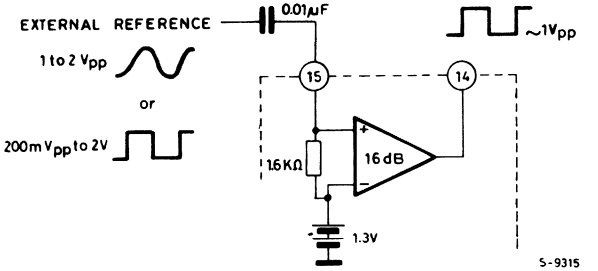
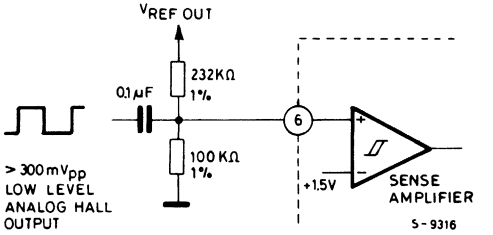


Fig. 3 - Method for Deriving Rotation Feedback Signal From Analog Hall Effect Device



* This signal may require filtering if chopped mode drive scheme is used.

APPLICATION INFORMATION (continued)

Phase detector operation

The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low, the middle state output impedance is high, tipically 6.0KΩ. When there is any static frequency difference between the inputs the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level the remainder of the period. If the phase relationship is reversed then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector, $K\phi$, is $5V/4\pi$, radians, or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic and the connecting arrows the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge on the-input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from a frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6 or 7.

Fig. 4 - Typical Phase Detector Output Waveforms

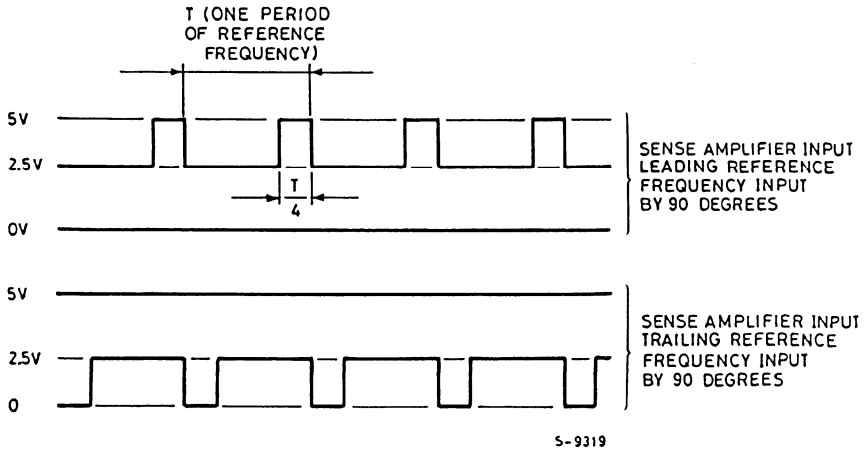


Fig. 5 - Phase Detector State Diagram

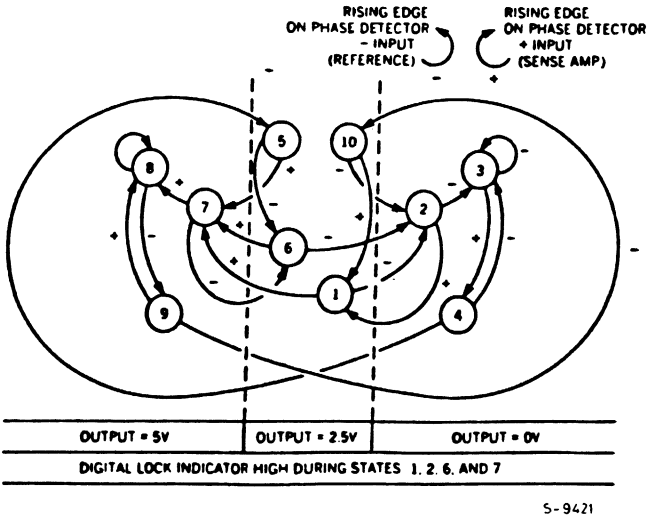
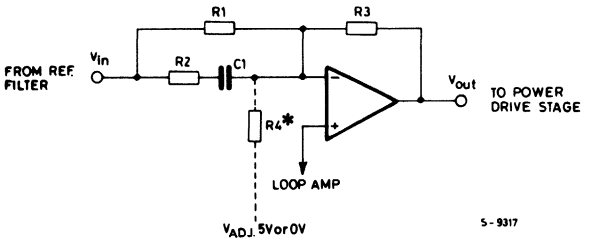


Fig. 6 - Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{R3}{R1} \cdot \frac{1 + S/\omega Z}{1 + S/\omega P}$$

$$\omega P = \frac{1}{R2\,C1}$$

$$\omega Z = \frac{1}{(R1 + R2)\,C1}$$

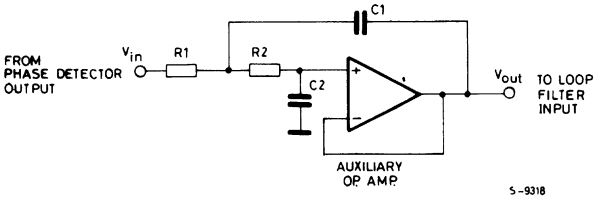
* The statistic phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by:

$$R4 = \frac{2.5V \cdot R3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

$(V_{OUT} - 2.5) > 0$ R4 Goes to 0V
$(V_{OUT} - 2.5) < 0$ R4 Goes to 5.0V

Fig. 7 - Reference Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{1}{1 + \frac{S2}{\omega N} + \frac{S^2}{\omega N^2}}$$

$$\omega N = \frac{1}{\sqrt{R1\,R2\,C1\,C2}}$$

$$\delta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C2}{C1}}\quad\frac{R1 + R2}{\sqrt{R1\,R2}}$$

Note: with R1 = R2 $\quad \delta = \sqrt{\frac{C2}{C1}}$

Fig. 8 - Reference Filter Design Aid - Gain Response

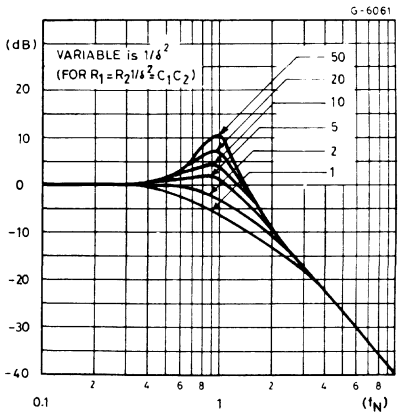
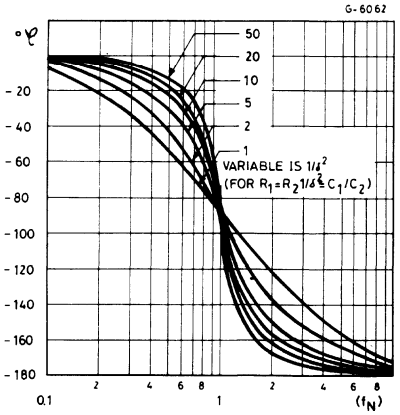


Fig. 9 - Reference Filter Design Aid - Phase Response



L6235

ADVANCE DATA

R-DAT BRUSHLESS DC MOTOR DRIVER

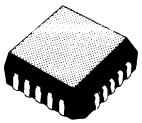
- 400mA OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- INHIBIT FUNCTION
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

The L6235 is single-chip driver for three-phase brushless DC motors capable of delivering 400mA output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase drive.

To limit EMI emission the L6235 controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL system, may be used with the L6235 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

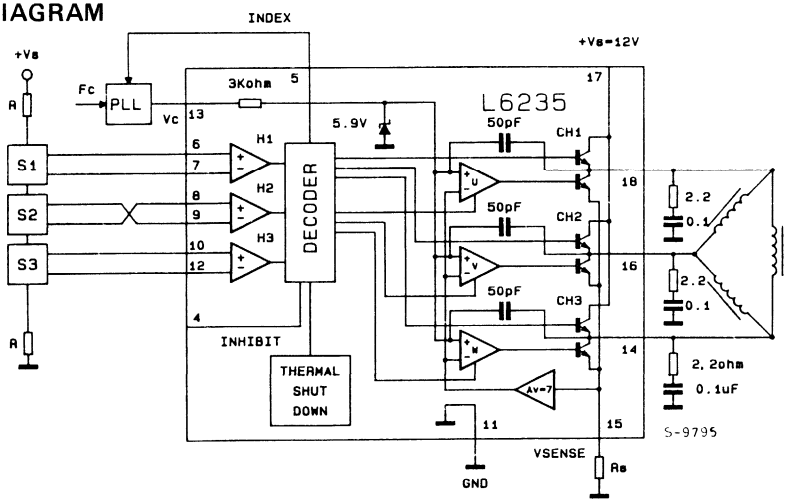
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



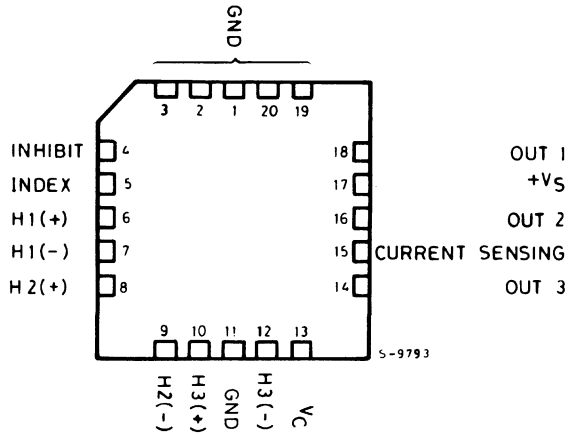
PLCC (15+5)

ORDERING NUMBER: L6235

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	18	V
I_o	Peak output current each channel		
	– non repetitive (100μs)	1.5	A
	– repetitive (80% on - 20% off; t_{on} = 10ms)	500	mA
	– DC operation	400	mA
V_i	Logic and analogic inputs	$+V_s$	
P_{tot}	Total power dissipation at T_{pins} = 50°C	5	W
T_{op}	Operating temperature range	0 to 70	°C
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W
R_{tt}	Transient thermal resistance (t = 2sec.)	max	30	°C/W

PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
4	INHIBIT	I	Output stage inhibit. When this pin is high all three output stages are in a high impedance state!
5	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
6	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
7	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
8	H2 (+)	I	Same as pin 3 for channel 2.
9	H2 (-)	I	Same as pin 4 for channel 2.
10	H3 (+)	I	Same as pin 3 for channel 3.
11	GND		Ground connection.
12	H3 (-)	I	Same as pin 4 for channel 3.
13	V_C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
14	Out 3	O	Output motor drive for phase 3.
15	Sense	I	Current Sensing. Input for load current sense voltage for output stage.
16	Out 2	O	Output motor drive for phase 2.
17	V_S		Motor supply voltage.
18	Out 1	O	Output motor drive for phase 1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_s = 12V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		10	12		V
I_s	Quiescent supply current	Without Load		30	60	mA
HALL AMPLIFIERS						
V_{CM}	Common mode voltage range		0		10	V
V_{io}	Input offset voltage	V_i = 6V		2	10	mV
I_{ib}	Input bias current	V_i = 6V		2	10	μA
I_{io}	Input offset current	V_i = 6V		0.1		μA
SPEED CONTROL INPUT (V_C)						
V_i	Input voltage range		0		5	V
I_{ib}	Input bias current	$V_C < V_{sens}$		1	5	μA
V_{ic}	Input clamping voltage			5.9		V
INHIBIT INPUT						
V_{IH}	Input high voltage		2		V_s	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current				10	μA
I_{IL}	Input low current			-5	-50	μA
HALL LOGIC OUTPUT						
V_{LO}	Low output voltage	I = 5mA			0.8	V
I_L	Leakage current	V_{CE} = 12V			10	μA
OUTPUT POWER STAGE						
V_{sat}	Total saturation voltage	I_o = 0.15A I_o = 0.4A I_o = 1.0A		2.2 2.5 2.7		V
V_{OSR}	Output voltage slew-rate			100		V/ms
V_{sens}	Sense voltage range		0		0.7	V
THERMAL SHUTDOWN						
T_j	Junction temperature		150			°C
T_H	Hysteresis				30	°C

DESCRIPTION

The L6235 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase drive. When the INHIBIT INPUT is high all three OUTPUTS ARE PLACED in a high - IMPEDANCE STATE.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth table of Fig. 1.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input of the device at pin 10, V_C.

In addition, a 1V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s, senses the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = \frac{(V_C - 1)}{7\ R_s}$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1)/(7\ I_{max})$$

where V_X is the full scale voltage of V_C.

In this way the V_C/I_{out} characteristics can be modified. Note that V_X max is clamped at 5.9V.

The most important feature of the L6235 is slew rate control. With this device a typical value of 0.1V/μs is achieved, reducing EMI to a very low value.

Another key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the free-wheeling diodes in the acceleration phase and through the motor is steady-state conditions. Torque ripple is also minimized.

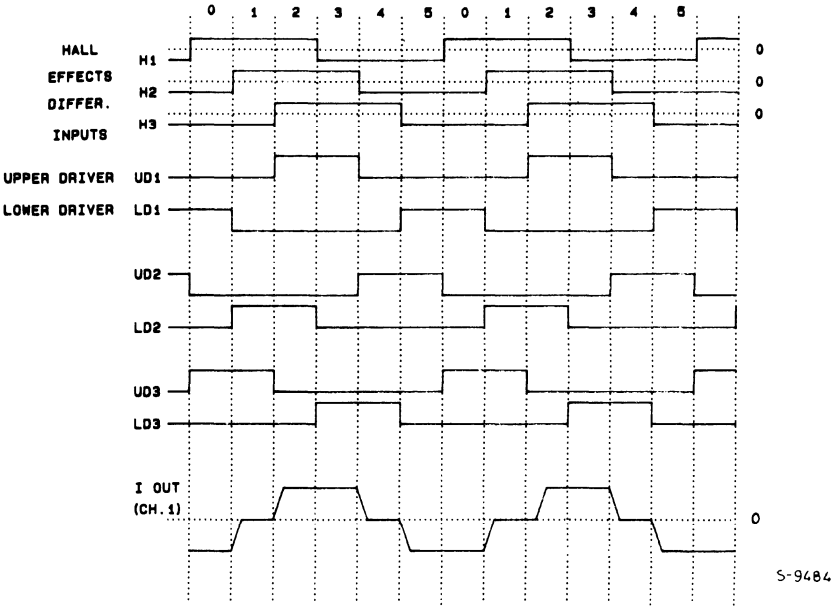
The L6235 can also operate with a brushless motor connected in a star configuration, leaving the centre floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - TRUTH TABLE

HALL EFFECT DIFF. INPUT			UPPER DRIVER STATUS			LOWER DRIVER STATUS		
1 = POSITIVE 0 = NEGATIVE			1 = ON 0 = OFF			1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	0	0	1	1	0	0
1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	0	1	0
0	1	1	1	0	0	0	0	1
0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	0	0

Fig. 2 - Timing diagram

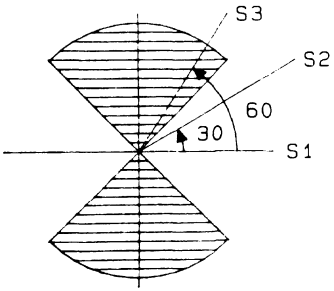


DETERMINING HALL EFFECT SENSOR CODING

The L6335 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 2, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6235. Note that the rotation in fig. 3 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 3 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6235 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 3



For example, let us examine the output pattern of a different type of motor (fig. 4). Assuming 90 windows at 180 intervals, then with respect to fig. 3, a similar diagram, fig. 5, results in sensors 60 apart with the windows rotating clockwise. The situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 5, this should be used for the L6235 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6235 must go high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6235.

Fig. 4

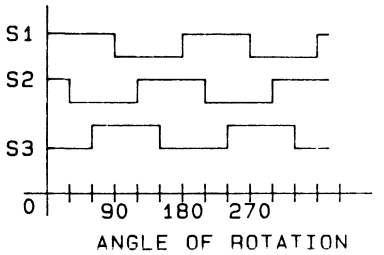
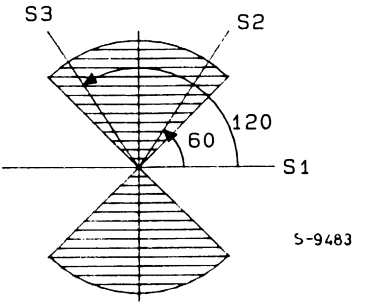


Fig. 5

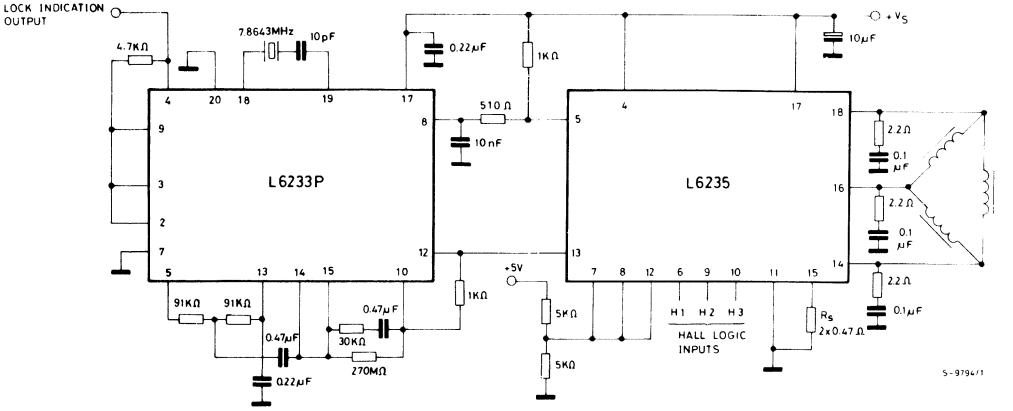


Thus the conversion table for this particular motor is:

Motor Sensors	L6235 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6235. Since the L6235 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

Fig. 6 - Application circuit using the L6233 PLL-Controller



L6236

ADVANCE DATA

BIDIRECTIONAL R-DAT BRUSHLESS DC MOTOR DRIVER

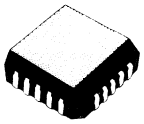
- 400mA OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

The L6236 is a single-chip driver for three-phase brushless DC motors capable of delivering 400mA output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase bidirectional drive. Both delta and wye configurations may be used.

To limit EMI esmission the L6236 operates in a linear mode and controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6236 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

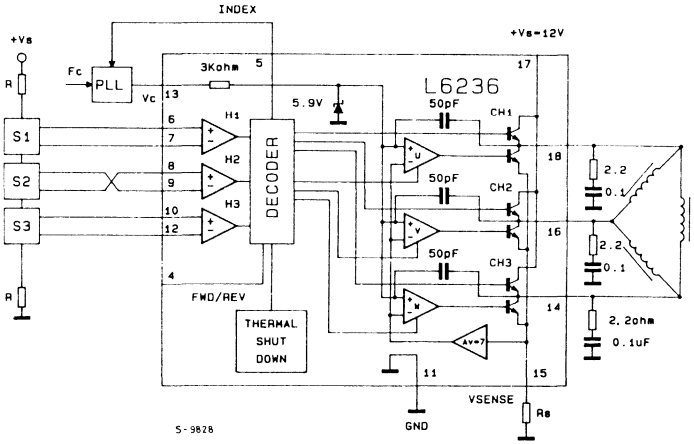
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



PLCC (15 + 5)

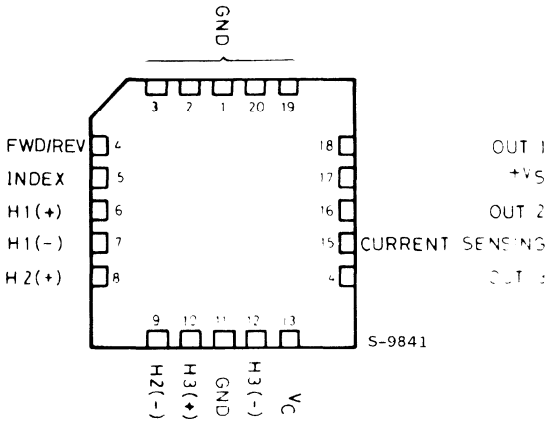
ORDERING NUMBER: L6236

BLOCK DIAGRAM



L6236

CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	18	V
I_o	Peak output current each channel		
	– non repetitive (100μs)	1.5	A
	– repetitive (80% on - 20% off; t_{on} = 10ms)	500	mA
	– DC operation	400	mA
V_i	Logic and analogic inputs	$+V_s$	
P_{tot}	Total power dissipation at T_{pins} = 50°C	5	W
T_{op}	Operating temperature range	0 to 70	°C
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W
R_{tt}	Transient thermal resistance (t = 2sec.)	max	30	°C/W

PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
4	FWD/REV	I	Direction Control. When this pin is low, the motor will run in the forward direction. A high will drive the motor in the reverse direction. Direction is defined by the positive of the sensors in the motor.
5	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
6	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
7	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
8	H2 (+)	I	Same as pin 3 for channel 2.
9	H2 (-)	I	Same as pin 4 for channel 2.
10	H3 (+)	I	Same as pin 3 for channel 3.
11	GND		Ground connection.
12	H3 (-)	I	Same as pin 4 for channel 3.
13	V_C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
14	OUT3	O	Output motor drive for phase 3.
15	SENSE	I	Current Sensing. Input for load current sense voltage for output stage.
16	OUT2	O	Output motor drive for phase 2.
17	V_S		Motor supply voltage.
18	OUT1	O	Output motor drive for phase 1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_s = 12V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		10	12		V
I_s	Quiescent supply current			30	60	mA
HALL AMPLIFIERS						
V_{CM}	Common mode voltage range		0		10	V
V_{io}	Input offset voltage	V_i = 6V		2	10	mV
I_{ib}	Input bias current	V_i = 6V		2	10	μA
I_{io}	Input offset current	V_i = 6V		0.1		μA
SPEED CONTROL INPUT (V_C)						
V_i	Input voltage range		0		5	V
I_{ib}	Input bias current	$V_C < V_{sens}$		1	5	μA
V_{ic}	Input clamping voltage			5.9		V
FWD/REVERSE INPUT						
V_{IH}	Input high voltage		2		V_s	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current				10	μA
I_{IL}	Input low current			-5	-50	μA
HALL LOGIC OUTPUT						
V_{LO}	Low output voltage	I = 5mA			0.8	V
I_L	Leakage current	V_{CE} = 12V			10	μA
OUTPUT POWER STAGE						
V_{sat}	Total saturation voltage	I_o = 0.15A I_o = 0.4A I_o = 1.0A		2.2 2.5 2.7		V
V_{OSR}	Output voltage slew-rate			100		V/ms
V_{sens}	Sense voltage range		0		0.7	V
THERMAL SHUTDOWN						
T_j	Junction temperature		150			°C
T_H	Hysteresis				30	°C

DESCRIPTION

The L6236 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase bidirectional drive.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

The direction of rotation is controlled by the forward/reverse input (pin 1). When this pin is at a low level the motor rotates in the forward direction.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input on the device at pin 10, V_C.

In addition, a 1V offset is added to the speed demand voltage to match the minimum output on the PLL.

An external resistor, R_s, sense the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop in the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = (V_C - 1)/7\ R_s$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1)/(7\ I_{max})$$

where V_X is the full scale voltage of V_C.

In this way the V_C/I_{out} characteristics can be modified. Note that V_X max is clamped at 5.9V.

The most important feature of the L6236 is slew rate control. With this device a typical value of $0.1V/\mu s$ is achieved, reducing EMI to a very low value.

In a delta configuration a key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the integrated free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

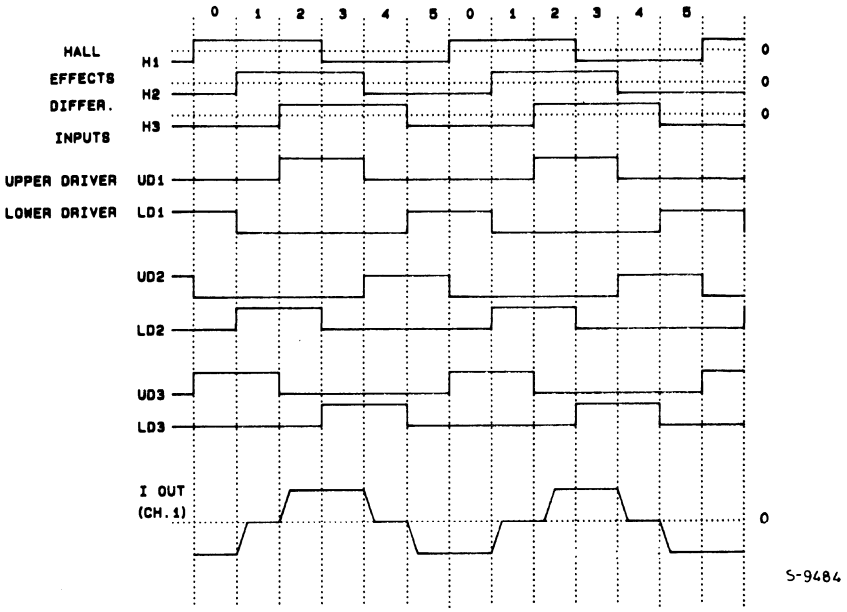
The L6236 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - **TRUTH TABLE FOR FORWARD ROTATION**

HALL EFFECT DIFF. INPUT			UPPER DRIVER STATUS			LOWER DRIVER STATUS		
1 = POSITIVE 0 = NEGATIVE			1 = ON 0 = OFF			1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	1	0	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	1	0
0	0	0	1	0	0	0	1	0

Fig. 2 - Timing diagram

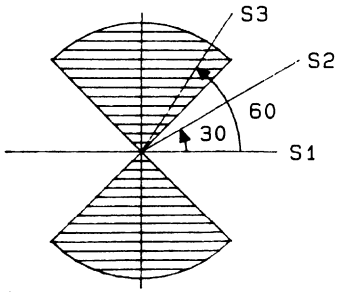


DETERMINING HALL EFFECT SENSOR CODING

The L6236 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 2, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6236. Note that the rotation in fig. 3 must be counterclockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 3 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chose whose sensor outputs do not match the L6236 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 3



For example, let us examine the output pattern of a different type of motor (fig. 4). Assuming 90 windows at 180 intervals, then with respect to fig. 3, a similar diagram, fig. 5, results in sensors 60 apart with the windows rotating clockwise. The situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 5, this should be used for the L6236 Hall Effect Input H1. After 30 of rotation CW, the H2 input of the L6236 must go high. The inverse of S1 from the motor would satisfly this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By countinuing around the diagram, one can develop a pattern which matches that for the L6236.

Fig. 4

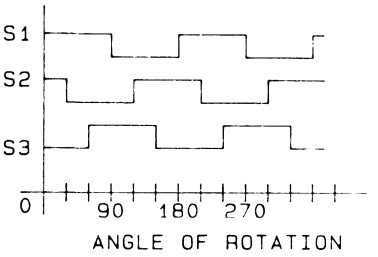
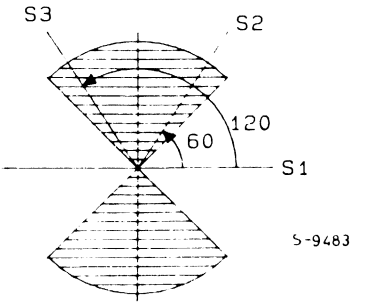


Fig. 5

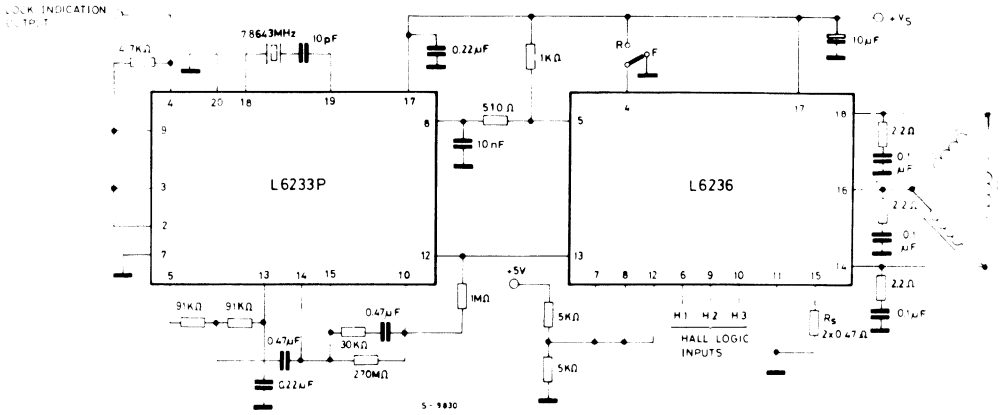


Thus the conversione table for this particular motor is:

Motor Sensors	L6236 inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 actual inverter gate is not necessary with the L6236. Since the L6236 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

Fig. 6 - Application circuit using the L6233 PLL-Controller



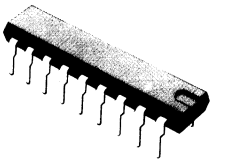
L6506

ADVANCE DATA

CURRENT CONTROLLER FOR STEPPING MOTORS

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, or L7180, the chip set forms a constant current drive for an inductive load and performs all the interface function from the control logic thru the power stage.

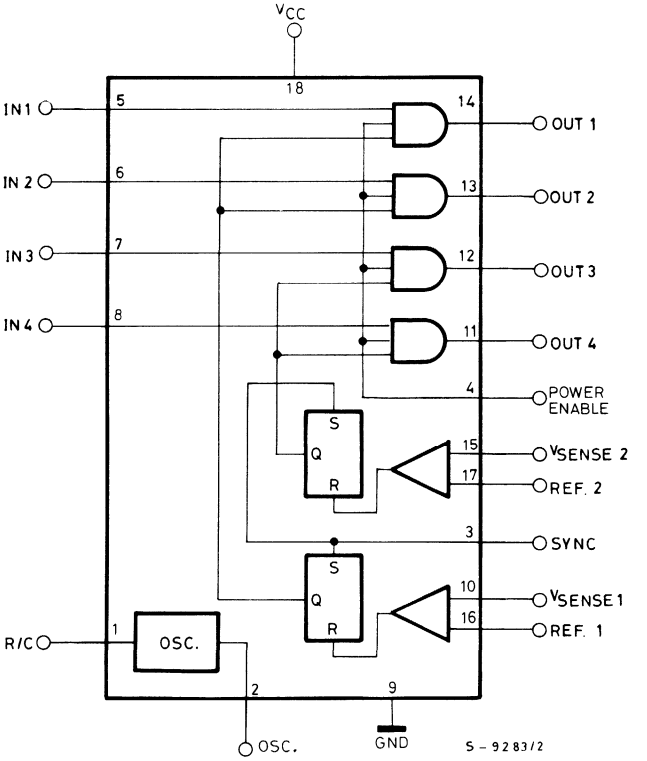
Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.



DIP-18 Plastic

ORDERING NUMBER: L6506

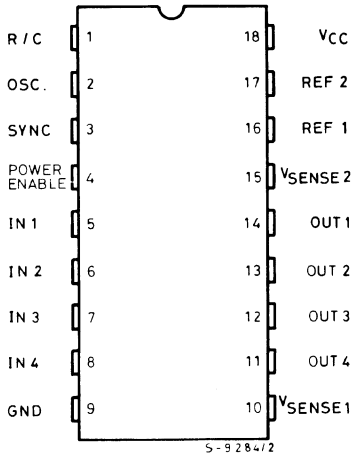
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	10	V
V_i	Input signals	7	V
P_{tot}	Total power dissipation ($T_{amb} = 70°C$)	1	W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_{amb} = 25°C unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		4.5		7	V
I_{CC}	Quiescent supply current	V_{CC} = 7V			25	mA

COMPARATOR SECTION

V_{IN}	Input voltage range	V_{sense} inputs	-0.3		3	V
V_{IO}	Input offset voltage	V_{IN} = 1.4V			± 5.0	mV
I_{IO}	Input Offset Current				± 200	nA
I_{IB}	Input bias current				1	μA
	Response time	V_{REF} = 1.4V V_{SENS} = 0 to 5V		0.8	1.5	μs

COMPARATOR SECTION PERFORMANCE (over operating temperature range)

V_{IO}	Input offset voltage	V_{IN} = 1.4V			± 20	mV
I_{IO}	Input offset current				± 500	nA

LOGIC SECTION (over operating temperature range) - (TTL compatible inputs & outputs)

V_{IH}	Input high voltage		2.0		V_S	V
V_{IL}	Input low voltage				0.8	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = 400μA	2.5	3.5		V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} = 4.0mA		0.25	0.4	V
I_{OH}	Output source current Outputs 1 - 4	V_{CC} = 4.75V	2.75			mA

OSCILLATOR

f_{osc}	Frequency Range		5		70	KHz
$V_{th\,L}$	Lower threshold voltage			0.33V_{CC}		V
$V_{th\,H}$	Higher threshold voltage			0.66V_{CC}		V
R_i	Internal discharge resistor		0.7	1	1.3	KΩ

CIRCUIT OPERATION

The L6506 is intended for use with dual bridge drivers, such as the L298, quad darlington arrays, such as the L7180, or discrete power transistors to drive stepper motors and other similar loads. The main function of the device is to sense and control the current in each of the load windings.

A common on-chip oscillator drives the dual chopper and sets the operating frequency for the pulse width modulated drive. The RC network on pin 1 sets the operating frequency which is given by the equation:

$$f = \frac{1}{0.69\ RC} \quad \text{for } R > 10K$$

The oscillator provides pulses to set the two flip-flops which in turn cause the outputs to activate the drive. When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to V_{ref} and the corresponding comparator resets its flip-flop interrupting the drive current until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref}. Since separate inputs are provided for each chopper, each of the loads may be programmed independently allowing the device to be used to implement microstepping of the motor. Lower threshold of L6506's oscillator is 1/3 V_{CC}. Upper threshold is 2/3 V_{CC} and internal discharge resistor is 1KΩ ±30%.

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground.

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can be found by looking at the figure 1 and are:

$$T2 = 0.69\ C1\ \frac{R1\ R_{IN}}{R1 + R_{IN}} \qquad (1)$$

$$T1 = 0.69\ R1\ C1 \qquad (2)$$

$$DC = \frac{T2}{T1 + T2} \qquad (3)$$

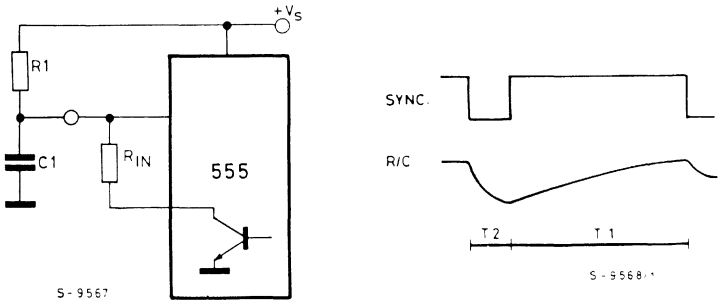
By substituting equations 1 and 2 into equation 3 and solving for the value of R1 the following equations for the external components can be derived:

$$R1 = \left(\frac{1}{DC} - 2\right) R_{IN} \qquad (4)$$

$$C1 = \frac{T1}{0.69\ R1} \qquad (5)$$

Looking at equation 1 it can easily be seen that the minimum pulse width of T2 will occur when the value of R1 is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 4 the minimum value for R1 of 700Ω (1KΩ - 30%) should be used to guarantee the required pulse width.

Fig. 1 - Oscillator circuit and waveforms



APPLICATIONS INFORMATION

The circuits shown in figures 2 and 3 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. Figure 3 shows the L6506 used with the L7180 to drive a 4 phase unipolar motor. The peak current can be calculated using the equation:

$$I_{peak} = \frac{V_{ref}}{R_{sense}}$$

The circuit of Fig. 2 can be used in applications requiring different peak and hold current values by modifying the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

Fig. 2 - Application circuit bipolar stepper motor driver

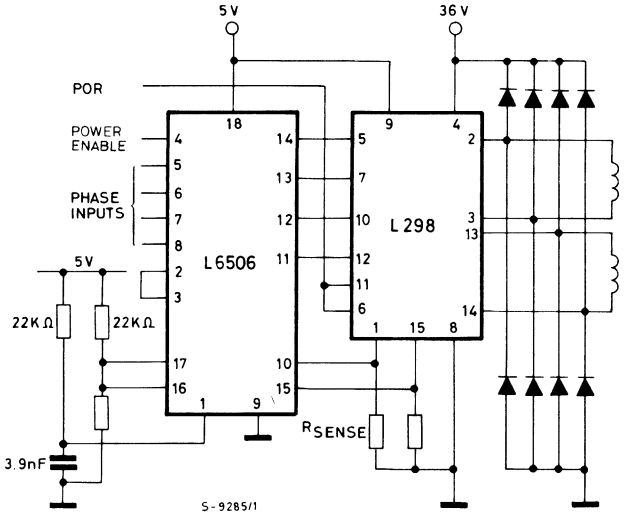
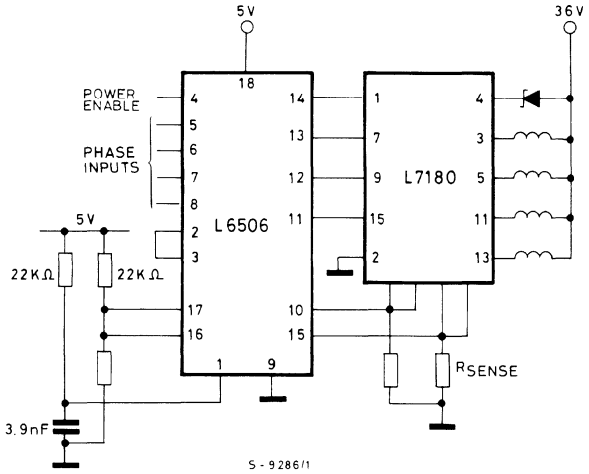


Fig. 3 - Application circuit unipolar stepper motor

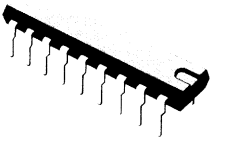


LM1837

DUAL LOW NOISE TAPE PREAMPLIFIER WITH AUTOREVERSE

- PROGRAMMABLE TURN-ON DELAY
- TRANSIENT-FREE MUTING AND POWER-UP – NO POPS
- LOW-NOISE – 0.6 μV CCIR/ARM
- HIGH POWER SUPPLY REJECTION – 95dB
- LOW DISTORTION – 0.03% AND HIGH SLEW RATE – 6V/μs
- SHORT CIRCUIT PROTECTION
- INTERNAL DIODES FOR DIODE SWITCHING APPLICATIONS

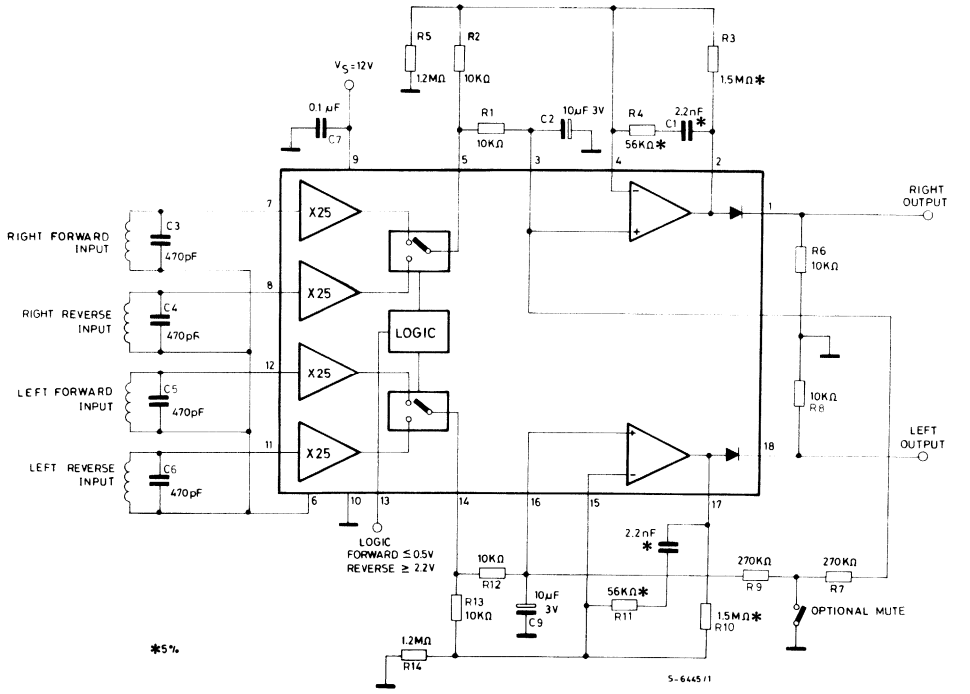
The LM1837 is a dual autoreversing high gain tape preamplifier for applications requiring optimum noise performance. It has forward (left, right) and reverse (left, right) inputs which are selectable through a high impedance logic pin. It is an ideal choice for a tape playback amplifier when a combination of low noise, autoreversing, good power supply rejection, and no power-up transients are desired. The application also provides transient-free muting with a single pole grounding switch.



DIP-18 Plastic

ORDERING NUMBER: LM1837

Fig. 1 – Autotoreversing tape plyback application

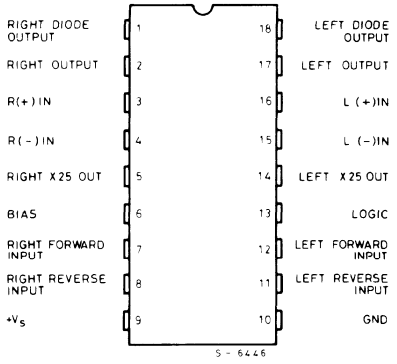


LM1837

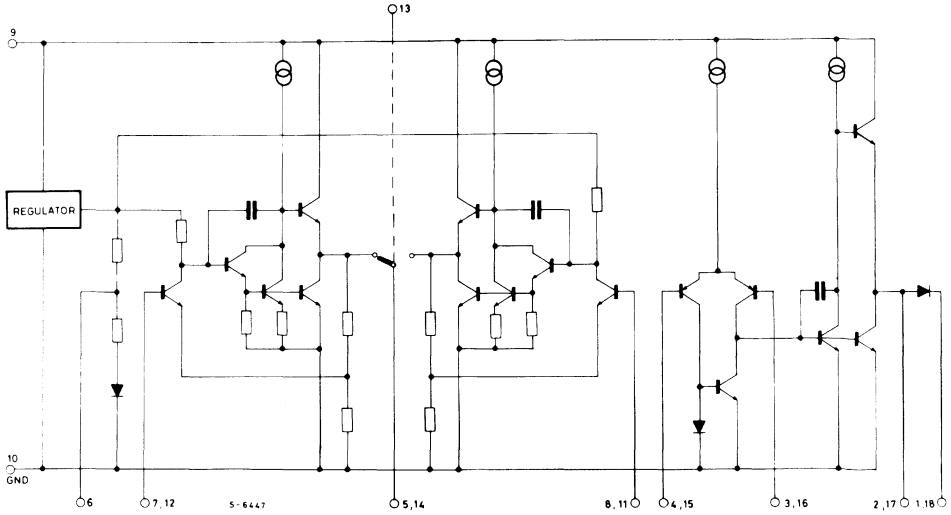
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	18 V
	Voltage on pins 1 and 18	18 V
P_{tot}	Package dissipation	1390 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature	0 to 70 °C
	Minimum voltage on any pin	-0.1 V

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	90	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V, see test circuits)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage	R5 removed from circuit for low voltage operation	4		18	V
I_S	Supply current	V_S = 12V		9	15	mA
d	Total harmonic distortion	f = 1KHz V_I = 0.3mV pins 2 and 17, see test circuit		0.03		%
	THD + noise (note 1)	f = 1KHz V_O = 1V pins 2 and 17, see test circuit		0.1	0.25	%
SVR	Power supply rejection	input ref. f = 1KHz, 1 Vrms	80	95		dB
C_S	Channel separation (note 2)	f = 1KHz, output = 1 Vrms Output to output				
	Left to right		40	60		dB
	Forward to reverse		40	60		dB
S/N	Signal-to-noise (note 3)	Unweighted 32Hz - 12.74 KHz (note 1)		58		dB
		CCIR/ARM (note 4)		62		dB
		A weighted		64		dB
		CCIR, peak (note 5)		52		dB
e_N	Noise	Output voltage CCIR/ARM (note 4)		120	200	μV

INPUT AMPLIFIERS

I_b	Input bias current			0.5	2	μA
	Input impedance	f = KHz	150			KΩ
	AC gain		27	28	29	dB
	AC gain imbalance			± 0.15	± 0.5	dB
V_O	DC output voltage		2.1	2.5	2.9	V
V_O	Output voltage mismatch	pins 5 and 14	- 200	30	200	mV
I_O^+	Output source current	pins 5 and 14	2	10		mA
I_O^-	Output sink current	Pins 5 and 14	300	600		μA

LOGIC LEVEL

	Forward				0.5	V
	Reverse		2.2			V
	Logic pin current			2	6	μA
	DC voltage change at pins 5 and 14	Change logic state	-100	20	100	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OUTPUTS AMPLIFIERS						
	Closed loop gain	stable operation	5			V/V
G_v	Open loop voltage gain	DC		100		dB
	Gain bandwidth product			5		MHz
	Slew rate			6		V/μs
V_{OS}	Input offset voltage			2	5	mV
I_{OS}	Input offset current			20	100	nA
I_i	Input bias current			250	500	nA
I_O^+	Output source current	Pin 2 or 17	2	10		mA
I_O^-	Output sink current	Pin 2 or 17	400	900		μA
V_O	Output voltage swing	Pin 2 or 17		11		Vp-p
	Output diode leakage	Voltage on pins 1 and 18 = 18V		0	10	μA

Note:

1 — Measured with an average responding voltmeter using the filter circuit in figure 4. This simple filter is approximately equivalent a "brick wall" filter with a passband of 20Hz to 20KHz (see Application Hints). For 1KHz THD the 400Hz high pass filter on the distortion analyzer is used.

2 — Channel separation can be measured by applyng the input signal through transformers to simulate a floating source (see Application Hints). Care must be taken to shield the coils from extraneous signal. Actual production test techniques simulate this floating source with a more complex op amp circuit.

3 — The numbers are referred to an output level of 160mV at pins 2 and 17 using the circuit figure 2. This corresponds

4 — Measured with an average responding voltmeter using the Dolby lab's standard CCIR filter having a unity gain reference 2KHz.

5 — Measured using the Rhode-Schwartz psophometer, mode UPGR.

Fig. 2 – Test circuit

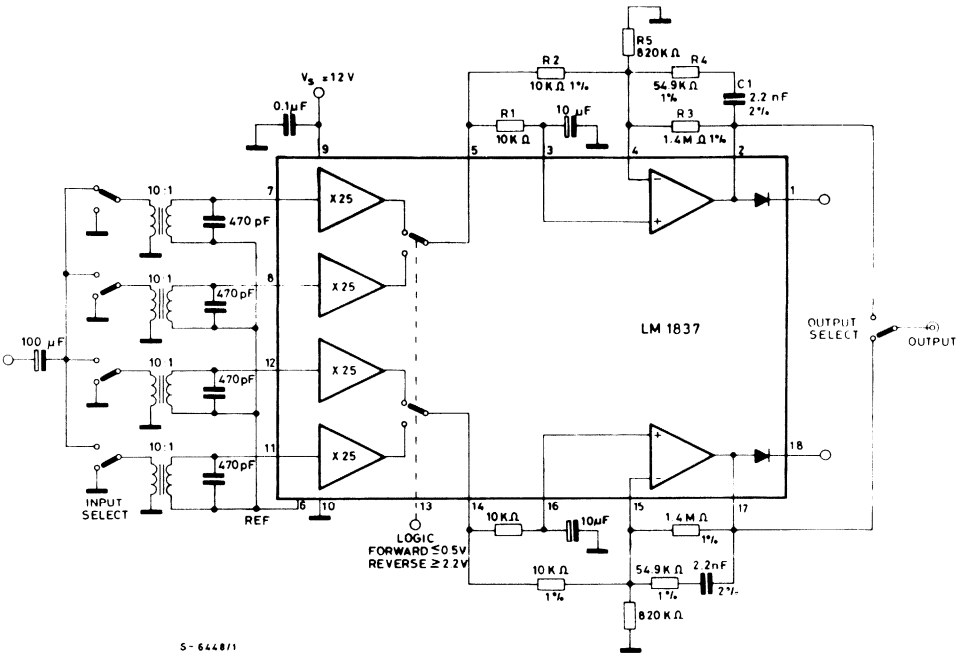


Fig. 3 – Input amplifier distortion vs. input level

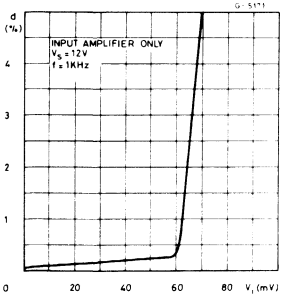


Fig. 4 – Input amplifier gain and phase vs frequency

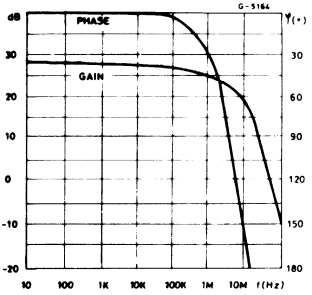


Fig. 5 – Output amplifier open loop gain and phase vs. frequency

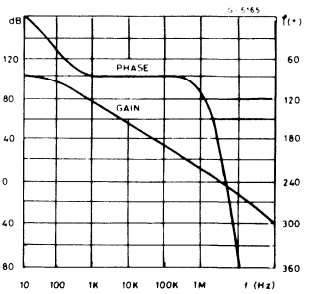


Fig. 6 – Noise voltage vs. frequency

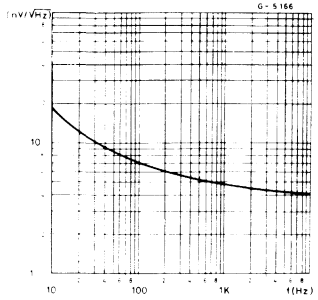


Fig. 7 – Noise current vs. frequency.

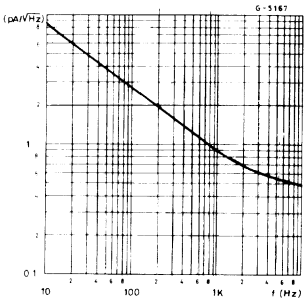


Fig. 8 – Total harmonic distortion vs. frequency

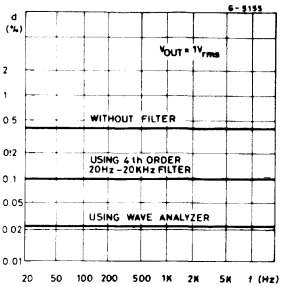


Fig. 9 – Turn-on delay vs. component values and gain

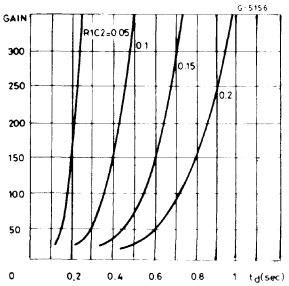


Fig. 10 SVR vs. frequency

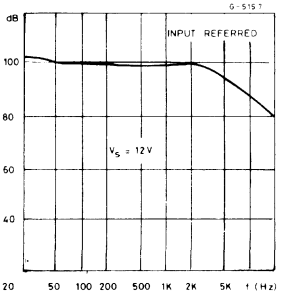


Fig. 11 – SVR vs. supply voltage

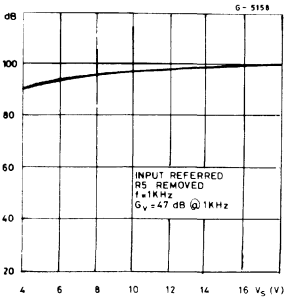


Fig. 12 – I_S vs. V_S

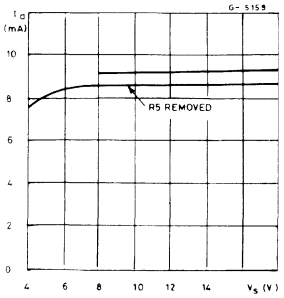


Fig. 13 – Rigth to left channel separation vs. frequency

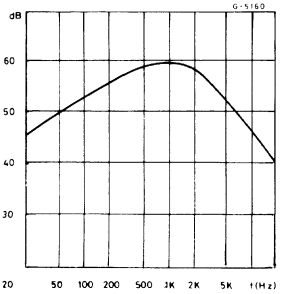


Fig. 14 – Forward to reverse channel separation vs. frequency

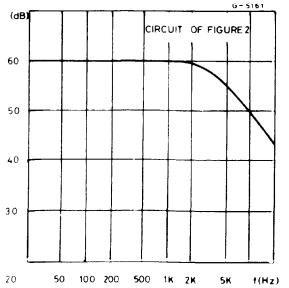


Fig. 15 – Input amplifier DC output voltage vs. temperature (pins 5, 4)

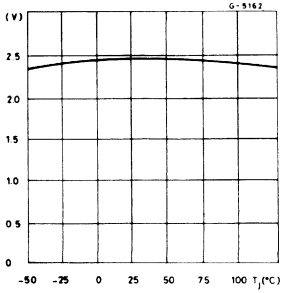


Fig. 16 – Frequency response of test circuit

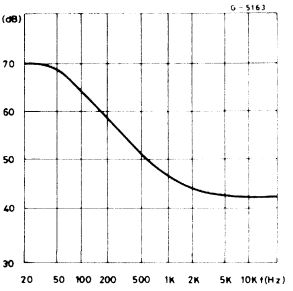
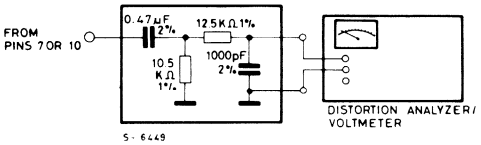


Fig. 17 – Simple 32Hz - 12740Hz filter and meter



APPLICATION INFORMATION

EXTERNAL COMPONENTS (Figures 1 and 18)

Component	Normal Range of Value and Function
R1, C2 and R12, C9	2KΩ-40KΩ, 0.1μF-10μF (low leakage). Set turn-on delay and second amplifier's low frequency pole. Leakage current in C2 results in DC offset between the amplifier's inputs and therefore this current should be kept low. R1 is set equal to R2 such that any input offset voltage due to bias current is effectively cancelled. An input offset voltage is generated by the input offset current multiplied by the value of these resistors.
R2, R3 and R13, R10	2KΩ-40KΩ, 500KΩ-10KΩ. Set the DC and frequency gain of the output amplifier. The total input offset voltage will also be multiplied by the DC gain of this amplifier. They are threfore essential to keep the input offset voltage specification in mind when employing high DC gain in the output amplifier; i.e., 5mV x 400 = 2V offset at the output.
R4, C1 and R11, C8	10KΩ-200KΩ, 470pF to 10nF. Set tape playback equalization characteristics in conjunction with R3 (calculations for the component values are included in the application (Hints section).
R6, R8	2KΩ-47KΩ. Blas the output diode in DC switching applications. These resistors can be excluded if diode switching is not desired.
C3...C6	100pF-1000pF Often used to resonate with tape head in order to compensate for tape playback losses including tape head gap and eddy current. For a typical cassette tape head, the resonant frequency selected is usually between 13KHz and 17KHz.
R5, R14	100KΩ-10MΩ. Increase the output DC bias voltage from the nominal 2.5V value (see Application information).
R7, R9	Optionally used for tape muting. The use of these resistor can also provide "no-pop" turn-off if desired (see Application information).

APPLICATION INFORMATION (continued)

Fig. 18 - Autoreversing tape plyback application.

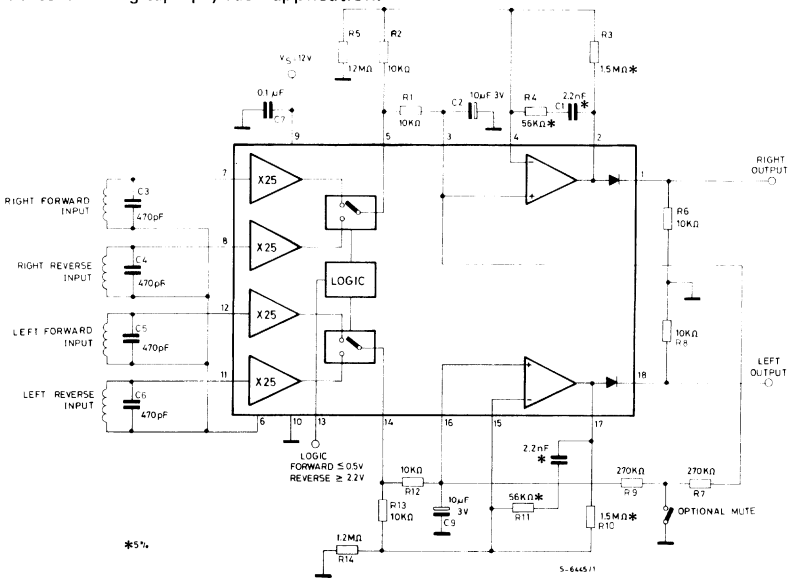
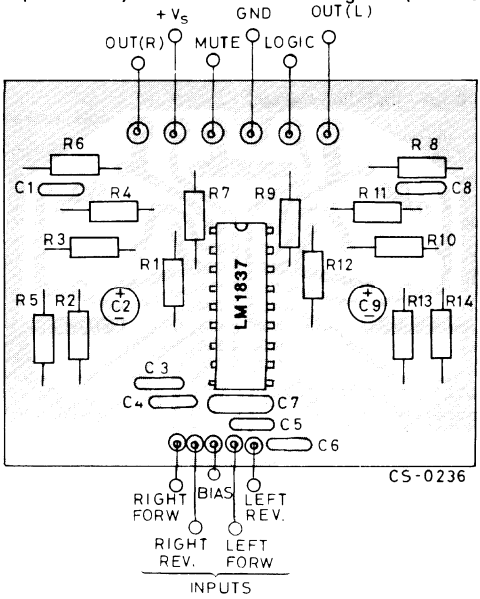


Fig. 19 - P.C. board and components layout of the circuit of Fig. 18 (1 : 1 scale)

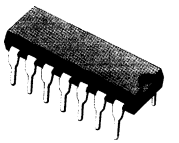


LS404

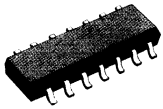
HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is partucularly intended for professional and telecom applications (active filters, etc.).
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.



DIP-14 Plastic
(0.25)



SO-14J

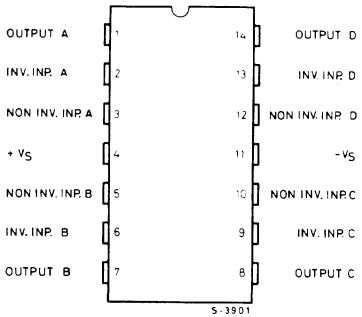
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_i	Input voltage	(positive)	$+ V_s$	
		(negative)	$-V_s - 0.5$	V
V_i	Differential input voltage		$\pm (V_s - 1)$	
T_{op}	Operating temperature	**LS 404**	-25 to + 85	°C
		LS 404C	0 to + 70	°C
P_{tot}	Power dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage temperature		-55 to + 150	°C

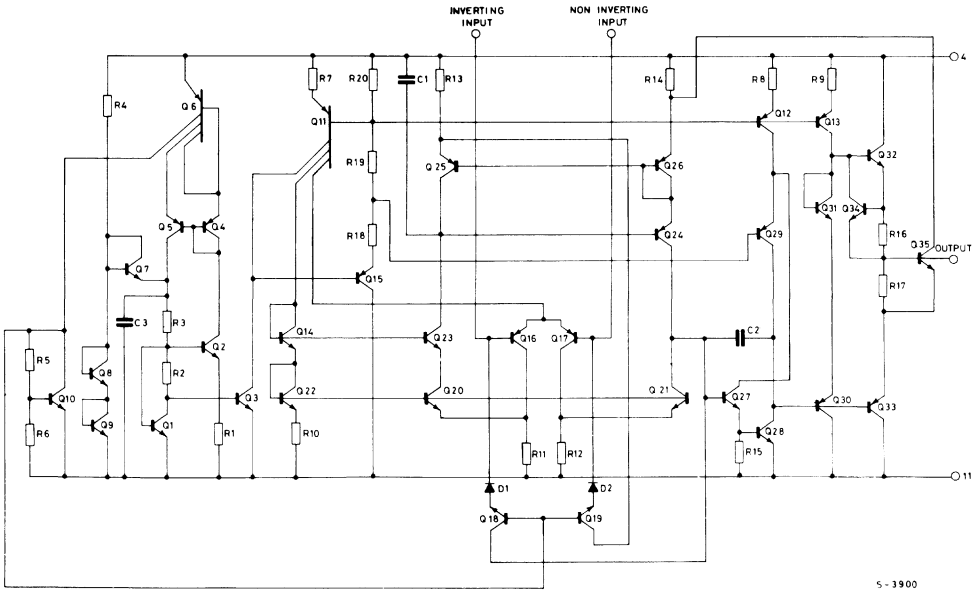
CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)

Type	DIP 14	SO-14
LS 404 LS 404C	— LS 404CB	LS 404M LS 404CM



SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			DIP 14	SO-14
$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 12V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	LS 404			LS 404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			1.3	2		1.5	3	mA
I_b	Input bias current			50	200		100	300	nA
R_i	Input resistance	f = 1KHz		0.7			0.5		MΩ
V_{os}	Input offset voltage	R_g = 10KΩ		1	2.5		1	5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input offset current			10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	R_L = 2KΩ V_s = ±12V V_s = ±4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	unity gain R_L = 2KΩ f = 1 KHz V_o = 2Vpp f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC output voltage swing	R_L = 2KΩ V_s = ± 12V V_s = ± 4V	± 10	± 3		± 10	± 3		V
V_o	Large signal voltage swing	f = 10KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		Vpp
SR	Slew rate	unity gain R_L = 2KΩ	0.8	1.5			1		V/μs
CMR	Comm. mode rejection	V_i = 10V	90	94		80	90		dB
SVR	Supply voltage rejection	V_i = 1V f = 100Hz	90	94		86	90		dB
CS	Channel separation	f = 1KHz	100	120			120		dB

Fig. 1 - Supply current vs. supply voltage

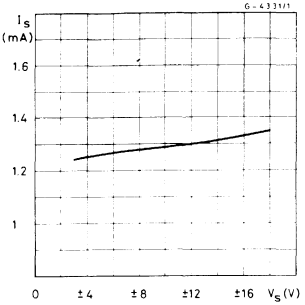


Fig. 2 - Supply current vs. ambient temperature

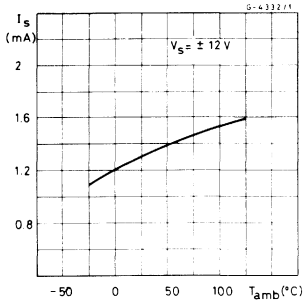


Fig. 3 - Output short circuit current vs. ambient temperature

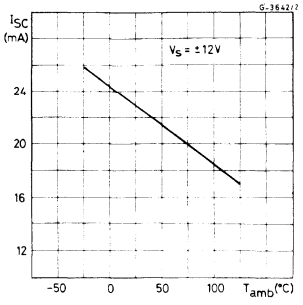


Fig. 4 - Open loop frequency and phase response

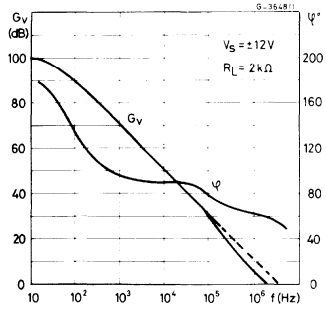


Fig. 5 - Open loop gain vs. ambient temperature

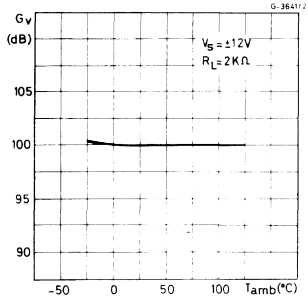


Fig. 6 - Supply voltage rejection vs. frequency

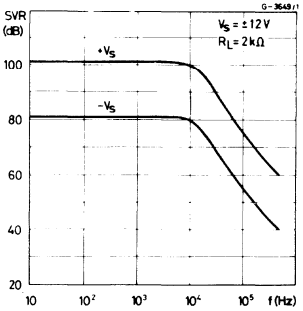


Fig. 7 - Large signal frequency response

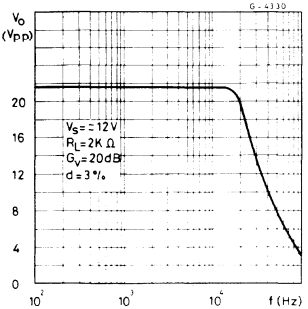


Fig. 8 - Output voltage swing vs. load resistance

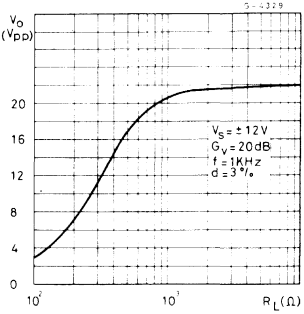
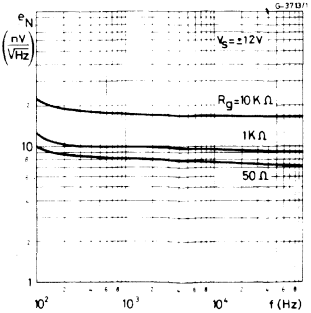


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

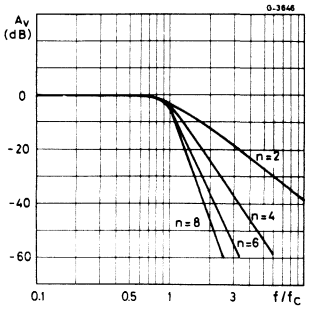
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Fig. 10 - Amplitude response



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

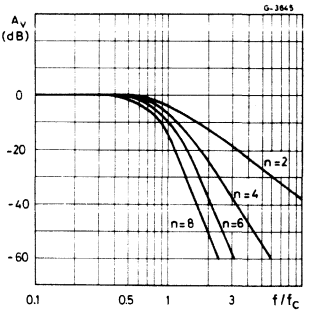
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyshev or Butterworth.
- Very small overshoot response to step inputs
- Fast rise time.

Fig. 11 - Amplitude response

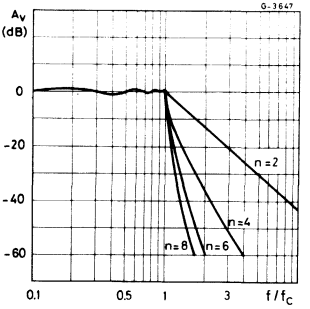


CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs.

Fig. 12 - Amplitude response (± 1 dB ripple)



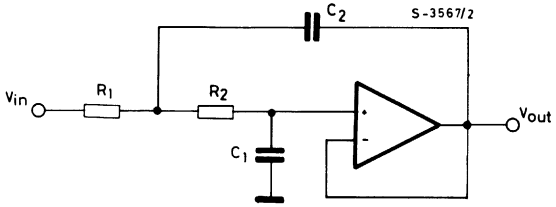
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filter to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

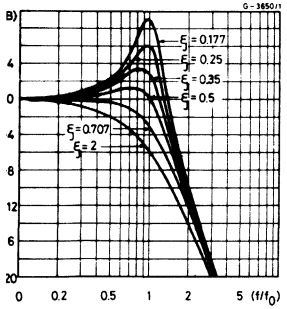
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

TAB. 1

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v = -3 dB
Chebyschev	$<\frac{\sqrt{2}}{2}$	$>\frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

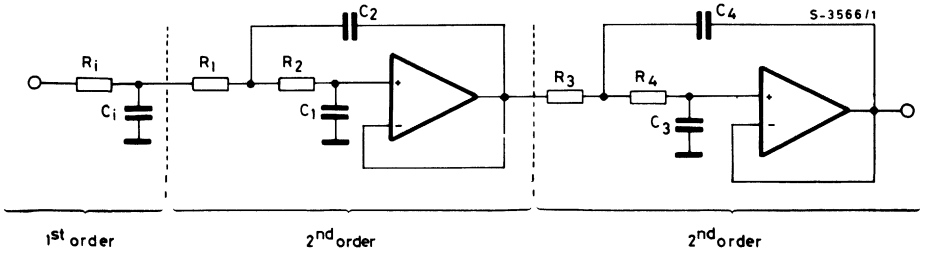
$$C_1 = \frac{1}{R}\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

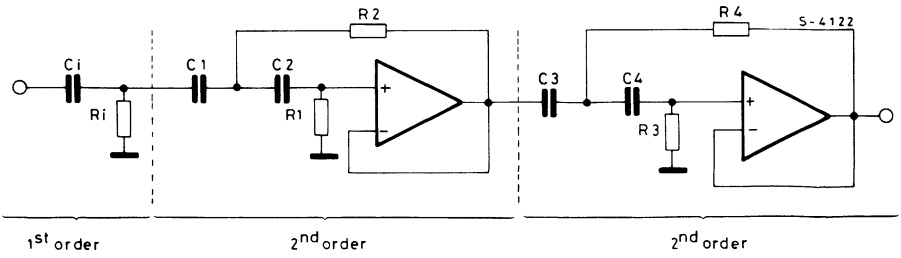
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

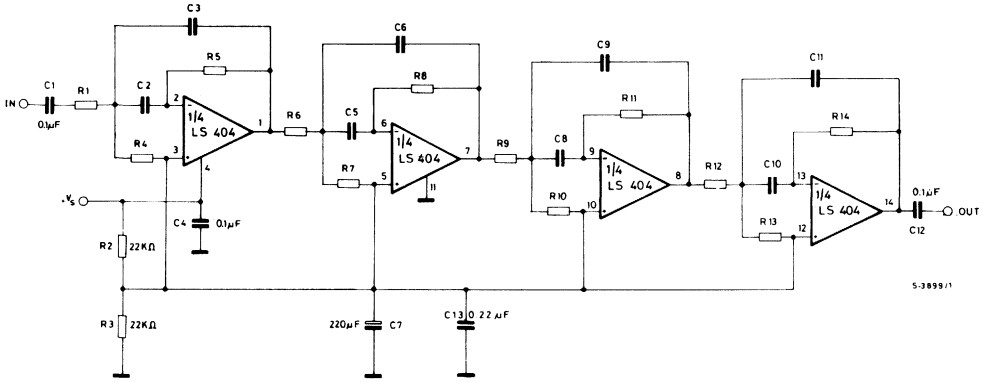
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

Fig. 17 - Multiple feedback 8-pole bandpass filter.



f_c = 1.180Hz; A = 1; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF;
$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ; $R_5 = R_8 = R_{11} = R_{14}$ = 330KΩ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3KΩ

Fig. 18 - Frequency response of band-pass filter

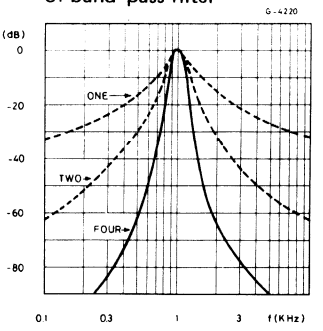
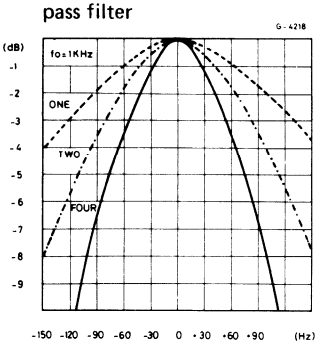
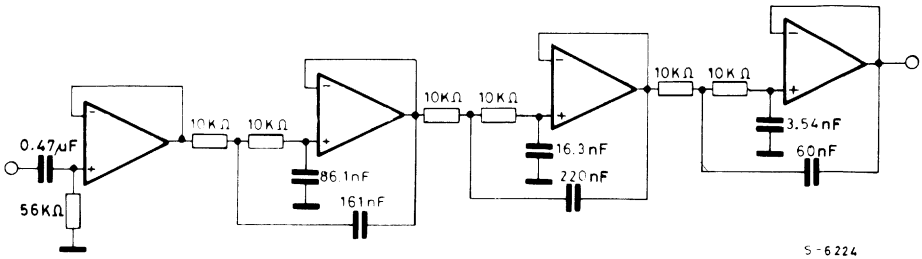


Fig. 19 - Bandwidth of band-pass filter



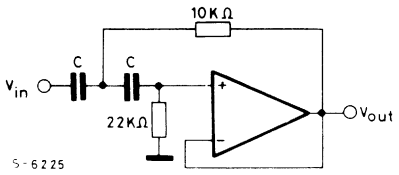
APPLICATION INFORMATION (continued)

Fig. 20 - Six-pole 355 Hz low-pass filter (Chebychev type)



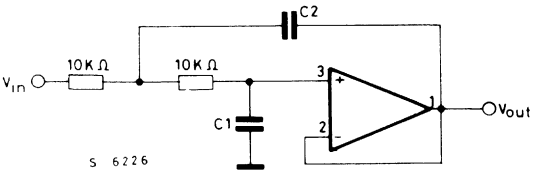
This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Fig. 21 - Subsonic filter (G_v = 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Fig. 22 - High cut filter (G_v = 0 dB)



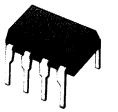
f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

LS4558N

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH UNITY GAIN BANDWIDTH
- NO CROSSOVER DISTORTION
- NO POP NOISE
- SHORT CIRCUIT PROTECTION
- HIGH CHANNEL SEPARATION

The LS4558N is a high performace dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range and the specially designed input stage allow the LS4558N to be used in **low noise audio signal processing application.** The optimized class AB output stage completely eliminates crossover, distortion, under any load conditions, has large source and sink capacity and is short circuit protected.



Minidip Plastic

SO-8J

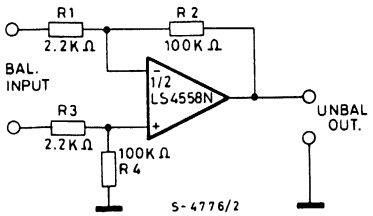
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_I	Input voltage		± V_s	
V_i	Differential input voltage		± (V_s - 1)	V
P_{tot}	Power dissipation at T_{amb}= 70°C	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

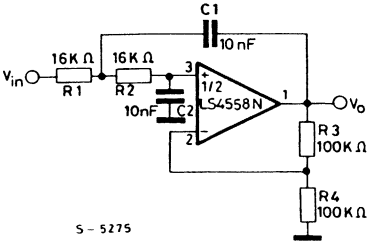
ORDERING NUMBER: LS 4558 NB (Minidip)
LS 4558 NM (Micropackage)

TYPICAL APPLICATIONS:

Balanced input audio preamplifier

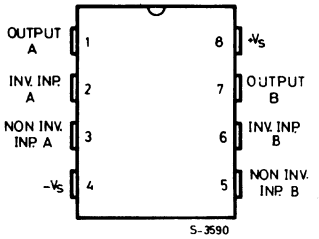


DC coupled low-pass active filter
(f = 1KHz, G_v = 6dB

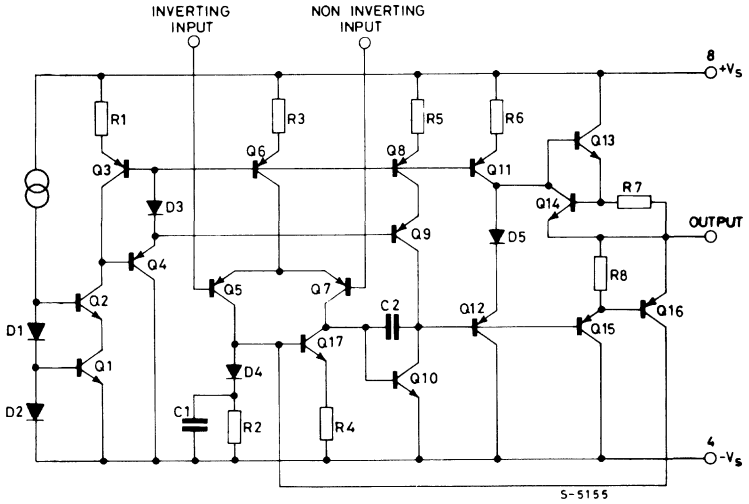


LS4558N

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one section)



THERMAL DATA

		Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	120 °C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current (*)			1	2	mA
I_b	Input bias current			50	500	nA
		$T_{min} < T_{op} < T_{max}$			800	nA
R_i	Input resistance	f = 1 KHz	0.3	1		MΩ
V_{os}	Input offset voltage	$R_g \leq 10$ KΩ		0.5	5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			7.5	mV
I_{os}	Input offset current			20	200	nA
		$T_{min} < T_{op} < T_{max}$			500	nA
I_{sc}	Output short circuit current			23		mA
G_v	Large signal open loop voltage gain	R_L= 2 KΩ	86	100		dB
B	Gain-bandwidth product	f = 20 KHz	2	3		MHz
e_N	Total input noise voltage	f = 1 KHz R_g= 50Ω R_g= 1 KΩ R_g= 10 KΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
e_N	Popcorn noise	B = 1 Hz to 1 KHz R_g= 10 KΩ t = 10 sec			10	μV peak
d	Distortion	G_v= 20 dB R_L= 2 KΩ V_o= 2 Vpp f = 1 KHz		0.03		%
V_o	Output voltage swing	R_L= 2 KΩ		± 13		V
V_o	Large signal voltage swing	R_L= 10 KΩ f = 10 KHz		28		Vpp
Transient response	Rise time	V_i = 20 mV R_L= 2 KΩ C_L= 100 pF		0.13		μS
	Overshoot			5		%
SR	Slew rate	unity gain R_L= 2 KΩ	0.8	1.5		V/μs
CMR	Common mode rejection	V_i= 10V $T_{min} < T_{op} < T_{max}$	70	90		dB
SVR	Supply voltage rejection	V_i= 1V f = 100 Hz $T_{min} < T_{op} < T_{max}$	80	100		dB
CS	Channel separation	f = 10 KHz R_g= 1 KΩ		105		dB

(*) Both amplifiers.

Fig. 1 - Open loop frequency and phase response

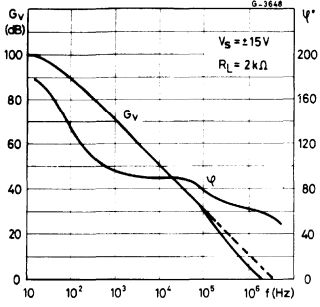


Fig. 2 - Open loop gain vs. ambient temperature

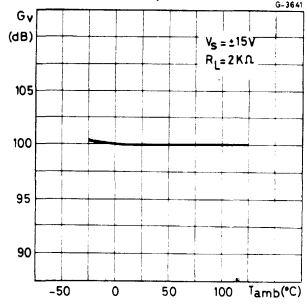


Fig. 3 - Supply voltage rejection vs. frequency

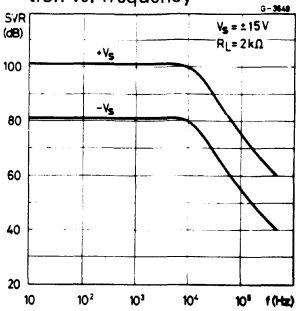


Fig. 4 - Large signal frequency response

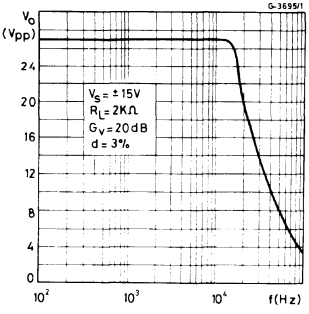


Fig. 5 - Output voltage swing vs. load resistance

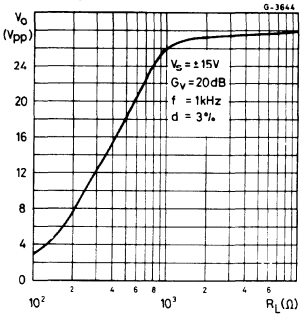


Fig. 6 - Total input noise vs. frequency

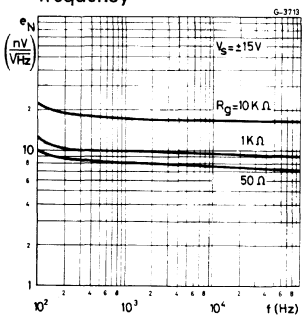


Fig. 7 - Channel separation

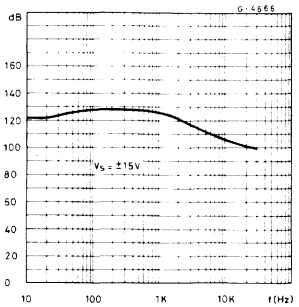


Fig. 8 - Transient response

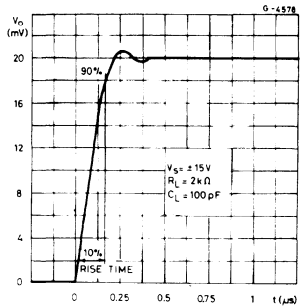
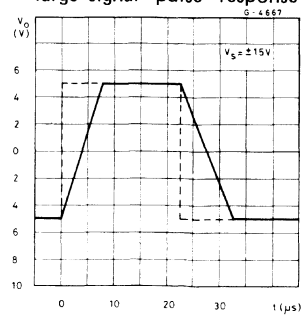
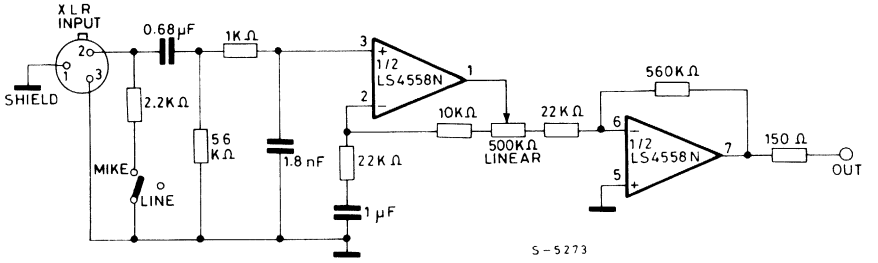


Fig. 9 - Voltage follower large-signal pulse response



APPLICATION INFORMATION

Fig. 10 - Mike/Line preamplifier for audio mixers (0 dB to 60 dB continuously variable gain)



Note – The particular characteristics of the circuit of fig. 10 is that using a linear potentiometer, the gain is continuously variable in a logarithmic mode from 0 dB to 60 dB in the audio band.

Fig. 11 - Microphones nomograph

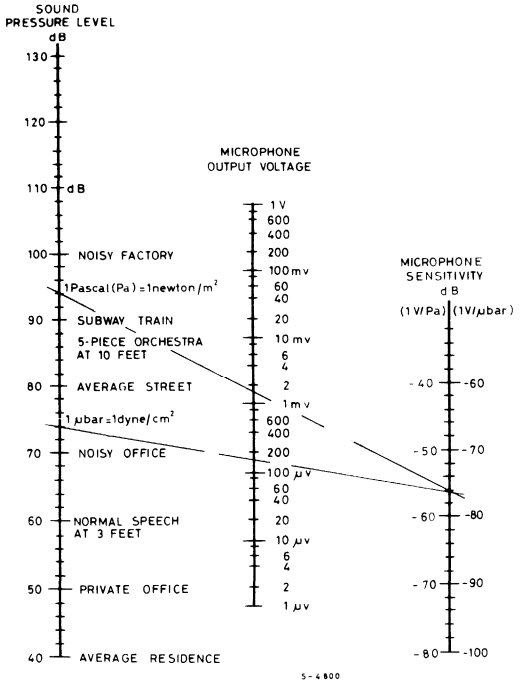


Fig. 12 - Very Low-Noise mike preamplifier (G_v= 40 dB)

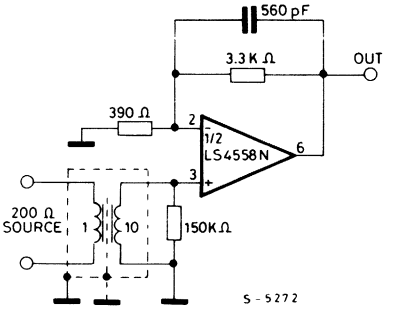
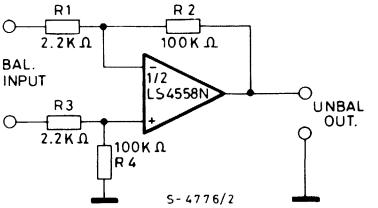


Fig. 13 - Balanced input audio preamplifier



APPLICATION INFORMATION (continued)

Fig. 14 - 20 Hz to 200 Hz variable High-pass filter (G_v = 3 dB)

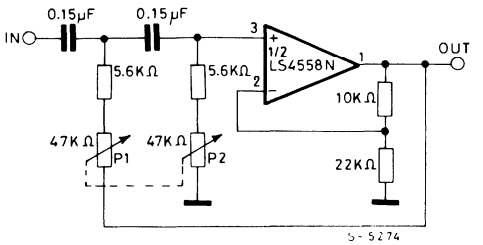


Fig. 15 - Frequency response of the High-pass filter of fig. 14

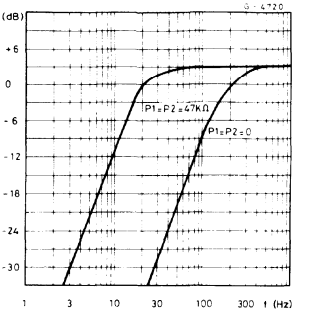


Fig. 16 - DC coupled low-pass active filter (f = 1KHz, G_v= 6 dB)

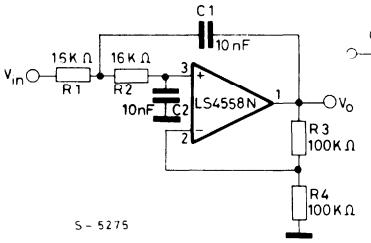


Fig. 17 - Switchable HP-LP audio filter

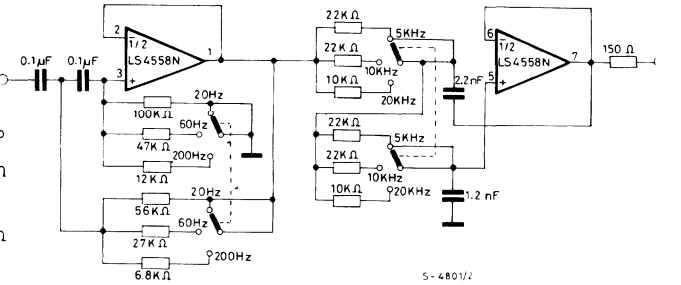
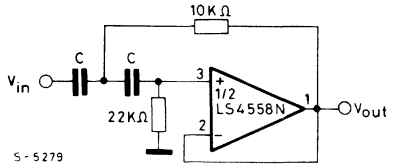
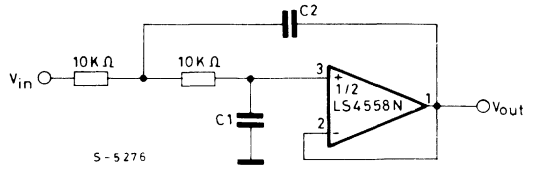


Fig. 18 - Subsonic or rumble filter (G_v= 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

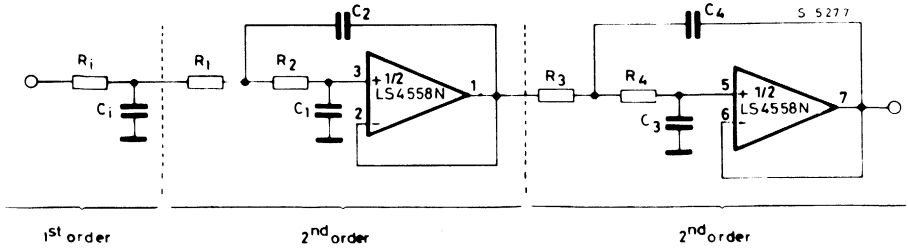
Fig. 19 - High-cut filter (G_v= 0 dB)



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 20 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33$ nF

$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97$ nF

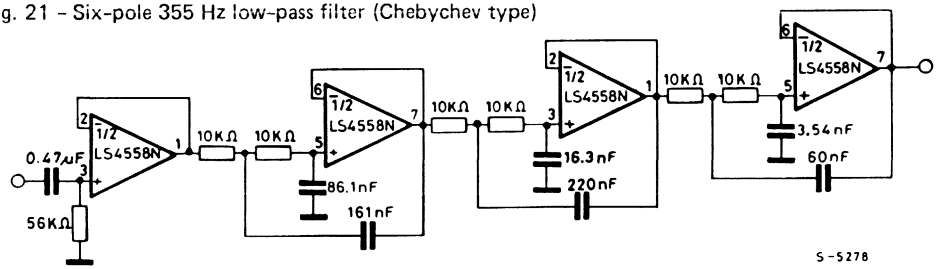
$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20$ nF

$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45$ nF

$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14$ nF

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 21 - Six-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

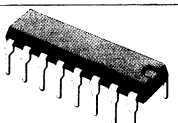
M082/A M083/A M086/A

NOT FOR NEW DESIGN

TONE GENERATORS

- SINGLE POWER SUPPLY
- WIDE SUPPLY VOLTAGE OPERATING RANGE
- LOW POWER DISSIPATION < 500mW
- 13 (M082/A, M083/A) OR 12 (M086/A) TONE OUTPUTS
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN ± 0.069%
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M082/A, M083/A and M086/A are monolithic tone generators specially designed for electronic organs. The only difference between the M082, M083, M086 and the M082A, M083A, M086A is the maximum input clock frequency, which is 4500KHz for the standard types and 2500KHz for the "A" types. Constructed on a single chip using low threshold N-channel silicon gate technology they are supplied in a 16 lead dual in-line plastic package.



DIP-16 Plastic
(0.25)

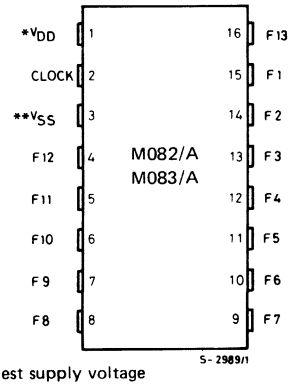
ORDERING NUMBERS: M082 B1 M082A B1
M083 B1 M083A B1
M086 B1 M086A B1

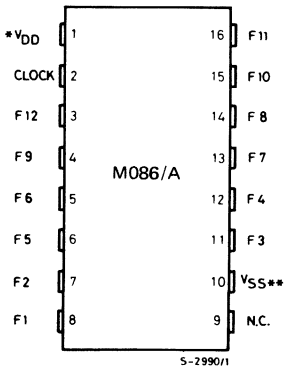
ABSOLUTE MAXIMUM RATINGS *

V_i	Voltage on any pin relative to V_{SS} (GND)	+20 to -0.3	V
T_{op}	Operating temperature	0 to 50	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS

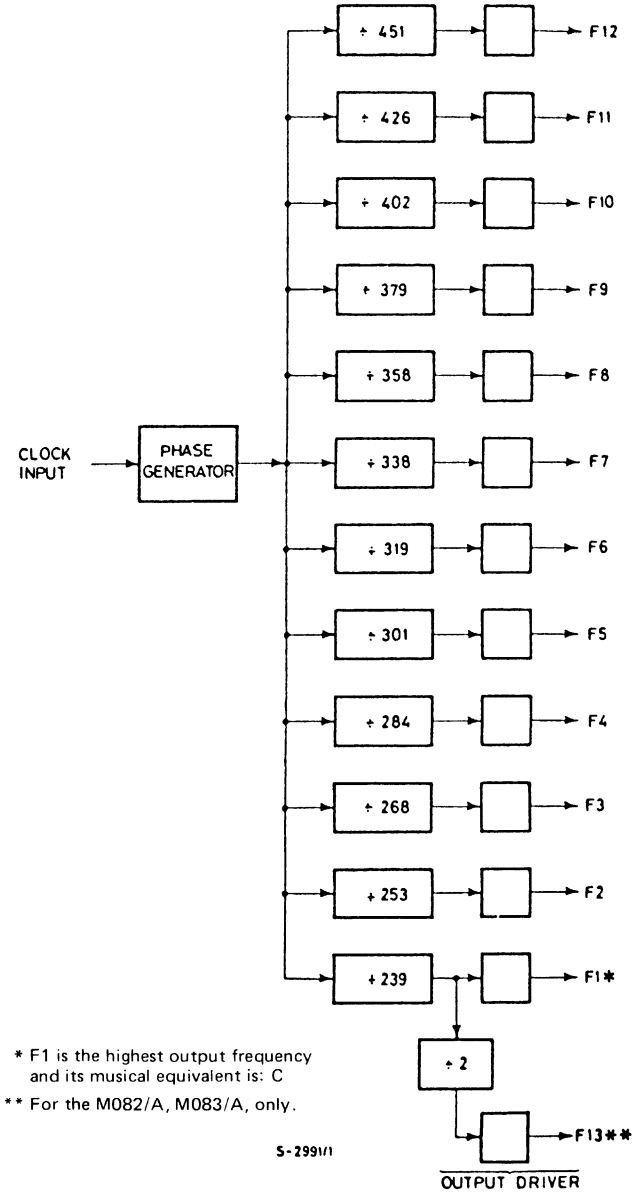




* V_{DD} is the highest supply voltage

** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



* F1 is the highest output frequency and its musical equivalent is: C

** For the M082/A, M083/A, only.

ELECTRICAL CHARACTERISTICS ($0°C \leq T_{amb} \leq 50°C$; $V_{SS}=0V$; $V_{DD}=+10V$ to $+14V$ unless otherwise specified)

Parameter		Test conditions	Values			Unit	Fig.
			Min.	Typ.	Max.		
V_{IL}	Input clock, low		V_{SS}		$V_{SS}+1$	V	1
V_{IH}	Input clock, high		$V_{DD}-1$		V_{DD}	V	
t_r, t_f	Input clock rise and fall times 10% to 90%	4.5 MHz			30	ns	1
t_{on}, t_{off}	Input clock on and off times	4.5 MHz		111		ns	1
C_I	Input capacitance			5	10	pF	
V_{OH}	Output high	0.50 mA	$V_{DD}-1.5$		V_{DD}	V	2
V_{OL}	Output low	0.70 mA	V_{SS}		$V_{SS}+1$	V	2
t_{ro}, t_{fo}	Output rise and fall times 500 pF load		250		2500	ns	3
t_{on}, t_{off}	Output duty cycle	M 082		30		%	
		M 083, M 086		50			
I_{DD}	Supply current			24	35	mA	*
f_I	Input clock frequency	M082, M083, M086	100	4000.48	4500	kHz	
f_I	Input clock frequency	M082A, M083A, M086A	100	2000.24	2500	kHz	

* Output unloaded.

Fig. 1 Input clock waveform

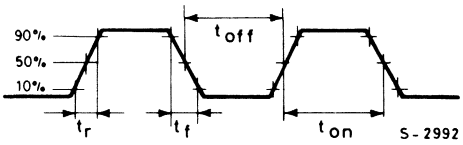


Fig. 2 - Output signal d.c. loading

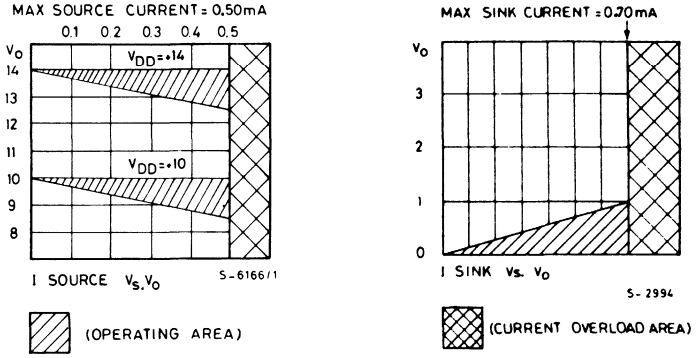
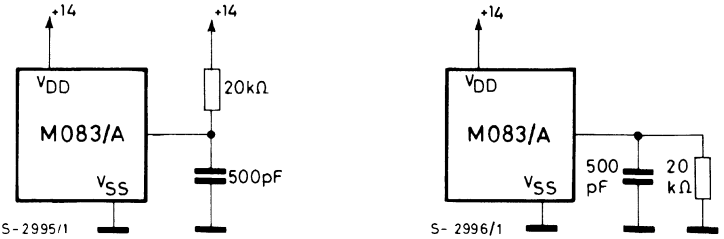


Fig. 3 - Output loading



APPLICATION INFORMATION

Keyboard frequencies for electronic organs (*)

NOTE		OCTAVES								
		0	1	2	3	4	5	6	7	8
DOH	C	16.3516	32.7032	65.4064	130.813	261.626	523.251	1046.50	2093.00	4186.01
	C #	17.3239	34.6478	69.2957	138.591	277.183	554.365	1108.73	2217.46	4434.92
RAY	D	18.3540	36.7081	73.4162	146.832	293.665	587.330	1174.66	2349.32	4698.64
	D #	19.4454	38.8909	77.7817	155.563	311.127	622.254	1244.51	2489.02	4978.03
ME	E	20.6017	41.2034	82.4069	164.814	329.628	659.255	1318.51	2637.02	5274.04
FAH	F	21.8268	43.6536	87.3071	174.614	349.228	698.456	1396.91	2793.83	5587.65
	F #	23.1247	46.2493	92.4986	184.997	369.994	739.989	1479.98	2959.96	5919.91
SOH	G	24.4997	48.9994	97.9989	195.998	391.995	783.991	1567.98	3135.96	6271.93
	C #	25.9565	51.9131	103.826	207.652	415.305	830.609	1661.22	2322.44	6644.88
LA	A	27.5000	55.0000	110.000	220.000	440.000	880.000	1760.00	3520.00	7040.00
	A #	29.1352	58.2705	116.541	233.082	466.164	932.328	1864.66	3729.31	7458.62
TE	B	30.8671	63.7354	123.471	246.942	493.883	987.767	1975.53	3951.07	7902.13

(*) The frequencies can be obtained from a 99680Hz (or multiples) master oscillator by the following division ratios, and subsequent repeated division by 2

$C^{\#}$ ÷ 451	F ÷ 358	A ÷ 284
D ÷ 426	$F^{\#}$ ÷ 338	B^{b} ÷ 268
E^{b} ÷ 402	G ÷ 319	B ÷ 253
E ÷ 379	$G^{\#}$ ÷ 301	C ÷ 239

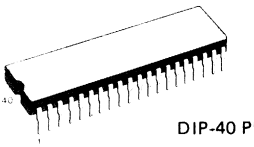
The frequency error in these approximations is less than ± 0.069%.

M108 M208

SINGLE CHIP ORGAN (SOLO + ACCOMPANIMENT)

- SIMPLE KEY SWITCH REQUIREMENTS FOR 61 KEYS, IN A MATRIX OF 12 x 6
- LOW TIME REQUIRED FOR SCANNING CYCLE OF 576 μsec.
- ACCEPTANCE OF ALL KEYS PRESSED
- TWO KEYBOARD FORMATS: 61 KEYS (SOLO) OR 24 + 37 (M108), 17 + 44 (M208) KEYS (ACC. + SOLO) WITH POSSIBILITY OF AUTOMATIC CHORDS OF THE "ACCOMPANIMENT" SECTION TOP OCTAVE SYNTHESIZER INCORPORATED FOR GENERATION OF 3 "FOOTAGES"
- MORE THAN ONE CHIP CAN BE EMPLOYED WITH SYNCHRONIZATION THROUGH THE RESET INPUT
- SEPARATED ANALOG OUTPUTS (FOR EACH FOOT) FOR "SOLO", "ACC" AND "BASS" SECTIONS (SQUARE WAVE 50% D.C.) WITH AVERAGE VALUE CONSTANT
- INTERNAL ANTI-BOUNCE CIRCUITS
- KEY DOWN AND TRIGGER OUTPUTS FOR "SOLO", "ACC." AND "BASS" SECTIONS
- SUSTAIN FOR THE LAST KEYS RELEASED IN THE "SOLO" SECTION
- CHOICE OF OPERATING MODE IN "ACC." SECTION
  - MANUAL, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEYS (FREE CHORDS WITH ALTERNATE BASS)
  - AUTOMATIC, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEY (PRIORITY TO THE LEFT FOR AUTOMATIC CHORDS AND BASS ARPEGGIO)
- MULTIPLE CHOICE POSSIBILITY ON THE CHORDS IN AUTOMATIC MODE
  - MAJOR OR MINOR THIRD
  - WITH OR WITHOUT SEVENTH
- LOW DISSIPATION OF ≤ 600 mW
- STANDARDS SINGLE SUPPLY OF +12V ± 5%
- INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGES

The M108 and M208 are realized on a single monolithic chip using N-channel silicon gate technology.
They are available in a 40 lead dual in-line plastic package.



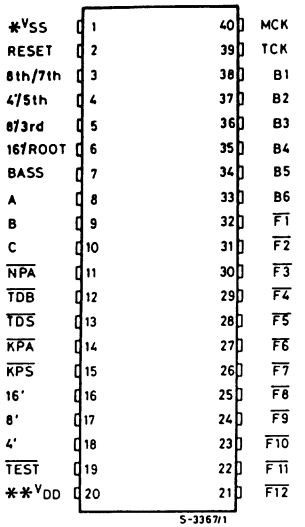
DIP-40 Plastic

ORDERING NUMBERS: M 108 B1
M 208 B1

ABSOLUTE MAXIMUM RATINGS

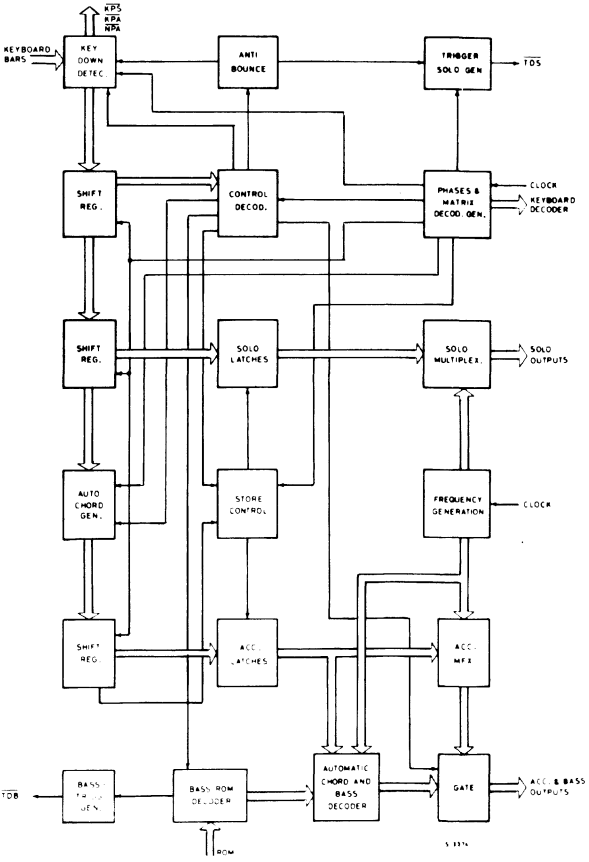
V_{DD}	Source supply voltage	-0.3 to +20	V
V_i	Input voltage	-0.3 to +20	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 50	°C

PIN CONNECTIONS



* V_{SS} is the lowest supply voltage
** V_{DD} is the highest supply voltage

BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The caracteristics of the M208 are similar to those of the M108; the only difference is the keyboard split, which is 24+37 for the M108 and 17+44 for the M208 when used in "accompaniment + solo" mode.

The circuit comprises:

a) 2 pins for clock input: one for the matrix scanning, the other for the incorporated T.O.S.; by connecting both the clock inputs to the same matrix scanning clock (1000.12 KHz), the three "footages" generated are 16', 8' and 4'.

b) 6 inputs from the octave bars (keyboard and control scanning).

c) 3 multiplexed data inputs for addressing the bass selection. These inputs normally come from the outputs of an external memory (negative or positive logic with control inside the chip)

d) 8 signal outputs divided by section: 3 for the "SOLO" section (16', 8', 4'), 4 for the "ACC." section (16' or root, 8' or 3rd, 4' or 5th, 8th/7th according to operating mode), 1 for the bass

e) 12 outputs for the matrix scanning

f) 5 "trigger" and "key down" outputs: $\overline{KPS}$ (key pressed "SOLO"), $\overline{TDS}$ (trigger decay "SOLO"), $\overline{KPA}$ (key pressed "ACC."), $\overline{NPA}$ (pitch present in "ACC." outputs), $\overline{TDB}$ (trigger decay "BASS") respectively. These outputs, in conjunction with an external time constant, allow the formation of the envelope of the sustain and percussion effects. The duration of the trigger pulses is $\cong$ 9 msec.

g) 1 input (reset) to synchronize the device or more than one device (with the same keyboard scanning and using a single contact per key).
The reset action, provided by an external circuit, is of the "POWER ON RESET" (high active) type and its duration must be $\cong$ 0.5 msec.

h) 1 $\overline{TEST}$ pin (in use it must be connected to V_{DD})

i) 2 supply pins.

MATRIX ORGANIZATION (Keyboard and controls)

M108/208 Matrix outputs	M108/208 Octave bar inputs					
	B_1	B_2	B_3	B_4	B_5	B_6
$\overline{F_1}$	C_1	C_2	C_3	C_4	C_5	C_6
$\overline{F_2}$	$C_1\#$	$C_2\#$	$C_3\#$	$C_4\#$	$C_5\#$	7th OFF/7th ON
$\overline{F_3}$	D_1	D_2	D_3	D_4	D_5	3rd+/3rd-
$\overline{F_4}$	$D_1\#$	$D_2\#$	$D_3\#$	$D_4\#$	$D_5\#$	Sust. OFF/Sust. ON
$\overline{F_5}$	E_1	E_2	E_3	E_4	E_5	$\overline{Latch}$/Latch
$\overline{F_6}$	F_1	F_2	F_3	F_4	F_5	Man/Auto
$\overline{F_7}$	$F_1\#$	$F_2\#$	$F_3\#$	$F_4\#$	$F_5\#$	61/24 + 37 (17 + 44)
$\overline{F_8}$	G_1	G_2	G_3	G_4	G_5	Antibounce ON/Antibounce OFF
$\overline{F_9}$	$G_1\#$	$G_2\#$	$G_3\#$	$G_4\#$	$G_5\#$	ROM Low/ROM High
$\overline{F_{10}}$	A_1	A_2	A_3	A_4	A_5	--------
$\overline{F_{11}}$	$A_1\#$	$A_2\#$	$A_3\#$	$A_4\#$	$A_5\#$	--------
$\overline{F_{12}}$	B_1	B_2	B_3	B_4	B_5	--------

C_1 is the first key on the left, C_6 is the last key on the right of the keyboard.

The main feature of this chip is the possibility of formating the keyboard either with 61 keys (only "SOLO" without automatism) or separating it into two sections ("ACCOMPANIMENT + SOLO") with the possibility of chord and bass automatic in the first section.

FEATURES

a) The "61/24 + 37" (17 + 44) control chooses the keyboard operating mode, i.e. the whole keyboard dedicated to "SOLO" or 24 (17) keys dedicated to "ACCOMPANIMENT" and 37 (44) to "SOLO".

b) The "Man/Auto" control, which operates only in case of "ACC.+ SOLO", chooses the manual or the automatic accompaniment.

c) The "Sust OFF/Sust ON" allows the storage of the "SOLO" section and handles the whole keyboard or 37 (44) keys depending on the operating mode.

d) The "$\overline{\text{Latch}}$/Latch" similarly allows the storage of the "ACC." section and operates in "ACC.+ SOLO" only.

e) The "3rd+/3rd-" which operates only in case of "ACC.+ SOLO" and "AUTOMATIC", changes the automatic chord generated from major to minor or viceversa.

f) The "7th OFF/7th ON" adds the seventh to the automatic chord generated.

g) The "Antibounce ON/Antibounce OFF" disables the antibounce circuit which is usually enabled.

h) The "ROM Low/ROM High" selects between ROMs with return to "1" (Low active) or with return to "0" (High active). Usually the chip is enabled for ROMs with return to "1" (Low active).

"SOLO" Operation

In this case the chip recognizes the whole keyboard as "SOLO" and does not read the controls which concern the "ACC.+ SOLO" operation.
The chip identifies all the keys pressed and transfers to the outputs of each section (ACC. and SOLO) the analog sum of corresponding pitches.
The outputs are current generators with average value constant, therefore it is sufficient to connect the pins to one load and send the signals on to the filters.
In the case of "Sustain OFF" each new key pressed or released is accepted or deleted in a time $\leqslant 576\ \mu$sec.
In the case of "Sustain ON" the chip has a different operation according to whether the new key (keys) is pressed or released: each new key pressed is always accepted in a time $\leqslant 576\ \mu$sec., whereas each key released is deleted with a delay of 73 msec. and only if there are still keys pressed.
In fact, if after the 73 msec. there are no keys pressed, the last key (or keys) released remains stored until new keys are pressed.
In this mode it is possible to have Sustain, with external envelope shaping, for the last keys (or key) released.
The pitch envelope is controlled by a D.C. signal $\overline{\text{KPS}}$ (any key pressed) and there is also an A.C. signal $\overline{\text{TDS}}$ (trigger decay "SOLO") which provides a pulse whenever a key is pressed.
An appropriate antibounce circuit, inside the chip, solves the problems associated with the keyboard contacts.

"SOLO + ACCOMPANIMENT" Operation

In this case the chip identifies the "ACCOMPANIMENT" on the first 24 (17) keys on the left, and the "SOLO" on the remaining 37 (44) keys and reads all the controls which concern the "ACC." section. The "SOLO" function is identical to "61 keys" mode, but for the "ACC." section there are two possibilities:

A) **MANUAL**
The chip identifies which keys are pressed in the "ACC." section, and transfers to the "ACC." outputs the analog sum of the corresponding pitches.
The "ACC." section is fully independent of the "SOLO" section and the signals (if there is no "LATCH") remain at the output only while the keys are pressed even if there is "SUSTAIN ON".

The "BASS" section gives at the bass output an alternating bass between the first on the left and the first on the right of the keys pressed in the "ACC." section; the pitch switching timing is dependent on an external ROM (3 bits).
The "LATCH" control stores the last keys released and the output signals, including the bass output, remain until new keys are pressed.
The $\overline{TDB}$ (trigger decay "BASS") output gives a pulse corresponding to every output change; there are also two D.C. signals, $\overline{KPA}$ (any key pressed accompaniment) and $\overline{NPA}$ (pitches in output accompaniment) relative only to the "ACC." section.
The first of these signals (analogous to $\overline{KPS}$) concerns the keyboard and does not consider the "LATCH" condition.
The second on the contrary concerns the "ACC." output and considers the "LATCH" condition.

B) **AUTOMATIC**

The chip recognizes in the "ACC." section only the first on the left of the keys pressed and, according to the setting of the following controls, produces a major or minor chord with or without seventh only the 4' footage but with separated outputs for root, third, fifth and eighth (or seventh if the chord is with seventh).
The bass section gives the bass arpeggio among root, third, fourth, fifth, sixth, seventh and eighth with pitch switching dependent on an external ROM (3 bits).
In automatic mode the two octaves of the "ACC." section inside the chip are connected in parallel both for the chord and for the bass; therefore by pressing anyone of the two keys of the same note the chip generates the same chord.
The "LATCH" control stores the major chord and the bass pitches (until new keys are pressed); the modification of the chord stored (from major to minor, addition of seventh) is always possible by operating the proper controls: by releasing these controls the chord becomes major again.
It is possible to delete the stored pitches both is manual and in "AUTOMATIC" mode by a $\overline{Latch}$ control signal.
Once again there are $\overline{KPA}$, $\overline{NPA}$, and $\overline{TDB}$ information; however the $\overline{TDB}$ pulse, which normally appears at each arrival of the ROM codes, does not appear if there are no pitches in the "ACC." (and bass) outputs or, in the case of alternate bass (in manual mode) if the codes indicate conditions of indifference.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		11.4	12	12.6	V

BASS TRUTH TABLES

LOW ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
1	1	1	No change	No change
1	1	0	Root	1st on the left
1	0	1	3rd	– – –
1	0	0	4th	– – –
0	1	1	5th	1st on the right
0	1	0	6th	– – –
0	0	1	7th	– – –
0	0	0	8th	– – –

HIGH ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
0	0	0	No change	No change
0	0	1	Root	1st on the left
0	1	0	3rd	– – –
0	1	1	4th	– – –
1	0	0	5th	1st on the right
1	0	1	6th	– – –
1	1	0	7th	– – –
1	1	1	8th	– – –

STATIC ELECTRICAL CHARACTERISTICS (Positive Logic, V_{DD}= +10 to +14V, V_{SS}= 0V, T_{amb}= 0 to 50°C unless otherwise specified)

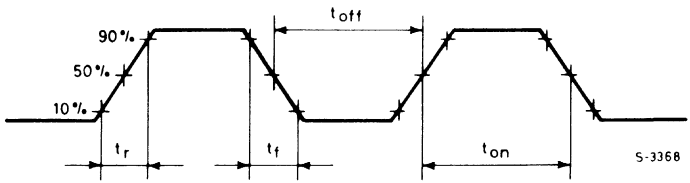
Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input high voltage	Note 1	V_{DD}-1		V_{DD}	V
		Note 2	4		18	V
		Note 3	V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage	Note 1	V_{SS}		V_{SS}+1	V
		Note 2	V_{SS}		V_{SS}+0.6	V
		Note 3	V_{SS}		V_{SS}+2	V
I_{LI}	Input leakage current	V_I= +14V T_{amb}= 25°C			10	µA
LOGIC SIGNAL OUTPUTS						
R_{ON}	Output resistance with respect to V_{SS}			300	500	Ω
R_{ON}	Output resistance with respect to V_{DD}	V_{OUT}= V_{DD}-1 (driver off)		15	25	kΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb}= 25°C		30	45	mA
ANALOG SIGNAL OUTPUTS (the external load must be connected to $V_{DD}/2$)						
I_{OH}	Output current with respect to $V_{DD}/2$	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	35	50	70	µA
I_{OL}	Output current with respect to V_{SS}	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	-35	-50	-70	µA

Npte 1 : Refers only to the clock inputs.
Note 2 : Refers only to the inputs from the external memory.
Note 3 : Refers only to the reset input.

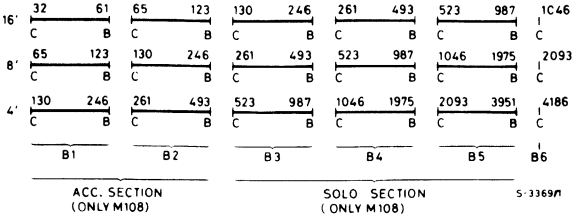
DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MASTER CLOCK INPUT						
f_i	Input clock frequency			1000.12	1100	KHz
t_r, t_f	Input clock rise and fall time 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	1000 KHz		500		ns
T.O.S. CLOCK INPUT						
f_i	Input clock frequency		100	1000.12	2500	KHz
t_r, t_f	Input clock rise and fall times 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2000 KHz		250		ns
$\overline{TDS}$ and $\overline{TDB}$ OUTPUTS						
t_{on}	Pulse duration	1000 KHz		9.216		ms
t_r, t_f	Outputs rise and fall times 10% to 90%	1000 KHz		100		ns

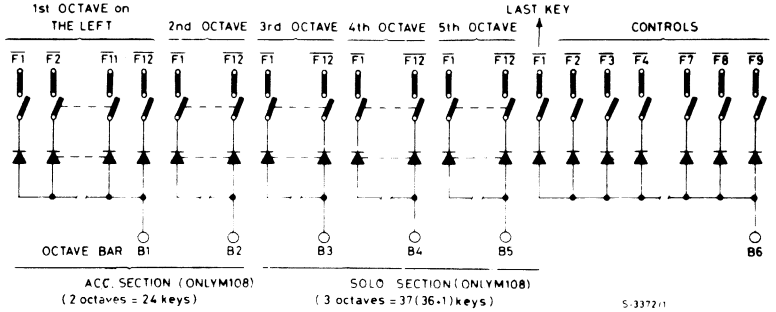
INPUT CLOCK WAVEFORM



FREQUENCY RANGE OF EACH OCTAVE (16', 8', 4' footages)

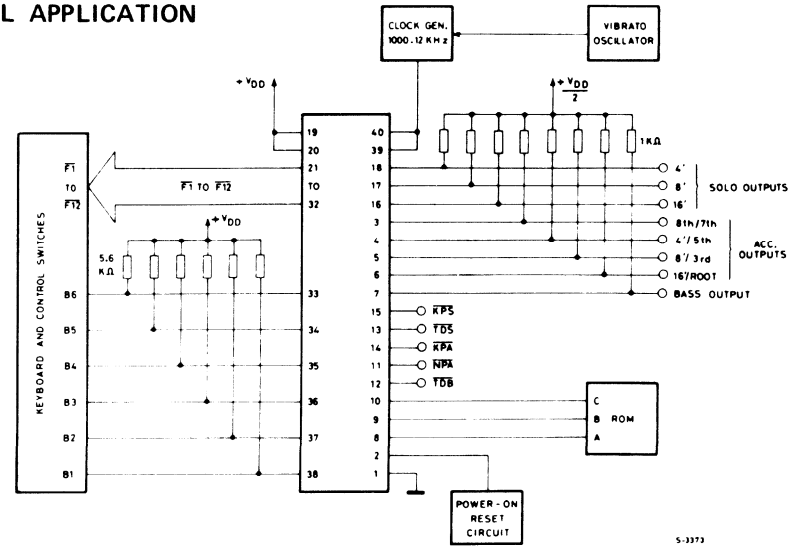


CONNECTION OF THE KEYBOARD AND CONTROL SWITCHES

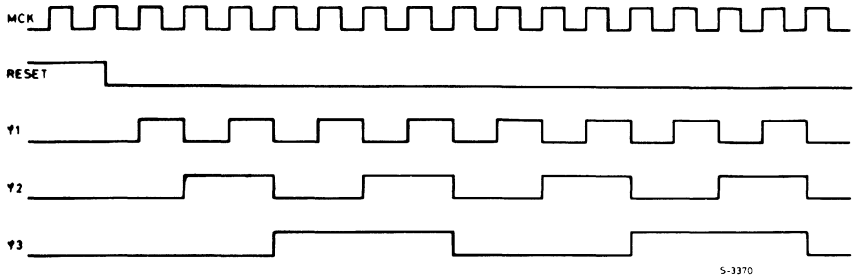


Note: The switch "OPEN" corresponds to "KEY NOT PRESSED" or "CONTROL IN THE FIRST CONDITION" (see the drawing "MATRIX ORGANIZATION").

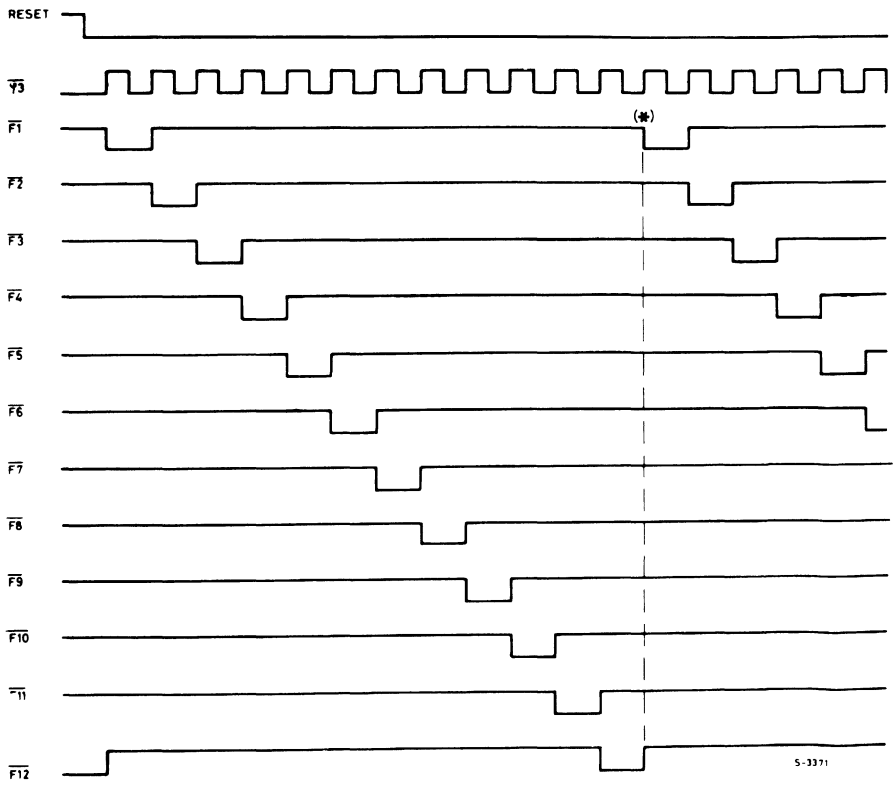
TYPICAL APPLICATION



TIMING DIAGRAMS



Note: MCK is the master clock input (matrix scanning), $\varphi 1$, $\varphi 2$, $\varphi 3$ are internal phases to generate $\overline{F1} \div \overline{F12}$.



Note: The matrix scanning starts (after the power on reset) at the second arrival in output of $\overline{F1}$ (*) from B1 to B6 in continuous sequence.

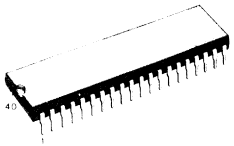
M112

POLYPHONIC SOUND GENERATOR

- 8μP PROGRAMMABLE SOUND GENERATOR CHANNELS
- 2MHz CLOCK
- INTERNAL TOS WITH POSSIBILITY OF EXTERNAL SYNCHRONIZATION FOR MULTICHIP USE
- 6 COMPLETE OCTAVE KEYBOARDS (72 KEYS)
- FIVE HOMOGENEOUS FOOTAGES μP PROGRAMMABLE BY ADDING A CONSTANT K TO THE KEYBOARD SITUATION
- SEVEN OCTAVE RELATED OUTPUTS ENVELOPED WITHOUT CONSTANT DC LEVEL (4 FOOTAGES)
- SEVEN FOOTAGE RELATED OUTPUTS WITH DIFFERENT CONFIGURATIONS FOR :

– FOOTAGES WITH ENVELOPE (WITHOUT CONSTANT DC LEVEL) AND:
– FOOTAGES WITHOUT ENVELOPE (WITH CONSTANT DC LEVEL) AND:
– VARIOUS SOUND CHANNEL DIVISIONS (SEE OPTION I, II AND III)

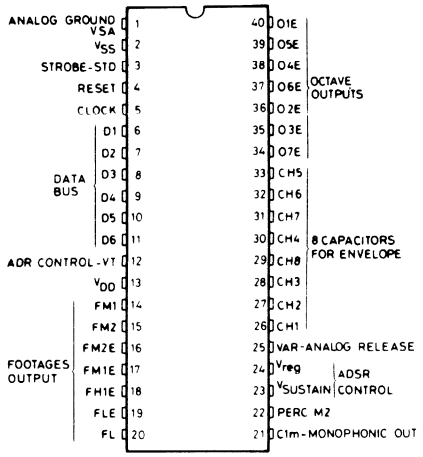
- POSSIBILITY OF EXCLUDING ONE OR MORE SOUND CHANNELS FROM THE NON ENVELOPED FOOTAGE OUTPUTS
- ONE MONOPHONIC OUTPUT NON ENVELOPED RELATED TO SOUND CHANNEL 1 WITH THE POSSIBILITY OF CHOOSING THE FOOTAGE (TWO ADDITIONAL MONOPHONIC OUTPUTS ON OPTION II)
- 50% DUTY CYCLE ON ALL OUTPUTS
- DIGITAL DRAWBAR CONTROL (32 LEVELS)
- ATTACK - DECAY - SUSTAIN - RELEASE (ADSR) ENVELOPE DEFINITION WITH DIGITAL CONTROL ON A.D.R. AND ANALOG CONTROL ON S
- ADDITIONAL ANALOG CONTROL ON RELEASE
- ANALOG PERCUSSION INPUT TO ENVELOPE ONE FOOTAGE (M2) ON THE OCTAVE RELATED OUTPUTS
- SPECIAL EXTERNAL ENVELOPE POSSIBILITY USING HOLD AND/OR RELEASE ∞
  HOLD AND RELEASE ∞ ARE DEDICATED TO DECAY AND PEDAL EFFECT
- N-CHANNEL TECHNOLOGY - 12V SINGLE SUPPLY.



DIP-40 Plastic

ORDERING NUMBER: M112B1

PIN CONNECTION



The M112 is a polyphonic sound generator that combines eight generators with envelope shapers and drawbar circuitry in a single package.
This versatile circuit simplifies the design of a wide range of polyphonic instruments and, interfacing directly with a microcomputer chip, gives designers an unprecedented degree of flexibility. The M112 is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology. It is available in a 40 lead plastic package.

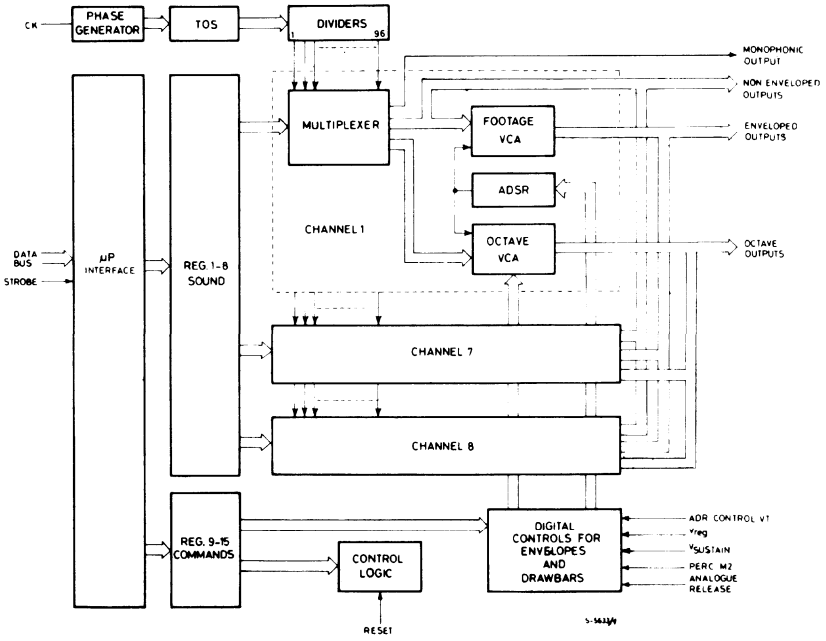
ABSOLUTE MAXIMUM RATINGS

V_{DD} *	Supply voltage	-0.3 to 20	V
V_i	Input voltage	-0.3 to V_{DD}	
$V_{O\ (off)}$	Off state output voltage	-0.3 to 20	V
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Rarings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* All voltages are with respect to V_{SS}.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{DD}	Highest Supply Voltage		11.4	12	12.6	V

STATIC ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input High Voltage	Pins 3, 6 to 11	2.4		V_{DD}	V
		All other inputs	6		V_{DD}	V
V_{IL}	Input Low Voltage	Pins 3, 6 to 11	-0.3		0.8	V
		All other inputs	-0.3		1	V
VSA	Analog Ground	R < 10Ω C = 100μF	0	0	1	V
VT	ADR Control Time	R = 1K C = 1μF	0		V_{DD}	V
VAR	Analog Release	R = 10K C = 0.1μ	0		V_{DD}	V
V_{reg}	Control OFF Asymptote	R < 10Ω C = 100μ	0	0	1	V
$V_{SUST.}$	Control Level Sustain	R = 1K C = 100μ	0		V_{DD}	V
Perc. M2	Control Level Percussion	R = 10K	0		V_{DD}	V
I_{LI}	Input Leakage Current	$V_I = V_{DD}$			1	μA
OUTPUT SIGNALS (One key pressed)						
I_{OL}	Output Low current	$V_{OL} = V_{DD/2-1V}$ (note 1)	10	30	50	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD/2+1V}$ (note 1)	10	30	50	μA
		V_{OH} = 10V (note 2)	100	300	500	μA
		V_{OH} = 10V	10	30	50	μA
$I_{O(off)}$	Off state output current	$V_O = V_{DD}$ (all output pins)			1	μA
		$V_O = V_{SS}$ (pins 14-15-20 in 3rd state)			-1	μA
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb} = 25°C			50	mA

Notes: 1. Refers only to FL, FM1, FM2 (pins 20, 15, 14).
2. Refers only to octave outputs with drawbar max.

DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK						
f_i	Input Clock Frequency		250	2000.24	2.300	kHz
t_r, t_f	Rise and Fall Times 10% to 90%				30	ns
t_{on}, t_{off}	ON and OFF Times		150			ns
RESET						
t_w	Pulse Width	Clock = 2 MHz	10			μs
t_f	Fall Time				30	ns
OUTPUT SIGNALS						
t_{on}, t_{off}	Outptu duty cycle			50		%

M112

GENERAL DESCRIPTION

The M112 contains a microprocessor interface, eight programmable sound generator channels, a top octave synthesiser, a divider chain and control circuitry, (see fig. 1). Each generator consists of logic to select the desired notes and harmonics from 96 frequencies obtained by division, an ADSR envelope generator and two voltage-controlled amplifiers. Programmable attenuators are included for drawbar control of the harmonic content of the sound.

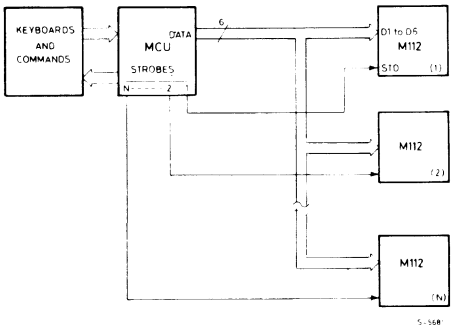
To simplify system design the signals generated in each channel are directed to octave separated outputs and footage outputs. Two voltage-controlled amplifiers are provided for each channel to keep the octave and footage outputs separate.

The attack time, decay time, release time and sustain level are set for all eight channels by common controls. Tone selection, the attack, decay, release parameters, drawbars and special effects are all software controlled.

In a typical configuration (fig. 2), one or more M112s are connected to a microprocessor which scans the keyboard and front panel controls in a matrix arrangement. When the microprocessor detects a key depression it chooses one of the sound generators and allocates it to that note. If another key is pressed the microprocessor allocates another sound generator and so on. This process can be repeated until there are no more free channels, i.e. when 8N keys are pressed simultaneously where N is the number of M112s used.

When one of the keys is released the microprocessor resets a control bit in the appropriate generator channel which will then be re-allocated to another key when needed.

Fig. 2



OUTPUTS

The M112 has 15 music output pins. Seven of these are octave outputs, seven are footage outputs and the last is a monophonic output from channel one. This standard configuration can be changed under program control.

The octave outputs, which are enveloped, are so called because there is one output for each octave, i.e. output signals from all eight channels that fall within the same octave are routed to the same output. These outputs are provided to simplify the generation of sinewaves from the squarewaves generated by the M112s digital circuitry. Since each of these outputs handles a limited range of frequencies – exactly one octave – a simple low pass or bandpass filter will do the job. The blend of harmonics sent to the octave outputs is controlled by the drawbar attenuators.

The footage outputs are related to the five footages generated by the M112. These are referred to as L, M1, M2, H1 and H2 (L = Low, M = mid, H = high) and can be programmed to give the three different ranges given in table 1, adding a constant K (number of half tones) to the keyboard information.

All five footages can be obtained from these outputs but only four are mixed by the drawbar circuitry and routed to the octave outputs.

TABLE 1 - THE THREE FOOTAGE RANGES OF THE M112

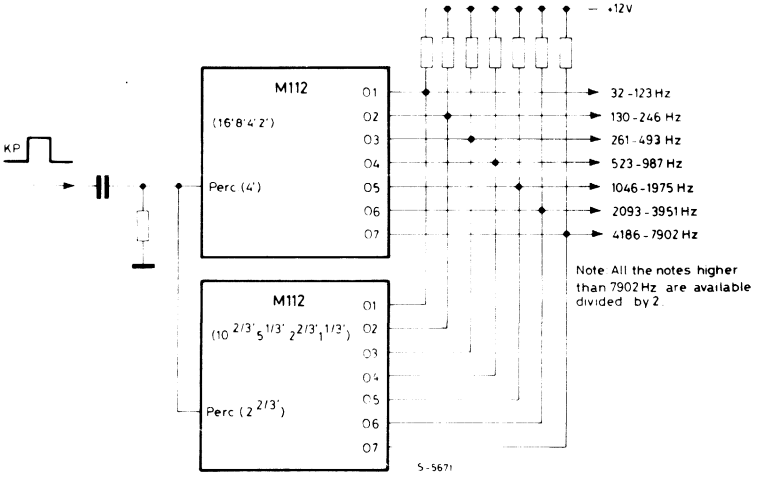
Enveloped footage outputs (option 2)

Octave outputs

Non Enveloped Footage Outputs

Footage / K	L	M1	M2	H1	H2
0	16'	8'	4'	2'	1'
7	$10\ 2/3'$	$5\ 1/3'$	$2\ 2/3'$	$1\ 1/3'$	2/3'
4	$12\ 4/5'$	$6\ 2/5'$	$3\ 1/5'$	$1\ 3/5'$	4/5'

Fig. 3 - Example of octave related output "EVEN" and "ODD" with Percussion input.



In no case will the maximum frequency be higher than 7902 Hz (with a 2 MHz clock).
The output configuration for the octave and footage outputs can be changed under program control as mentioned above. There are three options, including the standard configuration, and these are:

- Option 1, the normal configuration gives four enveloped footage outputs, LE, M1E, M2E, H1E, and three non-enveloped outputs, L, M1 and M2. All eight channels are present on each output.
- Option 2 is a special configuration for sawtooth generation (sawtooth waveforms are frequently used in sound synthesis). In this case channels two and three appear **only** on the outputs FM1 and FM2 (footages M1 and M2) and are excluded from the rest. All five footages are available as enveloped outputs.
- Option 3 is intended for sophisticated automatic accompaniment circuits. All the channels appear on three non-enveloped outputs (FL, FM1, FM2) for chord generation and can be disconnected or command. Channels 4, 5, 6 and 7 appear on four enveloped outputs for arpeggi. The octave outputs are used for the bass and include only channel 8.

TABLE 2 - OUTPUT CONFIGURATIONS

Pin	Option I	Option II	Option III	Option IV
15	FM2	FM2 (Channel 3)	FM2 — All channels (see note 3)	FM2 (Ch. 3)
14	FM1	FM1 (Channel 2)	FM1 — All channels (see note 3)	FM1 (Ch. 2)
20	FL	FH2E	FL — All channels (see note 3)	FH2E (Ch. 4, 5, 6, 7, 8)
18	FH1E	FH1E	FH1E	FH1E
16	FM2E	FM2E	FM2E — only channels 4-5-6-7	FM2E — only channels 4-5-6-7
17	FM1E	FM1E	FM1E — only channels 4-5-6-7	FM1E — only channels 4-5-6-7
19	FLE — For the 8 channels	FLE	FLE — only channels 4-5-6-7	FLE
40	O1E — For the 8 channels	O1E — Only channels 1-4-5-6-7-8	O1E	O1E
36	O2E — For the 8 channels	O2E — Only channels 1-4-5-6-7-8	O2E	O2E
35	O3E — For the 8 channels	O3E — Only channels 1-4-5-6-7-8	O3E	O3E
38	O4E — For the 8 channels	O4E — Only channels 1-4-5-6-7-8	O4E — only channel 8	O4E — only channel 8
39	O5E — For the 8 channels	O5E — Only channels 1-4-5-6-7-8	O5E	O5E
37	O6E — For the 8 channels	O6E — Only channels 1-4-5-6-7-8	O6E	O6E
34	O7E — For the 8 channels	O7E — Only channels 1-4-5-6-7-8	O7E	O7E
21	Monophonic out (channel 1)	Mono (channel 1)	Mono (channel 1)	Mono (channel 1)
	Standard use	Special for sawtooth generation etc.	Special for high class accompaniment	Only for information (no musical meaning)

– FL, FM1, FM2 are footage outputs not enveloped (with constant DC level)
– FLE, FM1E, FM2E, FH1E, FH2E are enveloped (without constant DC level).

Notes: 1) H2 is available only in option 2 on FH2 enveloped outputs. It is not available on octave related outputs.

2) In the option 2 the Sound channels 2 and 3 are available only on pins 14 and 15 and consequently are excluded from the other outputs.

3) Each channel can be disconnected with commands NC1 to NC8 (register 10).

DRAWBARS AND EFFECTS

One of the significant features of the M112 is the implementation of drawbar control circuitry. This consists of four programmable attenuators, one for each of the footages routed to the octave outputs, which are used to blend harmonics to produce the desired sound.

Other features of the M112 include hold, pedal and percussion effects, all of which are enabled/disabled under software control. Hold, when active, interrupts the decay of the ADSR envelope and Pedal interrupts the release curve. Hold and pedal permit external control of the envelope. This feature can be used, for example, to synthesize very realistic piano and harpisichord sounds.

A piano effect can be produced by suitably programming the envelope shapers but by using the hold and pedal controls and a few external components much greater realism can be obtained. Fig. 4 shows a simplified schematic of one of the envelope shapers together with the type of envelope generated. The envelope parameters are controlled by RA, RD, RR and V_{SUS} (RA, RD and RR are programmed resistors controlling attack, decay and release). Disabling the natural decay and release and adding a handful of components a close approximation to the ideal waveform can be produced (fig. 5). R1 is a very large resistance (typically 3 MΩ) to give the long (several seconds) time constant for the second decay.

Fig. 4 - With an external capacitor the M112's envelope shapers produce the standard ADSR envelope.

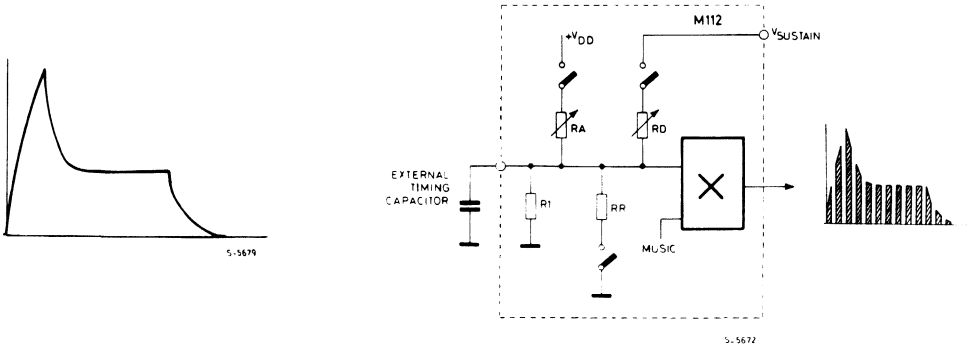
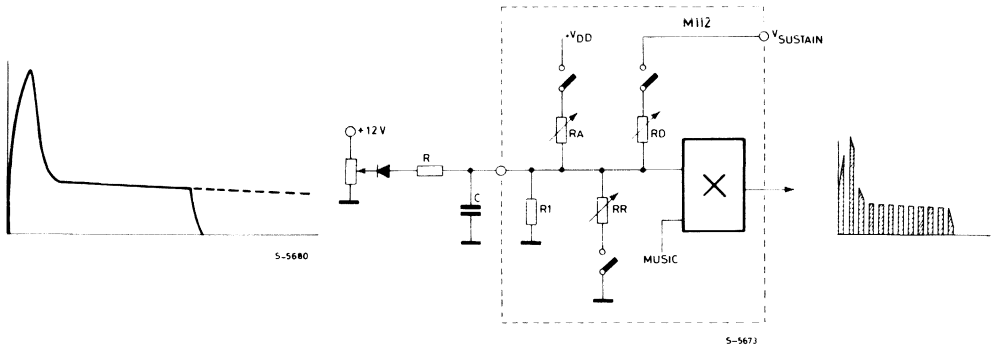


Fig. 5 - Disabling the normal decay and release and adding a few external components a realistic piano envelope can be produced.



INPUTS

Eight pins on the M112 are used to define the elementary time interval of the ADSR envelope shapers (Pins 26 to 33). Capacitors, nominally 1μF, are connected to these pins. Eight separate capacitors are necessary because the envelope shapers are independently triggered. Analog inputs are also provided to adjust the asymptotic release level (V_{reg} pin 24) and the charge/discharge current for attack, decay and release (VT pin 12) in order to compensate the differences of ADR time constant between several M112s used in the same instrument.
The sustain level is fixed by the voltage at pin 23.
The release time constant, digitally controlled by software, can also be fine adjusted by a trimmer connected at pin 25.

PROGRAMMING

The M112 is programmed using five basic commands:

- CHANNEL PROGRAM
- ADSR PROGRAM
- NON-ENVELOPED OUTPUT MASK
- LOAD CONTROL REGISTER
- DRAWBAR PROGRAM

These commands all consist of 12 bits transferred to the M112 (or one of the M112s) in two six-bit bytes through six data lines. Data is latched into the M112 synchronously by a strobe signal. The M112 can be connected directly to an M387X series microcomputer.
Each command contains the address of the Register in which data is to be memorized (there are 16 registers) and the data.

Channel program commands consist of the channel code (4 bits), octave code (3 bits), note code (4 bits) and a control bit, KP (key pressed). KP must be set if the key has just been pressed and reset if the note has just been released.

D1					D6
CHANNEL				KP	O2
O1	O0	NOTE			

CHANNEL PROGRAM

Resetting KP does not necessarily silence the channel because the sound continues after the key has been released if the release time is non-zero. To stop a channel completely the unused note and octave codes are used.

If an unused note code is programmed the channel is turned off with the output transistor in the ON state and if an unused octave code is used the channel is turned off with the output transistor in the OFF state. Six octave codes and twelve note codes are recognized, giving a keyboard span of 72 keys.

For example, to tell an M112 that channel three is to play F# in the third octave the command is:

D1					D6
0	0	1	0	1	0
1	1	0	1	1	0

CHANNEL 3 CODE IS 0010
OCTAVE 3 CODE IS 011
F # NOTE CODE IS 0110
KP IS SET

The ADSR Program command sets the attack, decay and release times for all the envelope shapers. This command takes the form:

D1					D6
1	0	0	0	r3	r2
r1	d2	d1	a3	a2	a1

ADSR PROGRAM

The code 1000 selects the ADSR control register, a3/a2/a1 is the attack time, d2/d1 is the decay time and r3/r2/r1 is the relase time. These times are all multiples of the time interval set by external capacitors. With the suggested 1μF values this time interval is 15ms. The release code 000 is used to enable the pedal effect.

The Non-Enveloped Output Mask command is used to select which channels are to be routed to the non-enveloped footage outputs. Any or all of the eight channels can be excluded by setting the appropriate bit.

D1					D6
1	0	0	1	NC8	NC7
NC6	NC5	NC4	NC3	NC2	NC1

OUTPUT MASK

The Load Control Register command selects the footage and output options and enables/disables the hold and percussion facilities.

D1					D6
1	0	1	0		PO
HOLD	OP3	OP2	NC1m	m2	m1

LOAD CONTROL REGISTER

"NC1m" is a control bit that excludes channel one from all outputs except the three non-enveloped footages outputs. PO is the percussion disable bit, m2/m1 is the footage option select code for the monophonic output and OP2/OP1 the output configuration select code.

The drawbar-controlled attenuators are set independently for each footage using the Drawbar Program Command which has the form:

D1							D6
FOOTAGE							
	ATTENUATION						

DRAWBAR PROGRAM

Footage is selected by addressing registers R12 to R15.
Attenuation is controlled in 32 linear steps which can be conveniently reduced to the conventional 16 or 8-step logarithmic scale using a lookup table.

APPLICATIONS

The M112 is intended for a wide range of applications ranging from simple single-keyboard organs to 2-3 manual instruments with sophisticated synthesis and accompaniment facilities. It can also be used in electronic pianos, harpsichords, string synthesizers etc.

DESCRIPTION

Pin 1 - VSA Analog ground

Ground connection of all outputs. It is typically connected to V_{SS}. By adjusting its value with respect to V_{SS} (plus/minus) it is possible to modify the output current and compensate the differences in current between several M112s used in the same applications.

Pins 2 and 13 - V_{SS}, V_{DD}

Power supply connections. V_{DD} is nominally 12V; V_{SS} is to be connected to GND.

Pin 4 - Reset input

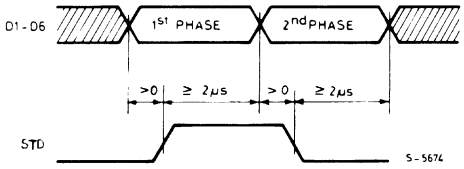
It is used to synchronize various M112s in multichip use. The reset is activated when the input is at H Level. In this condition the chip is blocked.

Pin 5 - Clock input

It has to be connected to an external oscillator of 2 MHz.

Pin 6 to 11 - D1, D6 Data bus input
Pin 3 - STD Data Strobe input

These pins are used to transfer the 12 bits of data from the microprocessor to the registers of various M112s using a two phase procedure.
The first six bits of data are latched on the positive edge of STD, while the other six bits are latched on the negative edge of STD.



Each 2 x 6 bit of information contains the address of the register (4 bit/16 registers) and the data up to 8 bits to be memorized in the selected register.

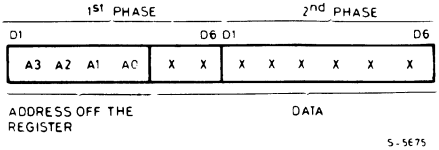


TABLE 3 - REGISTER SELECTION

A0	A1	A2	A3	Register n°	Register function
0	0	0	0	1	
1	0	0	0	2	
0	1	0	0	3	
1	1	0	0	4	Note-octave etc.
0	0	1	0	5	For Sound channel
1	0	1	0	6	
0	1	1	0	7	
1	1	1	0	8	
0	0	0	1	9	
1	0	0	1	10	
0	1	0	1	11	
1	1	0	1	12	Control Commands
0	0	1	1	13	
1	0	1	1	14	
0	1	1	1	15	
1	1	1	1	16	Used for test*

* This address sets the Ic in a test condition that can only be modified by a Reset command on pin 4.

Registers 1 to 8

There registers are related to the sound channels

	Bus	Data	
PHASE 1	D1	A3	must be "0"
	D2	A2	Sound
	D3	A1	Channel
	D4	A0	Selection
	D5	KP	
	D6	O2	
PHASE 2	D1	O1	Key
	D2	O0	information
	D3	N3	
	D4	N2	
	D5	N1	
	D6	N0	

A0-A2: Sound channel selection with reference to table 3, register 1 is related to channel 1, register 2 to channel 2 and so on up to channel 8.

KP : 1 = pressed key 0 = relased key
O0-O1-O2: Octave code of the note (Table 4).

TABLE 4

O0	O1	O2	Code	Octave	
0	0	0	0		Note OFF
1	0	0	1	1	
0	1	0	2	2	
1	1	0	3	3	
0	0	1	4	4	
1	0	1	5	5	
0	1	1	6	6	
1	1	1	7		Note OFF

Output transistor "OFF"

N0-N1-N2-N3 = Note Code (Table 5)

TABLE 5

N0	N1	N2	N3	Code	Note
0	0	0	0	0	DO
1	0	0	0	1	DO#
0	1	0	0	2	RE
1	1	0	0	3	RE#
0	0	1	0	4	MI
1	0	1	0	5	FA
0	1	1	0	6	FA#
1	1	1	0	7	SOL
0	0	0	1	8	SOL#
1	0	0	1	9	LA
0	1	0	1	10	LA#
1	1	0	1	11	SI
0	0	1	1	12	Note "OFF"
1	0	1	1	13	Note "OFF"
0	1	1	1	14	Note "OFF"
1	1	1	1	15	Note "OFF"

Output transistor "ON"

Register 9 to 15

These registers are related to the various control commands

TABLE 6

	Register / Data Bus	R9	R10	R11	R12	R13	R14	R15	R16
PHASE 1	D1	1	1	1	1	1	1	1	1
	D2	0	0	0	0	1	1	1	1
	D3	0	0	1	1	0	0	1	1
	D4	0	1	0	1	0	1	0	1
	D5	r3	NC8	X	X	X	X	X	X
	D6	r2	NC7	PO	X	X	X	X	X
PHASE 2	D1	r1	NC6	HOLD	X	X	X	X	X
	D2	d2	NC5	OP3	L5	M1 5	M2 5	H1 5	X
	D3	d1	NC4	OP2	L4	M1 4	M2 4	H1 4	X
	D4	a3	NC3	NC1m	L3	M1 3	M2 3	H1 3	X
	D5	a2	NC2	m2	L2	M1 2	M2 2	H1 2	X
	D6	a1	NC1	m1	L1	M1 1	M2 1	H1 1	X
		Envelope	Channel off	Various	Drawbar level on four footages only for octave outputs				Test

Register 9 - R9 selects the ADR envelope parameters for ADSR control (see fig. 6)

Attack – a1 - a2 - a3 = 3 bit
Decay – d1 - d2 = 2 bit
Release – r1 - r2 - r3 = 3 bit
} 8 bit

Fig. 6 - ADSR envelope control

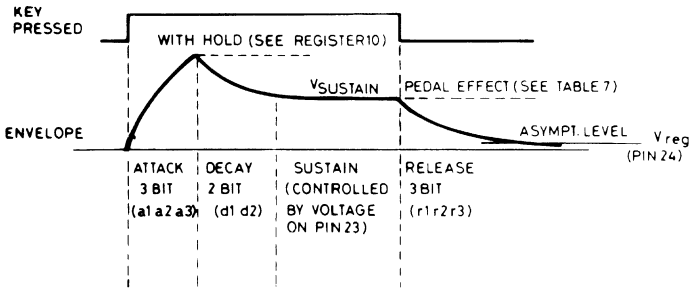


Table 7 shows the various time constants for Attack, Decay and Release.

TABLE 7

a3	a2	a1	Attack		
	d2	d1		Decay	
r3	r2	r1			-Release
0	0	0	T/2	4T	* ∞
0	0	1	T	8T	T
0	1	0	2T	16T	2T
0	1	1	4T	32T	4T
1	0	0	8T		8T
1	0	1	16T		16T
1	1	0	32T		32T
1	1	1	64T		64T

* In this case it is possible to obtain the pedal effect.
T = 3 ms is the typical time constant unit with 8 external capacitors of 1 μF connected to pins 26 to 33.

Register 10 - Contains 8 commands to exclude the corresponding sound channel from the non-enveloped footage outputs (FL-FM1-FM2)
0 = ON 1 = OFF

Register 11 - Contains the following 8 commands: m1 and m2 select one of the four footages available for the monophonic output (C1m) according to table 8.

TABLE 8

m1		0	1	0	1
m2		0	0	1	1
K	0	16′	8′	4′	2′
	7	10 2/3′	5 1/3′	2 2/3′	1 1/3′
	4	12 4/5′	6 2/5′	3 1/5′	1 3/5′

OP2-OP3 – Select the four output options described in table 1 according to table 9.

TABLE 9

BIT / OPTION	OP2	OP3
I	0	0
II	1	0
III	0	1
IV	1	1

HOLD - If 0, disconnects the external 8 capacitors of envelope (1 μF) and the $V_{SUSTAIN}$ pin (pin 23) in the decay phase.

PO (Percussion Off) - If 1, the percussion input is inhibited (see pin 22 description).

NC1m-If1, eliminates channel 1 from all outputs except the 3 footage outputs not enveloped (it can be eliminated from these outputs through the command NC1 of register 10).

N.B. NC1m command is inoperative on the monophonic output (C1m) where channel 1 is always present.

Registers 12-13-14-15

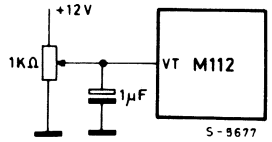
These registers contain the drawbar control for 4 footages on the octave related output.
Footages L, M1, M2 and H1 are controlled in 32 linear levels or for example, using conversion table in the microprocessor in 8 or 16 logarithmic levels.
Table 10 shows an example of footage L with 32, 16 and 8 step control in dB.

TABLE 10

L 5	L 4	L 3	L 2	L 1	Attenuation in dB		
					32 steps	16 steps	8 steps
0	0	0	0	0	OFF	OFF	OFF
0	0	0	0	1	-29.8	-29.8	-29.8
0	0	0	1	0	-23.8	-23.8	-23.8
0	0	0	1	1	-20.3	-20.3	-20.3
0	0	1	0	0	-17.8	-17.8	
0	0	1	0	1	-15.8	-15.8	
0	0	1	1	0	-14.3	-14.3	-14.3
0	0	1	1	1	-12.9		
0	1	0	0	0	-11.8	-11.8	
0	1	0	0	1	-10.7		
0	1	0	1	0	-9.8	-9.8	
0	1	0	1	1	-9.0		-9.0
0	1	1	0	0	-8.2	-8.2	
0	1	1	0	1	-7.5		
0	1	1	1	0	-6.9	-6.9	
0	1	1	1	1	-6.3		
1	0	0	0	0	-5.7	-5.7	
1	0	0	0	1	-5.2		
1	0	0	1	0	-4.7		
1	0	0	1	1	-4.2	-4.2	-4.2
1	0	1	0	0	-3.8		
1	0	1	0	1	-3.4		
1	0	1	1	0	-3.0	-3.0	
1	0	1	1	1	-2.6		
1	1	0	0	0	-2.2		
1	1	0	0	1	-1.9		
1	1	0	1	0	-1.5	-1.5	
1	1	0	1	1	-1.2		
1	1	1	0	0	-0.9		
1	1	1	0	1	-0.58		
1	1	1	1	0	-0.29		
1	1	1	1	1	0	0	0

Pin 12 - VT - ADR Control

It is used to adjust the ADR time constant for several M112s used in the same application. Using a single M112 it has to be connected to V_{DD}.



Pin 14 to 20 - FM1, FM2, FM2E, FM1E, FH1E, FLE, FL (Footages output)

The "wired-or" function is possible on all outputs.
The non enveloped outputs (with constant DC level) are push-pull current generators.
The enveloped outputs (with non constant DC level) are open drain sink current generators. Output duty cycle is 50%.

Pin 21 - C1m

Monophonic output of channel 1 (always present). Duty cycle of the waveform is 50%.

Pin 22 - Percussion M2

Using a specific signal on this input it is possible to have a percussion effect on M2 footage for the octave related output.

Pin 23 - $V_{SUSTAIN}$

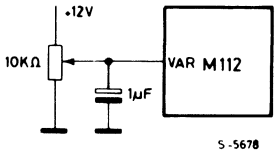
This input defines the level of sustain (see fig. 6).

Pin 24 - V_{reg}

This pin controls the asymptote of $V_{RELEASE}$ through the gate of a transistor which discharges the envelope capacitor. If the performance at the end of release time is considered satisfactory, this pin must be connected to V_{SS}. Otherwise this input can be connected to a voltage not higher than 1V.

Pin 25 - VAR Analog release

This pin is intended for analog control of the release time constant when it is required in addition to the digital one controlled by software.



It allows intermediate values not included in table 7 (see explanation of register 9). In the case of pedal effect connect this input to V_{SS}.

Pin 26 to 33 - CH1, CH8 Envelope capacitor inputs

8 capacitors (typical value = 1μF) have to be connected for the ADSR envelopes.

Pin 34 to 40 - O1E, O7E Octave Outputs

Octave related outputs. Duty cycle is 50%.

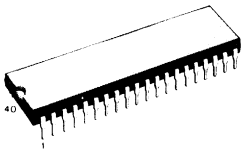
SGS Technology and Service

M114A

ADVANCE DATA

DIGITAL SOUND GENERATOR

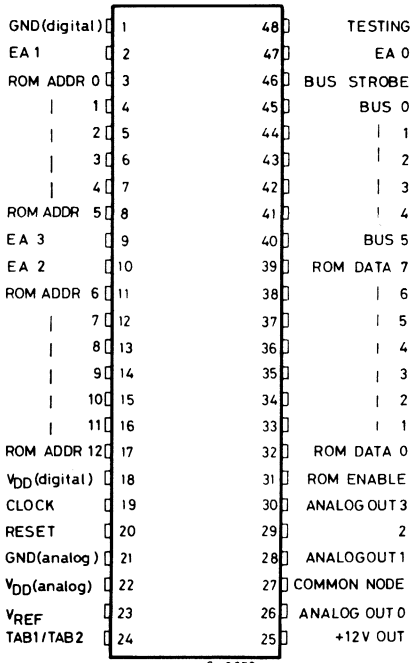
- MAX EXTERNAL ADDRESSING MEMORY OF 256K
- 16 INDEPENDENT CHANNELS
- 12 BIT EQUIVALENT D/A CONVERTER RESOLUTION (DELTA MODULATION)
- SOUND GENERATED BY READING TABLES CODED IN DELTA MODULATION OR IN ABSOLUTE VALUES, SITUATED IN AN EXTERNAL MEMORY
- 8 DIFFERENT TABLE LENGHTS AND 8 READING MODES GIVING A TOTAL OF 58 DISTINCT COMBINATIONS
- 16 DIFFERENT MIXABLE LAYERS BETWEEN TWO SEPARATE TABLES
- MULTIPLE READING PERMITS INTERPOLATION BETWEEN TWO ADJOINING SAMPLES ON THE SAME TABLE
- 4 SELECTABLE ANALOG OUTPUTS
- 10 BIT INTERNAL ATTENUATOR WITH GRADUAL AMPLITUDE VARIATION
- ROM ENABLE OUTPUT TO MINIMISE EXTERNAL MEMORY POWER CONSUMPTION
- POSSIBILITY OF SYNCHRONOUS AND ASYNCHRONOUS FREQUENCY-TABLE CHANGE AT THE END OF THE READING TABLE



DIP-48 Plastic

ORDERING NUMBER: M114A-B1

CONNECTION DIAGRAM



The M114A is a 16 channels digital polyphonic, politimbric sound generator.

The M114A must be driven by a microprocessor and needs an external memory.

With this device it is possible to synthesize a large range of sound by simply transcribing the most significant periods of the sound to be reproduced into an external memory and programming a suitable reading sequence for these periods with the use of a microprocessor.

The M114A is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology and is assembled in plastic DIP.48.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 7	V
V_I	Input voltage	-0.3 to V_{DD}	V
V_O	Output voltage	-0.3 to V_{DD}	V
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - Block Diagram

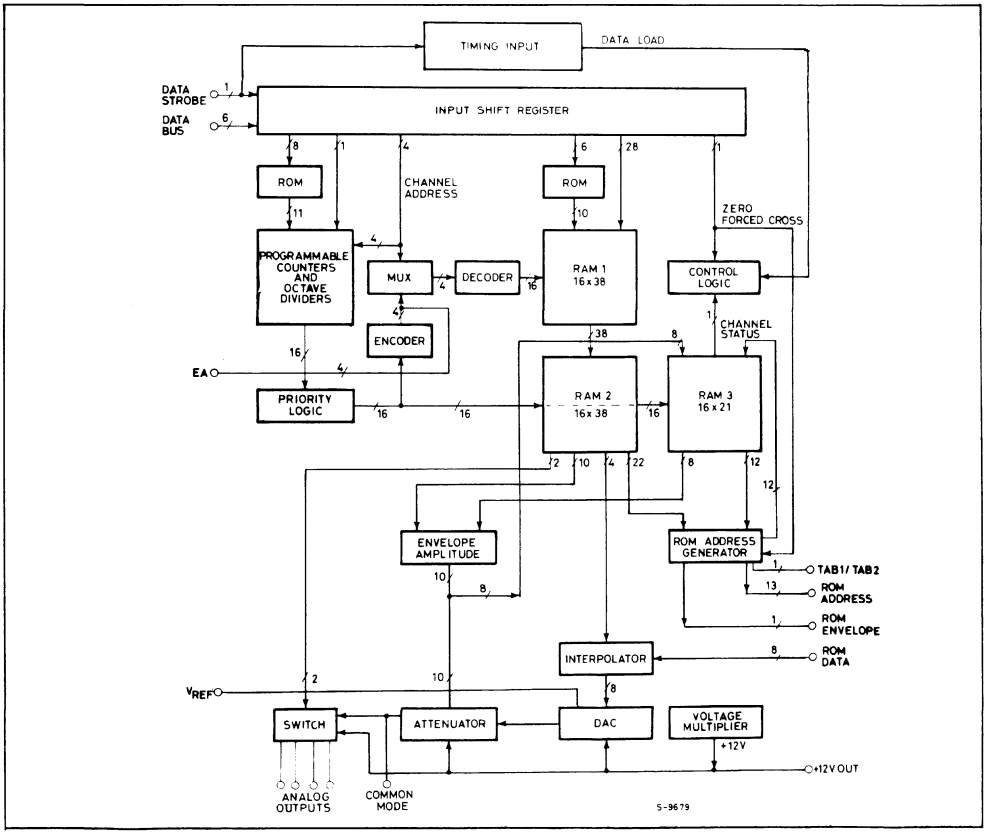
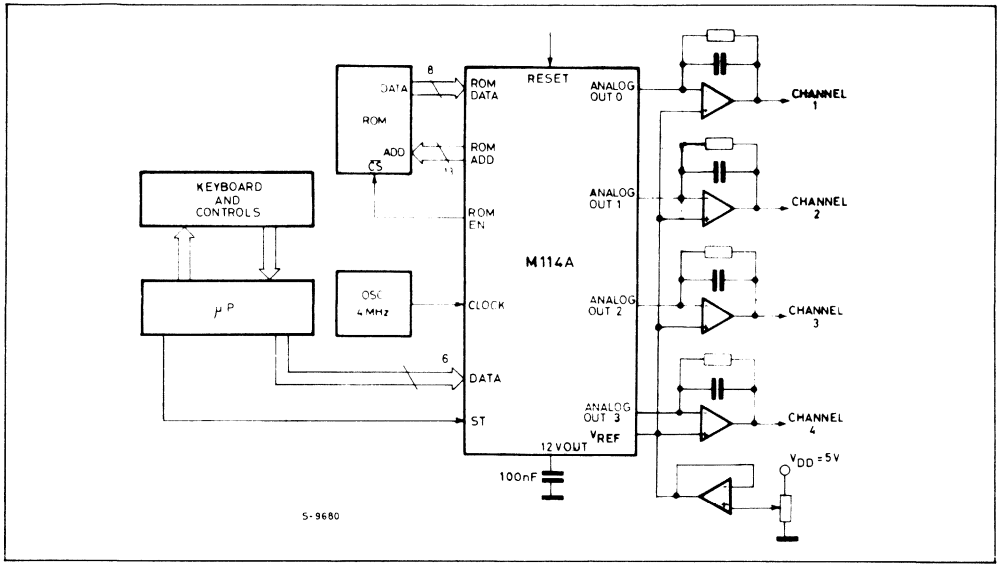


Fig. 2 - System Configuration



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 5%, V_{SS} = 0, T_{amb} = 0/70°C, V_{DD} DIG = V_{DD} Analog)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
INPUTS: RESET (pin 20), CLOCK (pin 19), ROM DATA (pins 32-39), DATA BUS (pins 40-45), DATA ST. (pin 46)						
V_{IL}	Low Input Level				0.8	V
V_{IH}	High Input Level		2.2			V
I_I	Input Leakage Current	$V_I = V_{DD}$ to V_{SS}			± 1	μA
DIGITAL OUTPUTS (HIGH IMPEDANCE* with 10 KΩ pull-up): ROM-ADD (pins 3-8; 11-17), EA (pins 2, 9, 10, 47), ROM EN. (pin 31)						
V_{OL}	Low Output Level	I_{OL} = 1 mA			0.4	V
V_{OH}	High Output Level	I_{OH} = 100 μA	2.4			V
ANALOG OUTPUTS: (pins 26, 28,29, 30), V_{REF} (pin 23)						
V_{REF}	Voltage Reference Output	I_O = ± 1 mA		2.5		V
I_O	Output Current (current generator)	Zero attenuation Max input code to the DAC		± 1		mA
POWER DISSIPATION						
I_{DD}	Supply Current	V_{DD} = 5.25V			100	mA

* High impedance means that, when the addresses are off, the digital output is connected with an internal resistive pull-up.

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLOCK						
t_{CK}	Input Clock Frequency			4.000		KHz
t_r, t_f	Rise and Fall Time	10% to 90%			20	ns
t_{WH}, t_{WL}	High and Low Pulse Width		80			ns
RESET						
t_W	Pulse Width	Clock = 4 MHz	10			μs
t_f	Fall Time	10% to 90%			20	ns
DATA BUS						
t_W	Pulse Width		750			ns
t_{set-up}	Set-up Time to DATA Strobe		0			ns
t_{hold}	Hold time from DATA Strobe		750			ns
DATA STROBE						
t_W	Pulse width		1		128	μs
t_{WR}	Pulse Width for Internal Reset generation		128			μs
t_f, t_r	Pulse and Fall Times				100	ns
t_{LOW}				600		μs
t_{HIGH}				350		μs
t_{set-up}(*)	Set-up Time ROM-EM		70			μs

(*) t_{set-up} time means that the data coming from ext. ROM must be stable at least 70 μsec before the rising edge of ROM-EN.

PIN FUNCTIONS

Pin 1 – GND (digital)
Digital ground is linked to this pin.

Pin 21 – GND (analog)
Analog ground is linked to this pin.

Pin 3-8 and 11-17 – ROM-ADD
13 PUSH PULL type output pins for external memory address.

Pins 2, 9, 10, 47 – EA
These four pins give in output the channel number that is reading the external memory.
When the output is off (does'nt exist an address) the output is connected to a internal pull-up. With these 4 pins the memory is expanded up to 128 Kbyte (8 Kbyte/channel).

Pin 24 – TAB1/TAB2
It shows which one of the two tables (TAB1 or TAB2) is read.
Pin 24 permits to double the memory so reading 256 Kbyte addressing memory (top configuration).

Pin 19 – CLOCK (4 MHz)
For correct functioning the generator must be external to the chip and the duty cycle must be very close to 50%.

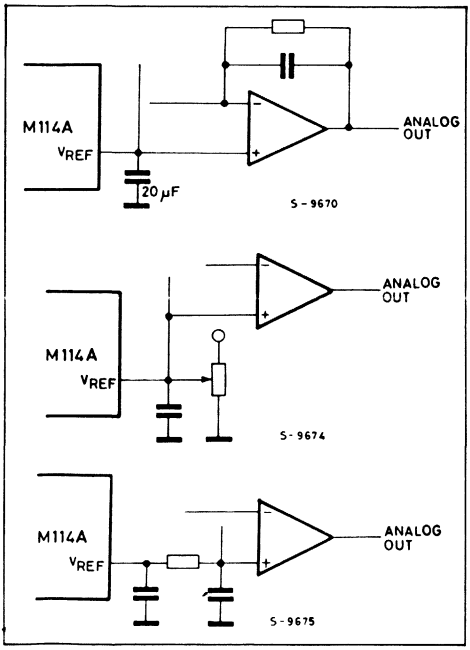
Pin 20 – RESET
All channel are reset by reading this pin and the 13 external ROM address outputs toghether with the 4 sound outputs are placed in a high impedence state.

Pin 22 – Analog power supply
The power supply for all analog parts, i.e. DAC attenuator, etc...., are linked to this pin. It is therefore important that this power supply should be very stable and well smoothed.
The internal power supply chip separation allows a great improvement of signal/noise ratio.

PIN FUNCTIONS (continued)

Pin 23 – Voltage reference Input (V_{REF})
V_{REF} is the average value of the DAC output. With V_{supply} = 5V, V_{REF} is nominally 2.5V but could vary by chip to chip (~10mV).
Even if the V_{REF} should be the optimum average value it is possible to use the external OP. AMP. or only a trimmer to adjust V_{REF}.
Instead of the external OP. AMP. it is possible to use and of the circuitry of Fig. 3.

Fig. 3



Pins 26, 28, 29, 30 – Analog out
These outputs are under current with an output impedance of approximatly 1 KΩ and the filter or external integra or must have a low input impedence. This means that the voltage between output and V_{REF} must be negligeable so as to obtain a good signal linearity.
An integrator together with a low pass filter are necessary if the tables have been DELTA coded. If on the other hand they have been coded in absolute values then only a low pass filter is needed.

If the channels do not have to be separated for stereofonic effects or otherwise, a single output may be used routing, by µP programming, all channels to this pin.

Pin 31 – ROM ENABLE (Low active)
This is a PUSH-PULL-TYPE-OUTPUT and is used to set the external memory in stand-by so as to reduce consumption whenever is not read.

Pin 32-39 – ROM-DATA
8 input pins for data from external memory.

Pin 40-45 – DATA-BUS
6 input pins for data from the microprocessor. 8 of these data groups make up a complete piece of information.

Pin 46 – BUS-STROBE
A signal from the microprocessor must arrive at this input in order to memorize the present code onto the DATA-BUS.
Memorization occurs on both edges.

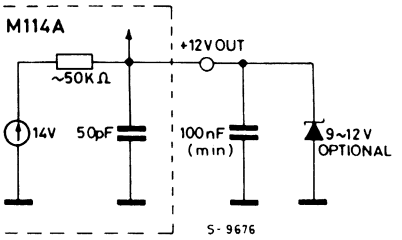
Pin 27 – COMMON NODE
This pin permit the access to the common point placed before the four output switches.

Pin 18 – Digital Power Supply
The power supply for all digital parts, i.e. counters, memories, etc...., are linked to this pin.

Pin 48 – Testing
This pin is utilized only for testing and must not be considered by the user.

Pin 25 (+12V out)
This pin is the output of an internal 5V/14V - DC-DC converter and it needs of an external filtering capacitance (min 100 nF). The performances of DAC and attenuator are very improved with an external zener that clamp the voltage elevator output (see Fig. 4).

Fig. 4



M114A

GENERAL DESCRIPTION

The M114A is a device that allows digital sound synthesis.

The essential system needed consists of a microprocessor, an M114A and an external memory with a maximum of 256 Kbytes.

Sound generation is based on cyclic reading of a table corresponding to a waveform of the timbre to be reproduced.

As the waveform and therefore also the spectrum frequently change, a series of tables of form and frequency appropriate to the sound are cyclically scanned during sound reproduction.

The effect caused by the sudden passage from one table to the next would be unpleasant unless there is such a large number of tables to allow a smooth unnoticeable change from one table to the following.

A favourable compromise between number of tables and quality of sound, that has been implemented in the M114A is the following: A limited number of tables which may even diverge from one another are chosen during an initial phase of analysis after which, during the reproduction phase, two adjoining tables are read simultaneously by extracting a percentage of one and the remaining percentage of the other.

Therefore by starting with 100% of one and zero of the other and successively increasing the second while decreasing the first, so that the sum of the percentages is always equal to 100, there will come a point at which there is a 100% of the second and zero of the first thus having achieved a smooth passage from one table to the next. In the M114A this passage is made up of a maximum of 16 steps.

The tables are stored in an external memory and may be of eight different lengths ranging from 16 to 2048 bytes. The M114 can handle up to a maximum of 256 Kbytes.

MEMORY EXPANSION

With the 13 pins ROM-ADD is possible to address 8 Kbyte of memory.
The 5 pins named EA permit an expansion to 128 Kbyte, while with the pin TAB1/TAB2 we have 256 Kbyte for the top configuration.

The tables may be coded using each waveform's absolute value or by the difference between adjoining samples, that is, in a incremental manner (Delta Modulation).
The typical resolution in Delta Modulation is 12 bit with a sinusoidal wave coded in a 16-byte table.
A low pass filter at the output is sufficient in the first case to reconstruct the original signal but with this mode interpolation is impossible and very long tables would be necessary for low frequency sounds causing a waste of memory.
With the addition of an integrator at the output in the second case, the waveforms are coded thus allowing easy interpolation. By simply reading the same data n time and dividing the amplitude of each reading by n, a ramp of n small steps is obtained instead of a large single step. The value of n may be 1, 2 or 4.
When a waveform is coded in this way (Delta-Modulation or incrementally), one must check that the sum of the samples in an entire period is always equal to zero or there would be a continuity which could even saturate the external integrator.
Always the M114A completes the reading of a table before the starting of another. This too avoids saturation of the external integrator. Whenever it is necessary to suddenly move from one table to another before the read cycle has been completed the FF forced-zero-cross code must be forwarded to the 8 frequency bits.
It is possible to drive the M114A in such a way that the programmed frequency becomes active immediately, without waiting for the running table to end (asynchronous mode); or that this change of frequency occurs only at the end of the running table (synchrounous-mode).

ASYNCHRONOUS MODE (SET UP AT RESET)
The frequency-information in a command causes the immediate change of the frequency, while the table and all the other parameters are changed only when the table has been completely scanned.
This type of operation is useful for producing vibrato effects on long tables or vibrato effects on low frequency sounds.

In fact in these cases it is useful to be able to vary continuously the scanning frequency of the same table, without being bound to execute the variation of frequency at the end of the table.

GENERAL DESCRIPTION (continued)

SYNCHROUNOUS MODE

The frequency-information in a command causes the synchronous change of table and frequency, this is obtained by delaying the frequency change until the running table has been completely scanned.

This command is very useful in same special effects (glide) because it avoids the reading of the table in part with the old frequency and in part with the new one, then causing on audible click.

This way-to-operate is useful in the reproduction of deep vibrato as notes placed at the octave boundary, for glide effects and in any case when it is necessary to go beyond the octave boundary without discontinuity.

In fact in these cases it is necessary to schedule in the M114 the length of table and table frequency scanning completely different from the previous programming.

To avoid clicks it is indispensable to finish the old table with the old frequency before starting the new one with new frequency.

The commands for synchronization are:

SSG **Set Global Sync.** (F9 Code). Activates the global synchronism also during normal working of the chip, without that the already active channels will be effected.

RSG **Reset Sync. Global** (F8 Code). This command disables global sync.

RSS **Reverse Sync. Status** (FA Code). This command inverts the synchronism state only for the next command.

Everyone of these three commands is accomplished by sending a complete command sequence with F9/FA/FB frequency codes, rispectively.

All the remaining bits are ignored.

Note that the **RSS** command can be obtained by sending eight times the 6-bit data 111110.

As shown in Tab. 3, there are six bit among the control bits that are dedicated to the choice of table pair length and n number of repeated readings of each table.

The frequency of sample readings is synchronous. This means that the frequency is a whole multiple of the table length.

In this way any problem caused by intermodulation is eliminated but a noise due to "collision" is produced. As there is a single output circuit for all channels, that is interpolator, D/A converter, attenuator, ecc., each time more than one channel requires access to this circuit one or more other channels must wait.

The amount of time necessary for the output circuit to process each table, that is the period of time for which each channel uses the circuit during each sample reading cycle, is of 2μs. The delay will therefore be proportional to the number of channels operating simultaneously and to the frequency that they are generating. As these parameters casually vary so will the delay thus producing a casual alteration of the original waveform.

Simulation has proved that under worst possible conditions the signal/noise ratio due to this problem is around 60dB.

In conclusion let us mention the envelope that has to be controlled by the microprocessor which, at suitable intervals, must forward the desired attenuation coefficient.

There are 64 possible attenuations each with steps of approximately 0.75dB;

The passage from one level to another may be immediate or to gradual increments of 1/256 of the maximum amplitude at a frequency proportional to external table reading frequency.

OPERATION

The M114A receives a single internal microprocessor instruction at a time. This instruction is made up of 48 bits per channel to be activated each time one or more parameters characterising the sound to be generated within a single channel are varied.

Each M114A channel continuously generates the same signal, that is it reads the same table, with the same mixing coefficient, with the same amplitude, ecc., until the microprocessor forwards a different instruction.

Timbre amplitude evolution and any other slight frequency changes must be handled in real-time by the microprocessor.

Often the microprocessor is unable to up-date the amplitude with sufficient frequency. For this reason the M114A carries out a gradual change from one amplitude to another at steps

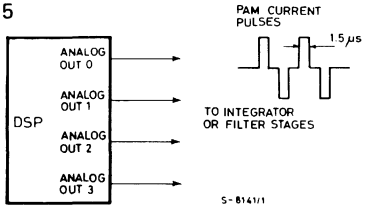
GENERAL DESCRIPTION (continued)

of 1/256 of maximum sample frequency amplitude if the change in level is greater than 128 steps, of 1/2 of this frequency if greater than 64, of 1/4 if greater than 32 and of 1/8 if smaller than or equal to 32 steps.

Each channel reads two samples at the sample frequency switch front by taking one from each table, sums them according to the mixing coefficient and forwards the result to the DAC whose suitably attenuated output goes to the previously selected output pin (Fig. 5).

This operation requires 2μs and as there is a single output circuit for all channels it is certain that one or more channels will simultaneously request the use of the circuit. Thus a priority order has been assigned to each channel. This order is fixed, channel zero being that of greatest priority followed in order by the others.

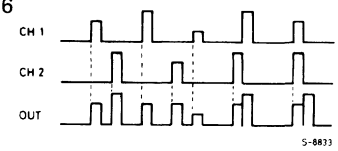
Fig. 5



When more than one channel is simultaneously active at the output pin there will be an overlap of impulse sequence of each channel.

The example of Fig. 6 shows an output signal with 2 active channels, CH1 has greater priority then CH2:

Fig. 6



The signal will change from impulsive to continuous by passing through:

- a low pass filter if the table have been coded using absolute values.
- an integrator if in delta modulation.

PROGRAMMING

48 bits subdivided into 8 groups of 6 bits each must be forwarded in order to programme a channel.

DATA PROGRAMMING ORDER

BYTE \ N. PIN	34	35	36	37	38	39
1st	ATTENUATION					
	A5	A4	A3	A2	A1	A0
2nd	4 OUTPUTS		TABLE 1 ADDRESS		TABLE 2 ADDRESS	
	1	0	7	6	7	6
3rd	TABLE 2 ADDRESS					
	5	4	3	2	1	0
4th	TABLE 1 ADDRESS					
	5	4	3	2	1	0
5th	READING METHOD & TABLE LENGTH					
	L2	L1	L0	M2	M1	M0
6th	INTERPOLATION				IMMEDIATE CONNECTION	OCTAVE DIVISOR
	3	2	1	0	0	1
7th	CHANNEL COEFFICIENT				FREQUENCY	
	3	2	1	0	1	0
8th	FREQUENCY					
	7	6	5	4	3	2

GENERAL DESCRIPTION (continued)

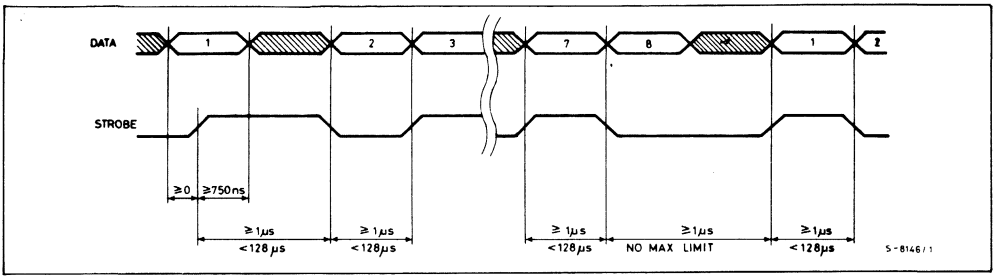
A group of 6 bits is memorised on every Data Strobe switch front.

As the data bus is read approximately 250ns after transition from the Data Strobe, the 6 data bits may simultaneously arrive with the Data Strobe switch.

The following graph shows the time lapse that must be assigned to these signal for correct functioning.

No more than 128μs must pass between one Data Strobe transition and the next during transmission of the 8 groups of data or else synchronisation is lost due to the internal automatic reset generated after 128μs from the last Data Strobe transition causing the data to be misinterpreted.

One should wait for at least 9μs after the forced-zero-cross command has been given between the last group of data of one instruction and the first group of the next.



The degree of priority of the channel and the number of channels in use at that moment must be taken into account in order to shorten this wait. If there is maximum priority the wait will be a minimum wait of approximately 2μs. The same holds if the priority is not maximum but there are no other channels in use. There will however be a maximum wait of 2μs for each active channel with greater priority than the channel in question.

If another instruction were to be transmitted without a sufficient wait, there would be the risk of losing the previous instruction of forced zero cross.

The wait is unnecessary after normal commands.

Every data group must be remain present for at least 1μs after Data Strobe transition.

The 48 bit functions are the following:

A) 8 address bits for the 1st table (ext. ROM)
B) 8 address bits for the 2nd table (ext. ROM)
C) 8 frequency bits (4-note and 4-twelfths of note and ± 1 or 2/1000)
D) 6 attenuation or amplitude address bits
E) 4 interpolation bits
F) 4 channel address bits
G) 6 reading mode and table length bits (ext. ROM)
H) 2 bits for choice between four outputs
I) 1 bit for a frequency octave change
J) 1 bit for gradual disenable of envelope

While waiting for the present 1st reading cycle to terminate, the above data (not immediately operational) is memorized into the internal RAM1).

The data is transfered to the addressed channel and made operational when the table address crosses through zero.

An exception is made by the 8 frequency bits and those varying the frequency octave as they operate immediately (See synchronization).

All data may be made operational by giving the forced-zero-cross command.

48 PROGRAMMING BIT FOR CHANNEL SELECTION

8 Address Bits 1st Table (ext. ROM)

These determine the most significant part of the 13 external memory address bits but according to the table length chosen by the 6 mode bits, some of the least significant of these 8 bits are suitably substituted by the M114A.

In the case of a maximum table length, 2048 bytes, there will only be 2 significant bits to address the table while the remaining 11 will address each single table word.

48 CHANNEL PROGRAMMING BIT DESCRIPTION (continued)

By already knowing the table length, the programmer will be able to programme the most significant bits needed for table address only and ignore the others.
As the maximum memory that can be handled is of 8Kbytes, if the table has a length of 1Kbyte it is sufficient to programme the three most significant bits and ignore the other five.

8 Address Bits 2nd Table (ext. ROM)
As above but refering to the second table.
One must consider that the zero-cross refers to the first table and that during table mixing the second table may assume a percentage value of zero while tha first table can only assume a minimum percentage value of 1/16 of the maximum value.

8 Frequency Bits
The 4 most significant bits characterize one of the 15 available notes with HEX. Codes from 0 to E. Eleven movements in twelfths of a semitone may be obtained with the remaining 4 bits as well as 4 ± 1/1000 and ± 2/1000 note frequency variations.
These permit the production of: Vibrato, Glissando, Effetto coro, etc...
The FF codes correspond to the forced-zero-cross command while FC maintains the previous frequency. F9, FA, FB are synchronization commands. The remaining codes are used for testing and therefore must not be used by the operator.
Table 1 shows the 240 frequencies obtainable by setting the external clock to 4MHz and the table length to 16 bytes, with single reading and without inserting an octave divisor. These are the highest octave frequencies obtainable with the M114A.
In practice double, quadruple, etc...frequencies may be obtained by writing 2, 4, etc. complete waveform periods in the table.

6 Attenuation Bits
These determine the attenuation addresses present at the output signal, to the internal table. The contents of this table follow a logarithmic pattern so as to produce a decrease of 0.75dB for each address unit increment. See table 2. The word length if of 10 bits.
Previous processing by a suitable circuit in order to obtain a gradual amplitude variation links the ten outputs of this table to the 10 bit output attenuator.
The gradual movement from the present level to that just programmed takes place by increasing or decreasing the 8 most significant bits of the attenuation table contents, with the same frequency with which the external memory tables are being scanned if the difference in level is greater than 128 steps, or with 1/2 of this frequency if greater than 64 steps, or 1/4 if greater than 32, or 1/8 if smaller than or equal to 32. In conclusion, output signal amplitude increases of decreases at each variation by 1/256 of the maximum value.
By setting the bit that deals with the gradual envelope there is an immediate passage from the present level to that programmed.

4 Interpolation Bits
These define the mixing coefficient between the two waveform tables.
It is possible in this way to sum the 1st waveform percentage with the remaining 2nd waveform percentage thus obtaining a third signal which will be forward to the output.
In greater detail, the operation carried out is the following:

$$D = (D1 * (K + 1)/16) + (D2 * (15 - K)/16)$$

where:
- D is the data at the output to the DAC (8 bits in complement with 2)
- D1 is the data read from the 1st table (8 bits in complement with 2)
- D2 is the data read from the 2nd table (8 bits in complement with 2)
- K is a 4 bit interpolation coefficient (from 0 to 15)

Obviously only the first waveform will be output if K = 15.

4 Channel Address Bits
These indicate to which of the 16 M114A channels the remaining 44 bits will be forwarded.

6 Mode Bits
These indicate the table couple reading mode (ext. ROM).
For each table there are 58 distinct combinations that include both table lengths and the number of repeated readings from the same address. (ext. ROM). See table N. 3.
The three most significant bits characterize the table lengths while the other three characterise the length ratio between tables and the number of repeated readings.

2 Output Address Bits
These indicate to which of the 4 output pins the corresponding channel signal must be forwarded. This is necessary in order to obtain stereophonic effect or to separate channels used for accompanyment from those of "SOLO", etc...

1 Octave Divisor Bit
This is used to pass from one octave to another without changing the table length.

1 Instant ENVELOPE Change Bit
This orders instant passage from the present amplitude to that programmed.

TABLE 1 — FREQUENCIES

NOTE	DEVIATION	-6/12	-5/12	-4/12	-3/12	-2/12	-1/12	-2/1000	-1/1000
	(Hex)	0	1	2	3	4	5	6	7
C	0	1016.78	1021.45	1026.69	1031.46	1036.27	1041.67	1044.39	1045.48
C#	1	1077.01	1082.25	1087.55	1092.90	1098.30	1103.14	1106.81	1107.42
D	2	1140.90	1146.79	1152.07	1158.08	1163.47	1168.91	1172.33	1173.71
D#	3	1209.19	1215.07	1221.00	1226.99	1232.29	1238.39	1242.24	1243.01
E	4	1281.23	1287.00	1293.66	1299.55	1305.48	1312.34	1315.79	1317.52
F	5	1356.85	1363.33	1369.86	1376.46	1383.13	1389.85	1393.73	1395.67
F#	6	1437.81	1445.09	1451.38	1458.79	1466.28	1472.75	1477.10	1478.20
G	7	1523.23	1530.22	1538.46	1545.60	1552.80	1560.06	1564.95	1566.17
G#	8	1614.21	1622.06	1629.99	1638.00	1644.74	1652.89	1658.37	1659.75
A	9	1709.40	1718.21	1727.12	1734.61	1743.68	1751.31	1755.93	1757.47
A#	A	1811.59	1819.84	1829.83	1838.24	1846.72	1855.29	1860.47	1862.20
B	B	1919.39	1928.64	1937.98	1947.42	1956.95	1966.57	1972.39	1974.33
2C	C	2032.52	2042.90	2053.39	2063.98	2072.54	2083.33	2089.86	2089.86
2C#	D	2155.17	2164.50	2176.28	2185.79	2195.39	2207.51	2212.39	2214.84
2D	E	2283.11	2293.58	2304.15	2314.81	2325.58	2339.18	2344.67	2347.42
	F	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing

NOTE	DEVIATION	0	+1/1000	+2/1000	+1/12	+2/12	+3/12	+4/12	+5/12
	(Hex)	8	9	A	B	C	D	E	F
C	0	1046.57	1047.67	1048.77	1051.52	1056.52	1061.57	1066.67	1071.81
C#	1	1108.65	1109.88	1111.11	1114.21	1119.19	1124.86	1130.58	1135.72
D	2	1174.40	1175.78	1177.16	1180.64	1186.24	1191.90	1197.60	1203.37
D#	3	1244.56	1246.11	1246.88	1250.78	1256.28	1262.63	1269.04	1274.70
E	4	1318.39	1320.13	1321.00	1324.50	1331.56	1337.79	1344.09	1350.44
F	5	1396.65	1398.60	1399.58	1403.51	1410.44	1417.43	1424.50	1430.62
F#	6	1480.38	1481.48	1482.58	1486.99	1494.77	1501.50	1508.30	1516.30
G	7	1567.40	1569.86	1571.09	1576.04	1583.53	1591.09	1598.72	1606.43
G#	8	1661.13	1662.51	1663.89	1669.45	1677.85	1684.92	1693.48	1702.13
A	9	1760.56	1762.11	1763.67	1768.35	1777.78	1785.71	1793.72	1803.43
A#	A	1863.93	1865.67	1869.16	1874.41	1883.24	1892.15	1901.14	1910.22
B	B	1976.28	1978.24	1980.20	1984.13	1994.02	2004.01	2014.10	2024.29
2C	C	2092.05	2094.24	2096.44	2103.05	2114.16	2123.14	2134.47	2143.62
2C#	D	2217.29	2219.76	2222.22	2227.17	2239.64	2249.72	2259.89	2272.73
2D	E	2350.18	2352.94	2352.94	2361.28	2372.48	2383.79	2395.21	2406.74
	F	For Testing	RSG	RSS	SSG	Previously Selected Frequency	For Testing	For Testing	Forced Zero Cross

TABLE 2 – ATTENUATION

ATTENUATION ADDRESS						OUTPUT ROM	ATTENUATION
A5	A4	A3	A2	A1	A0	DECIMAL	- dB
0	0	0	0	0	0	1024	0.00
0	0	0	0	0	1	939	0.75
0	0	0	0	1	0	862	1.50
0	0	0	0	1	1	790	2.25
0	0	0	1	0	0	725	3.00
0	0	0	1	0	1	665	3.75
0	0	0	1	1	0	610	4.50
0	0	0	1	1	1	559	5.26
0	0	1	0	0	0	513	6.00
0	0	1	0	0	1	471	6.75
0	0	1	0	1	0	432	7.50
0	0	1	0	1	1	396	8.25
0	0	1	1	0	0	363	9.01
0	0	1	1	0	1	333	9.76
0	0	1	1	1	0	306	10.49
0	0	1	1	1	1	281	11.23
0	1	0	0	0	0	257	12.01
0	1	0	0	0	1	236	12.75
0	1	0	0	1	0	216	13.52
0	1	0	0	1	1	199	14.23
0	1	0	1	0	0	182	15.00
0	1	0	1	0	1	167	15.75
0	1	0	1	1	0	153	16.51
0	1	0	1	1	1	141	17.22
0	1	1	0	0	0	129	17.99
0	1	1	0	0	1	118	18.77
0	1	1	0	1	0	108	19.54
0	1	1	0	1	1	99	20.29
0	1	1	1	0	0	91	21.03
0	1	1	1	0	1	84	21.72
0	1	1	1	1	0	77	22.48
0	1	1	1	1	1	70	23.30
1	0	0	0	0	0	65	23.95
1	0	0	0	0	1	59	24.79
1	0	0	0	1	0	54	25.56
1	0	0	0	1	1	50	26.23
1	0	0	1	0	0	46	26.95
1	0	0	1	0	1	42	27.74
1	0	0	1	1	0	38	28.61
1	0	0	1	1	1	35	29.32
1	0	1	0	0	0	32	30.10
1	0	1	0	0	1	29	30.96
1	0	1	0	1	0	27	31.58
1	0	1	0	1	1	25	32.25
1	0	1	1	0	0	23	32.97
1	0	1	1	0	1	21	33.76
1	0	1	1	1	0	19	34.63
1	0	1	1	1	1	17	35.60
1	1	0	0	0	0	15	36.68
1	1	0	0	0	1	14	37.28
1	1	0	0	1	0	13	37.93
1	1	0	0	1	1	12	38.62
1	1	0	1	0	0	11	39.38
1	1	0	1	0	1	10	40.21
1	1	0	1	1	0	9	41.12
1	1	0	1	1	1	8	42.14
1	1	1	0	0	0	7	43.30
1	1	1	0	0	1	6	44.64
1	1	1	0	1	0	5	46.23
1	1	1	0	1	1	4	48.16
1	1	1	1	0	0	3	50.66
1	1	1	1	0	1	2	54.19
1	1	1	1	1	0	1	61.21
1	1	1	1	1	1	0	Max.

TABLE 3 – READING MODES

MODE						Length		Length	N° of Table Reads	
M2	M1	M0	L2	L1	L0	1st Table		2nd Table	1st Table	2nd Table
0	0	0	0	0	0	16		16	2	2
0	0	0	0	0	1	32		32	2	2
0	0	0	0	1	0	64		64	2	2
0	0	0	0	1	1	128	(1/1)	128	2	2
0	0	0	1	0	0	256		256	2	2
0	0	0	1	0	1	512		512	2	2
0	0	0	1	1	0	1024		1024	2	2
0	0	0	1	1	1	2048		2048	2	2
0	0	1	0	0	0	16		16	1	1
0	0	1	0	0	1	32		32	1	1
0	0	1	0	1	0	64		64	1	1
0	0	1	0	1	1	128	(1/1)	128	1	1
0	0	1	1	0	0	256		256	1	1
0	0	1	1	0	1	512		512	1	1
0	0	1	1	1	0	1024		1024	1	1
0	0	1	1	1	1	2048		2048	1	1
0	1	0	0	0	0	16		16	4	4
0	1	0	0	0	1	32		32	4	4
0	1	0	0	1	0	64		64	4	4
0	1	0	0	1	1	128	(1/1)	128	4	4
0	1	0	1	0	0	256		256	4	4
0	1	0	1	0	1	512		512	4	4
0	1	0	1	1	0	1024		1024	4	4
0	1	0	1	1	1	1024		1024	4	4
0	1	1	0	0	0	16		16	1	1 *
0	1	1	0	0	1	32		16	1	1
0	1	1	0	1	0	64		32	1	1
0	1	1	0	1	1	128	(2/1)	64	1	1
0	1	1	1	0	0	256		128	1	1
0	1	1	1	0	1	512		256	1	1
0	1	1	1	1	0	1024		512	1	1
0	1	1	1	1	1	2048		1024	1	1
1	0	0	0	0	0	16		8	1	2
1	0	0	0	0	1	32		16	1	2
1	0	0	0	1	0	64		32	1	2
1	0	0	0	1	1	128	(2/1)	64	1	2
1	0	0	1	0	0	256		128	1	2
1	0	0	1	0	1	512		256	1	2
1	0	0	1	1	0	1024		1024	1	2
1	0	0	1	1	1	2048		1024	1	2
1	0	1	0	0	0	16		16	1	1 *
1	0	1	0	0	1	32		16	1	1 *
1	0	1	0	1	0	64		16	1	1
1	0	1	0	1	1	128	(4/1)	32	1	1
1	0	1	1	0	0	256		64	1	1
1	0	1	1	0	1	512		128	1	1
1	0	1	1	1	0	1024		256	1	1
1	0	1	1	1	1	2048		512	1	1
1	1	0	0	0	0	16		4	1	4
1	1	0	0	0	1	32		8	1	4
1	1	0	0	1	0	64		16	1	4
1	1	0	0	1	1	128	(4/1)	32	1	4
1	1	0	1	0	0	256		64	1	4
1	1	0	1	0	1	512		128	1	4
1	1	0	1	1	0	1024		256	1	4
1	1	0	1	1	1	2048		512	1	4

TABLE 3 – READING MODES (continued)

MODE						Length		Length	N° of Table Reads	
M2	M1	M0	L2	L1	L0	1st Table		2nd Table	1st Table	2nd Table
1	1	1	0	0	0	16		16	1	1 *
1	1	1	0	0	1	32		16	1	1 *
1	1	1	0	1	0	64		16	1	1 *
1	1	1	0	1	1	128	(8/1)	16	1	1
1	1	1	1	0	0	256		32	1	1
1	1	1	1	0	1	512		64	1	1
1	1	1	1	1	0	1024		128	1	1
1	1	1	1	1	1	2048		256	1	1

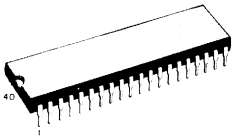
* Repetitions.

M114S

ADVANCE DATA

DIGITAL SOUND GENERATOR

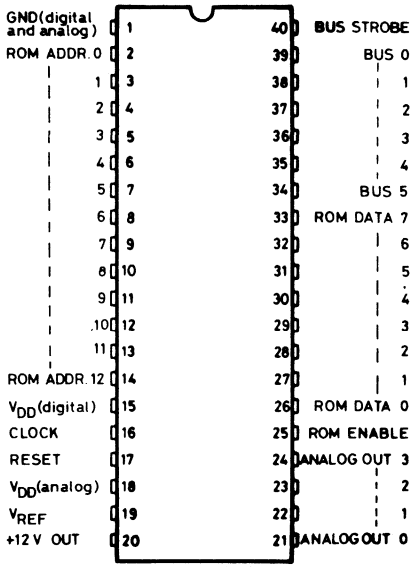
- SOUND GENERATED BY READING TABLES CODED IN DELTA MODULATION OR IN ABSOLUTE VALUES, SITUATED IN AN EXTERNAL MEMORY OF 8K MAX.
- 16 INDEPENDENT CHANNELS
- 12 BIT EQUIVALENT D/A CONVERTER RESOLUTION (DELTA MODULATION)
- 8 DIFFERENT TABLE LENGTHS AND 8 READING MODES GIVING A TOTAL OF 58 DISTINCT COMBINATIONS
- 16 DIFFERENT MIXABLE LAYERS BETWEEN TWO SEPARATE TABLES
- MULTIPLE READING PERMITS INTERPOLATION BETWEEN TWO ADJOINING SAMPLES ON THE SAME TABLE
- 4 SELECTABLE ANALOG OUTPUTS
- 10 BIT INTERNAL ATTENUATOR WITH GRADUAL AMPLITUDE VARIATION
- ROM ENABLE OUTPUT TO MINIMISE EXTERNAL MEMORY POWER CONSUMPTION
- POSSIBILITY OF SYNCHRONOUS AND ASYNCHRONOUS FREQUENCY-TABLE CHANGE AT THE END OF THE READING TABLE



DIP. 40 Plastic

ORDERING NUMBER: M114S-B1

CONNECTION DIAGRAM



The M114S is a 16 channel digital polyphonic, politimbric sound generator.

The M114S must be driven by a microprocessor and needs an external memory.

With this device it is possible to synthesize a large range of sound by simply transcribing the most significant periods of the sound to be reproduced into an external memory and programming a suitable reading sequence for these periods with the use of a microprocessor.

The M114S is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology and is assembled in plastic DIP.40.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 7	V
V_I	Input voltage	-0.3 to V_{DD}	V
V_O	Output voltage	-0.3 to V_{DD}	V
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - Block Diagram

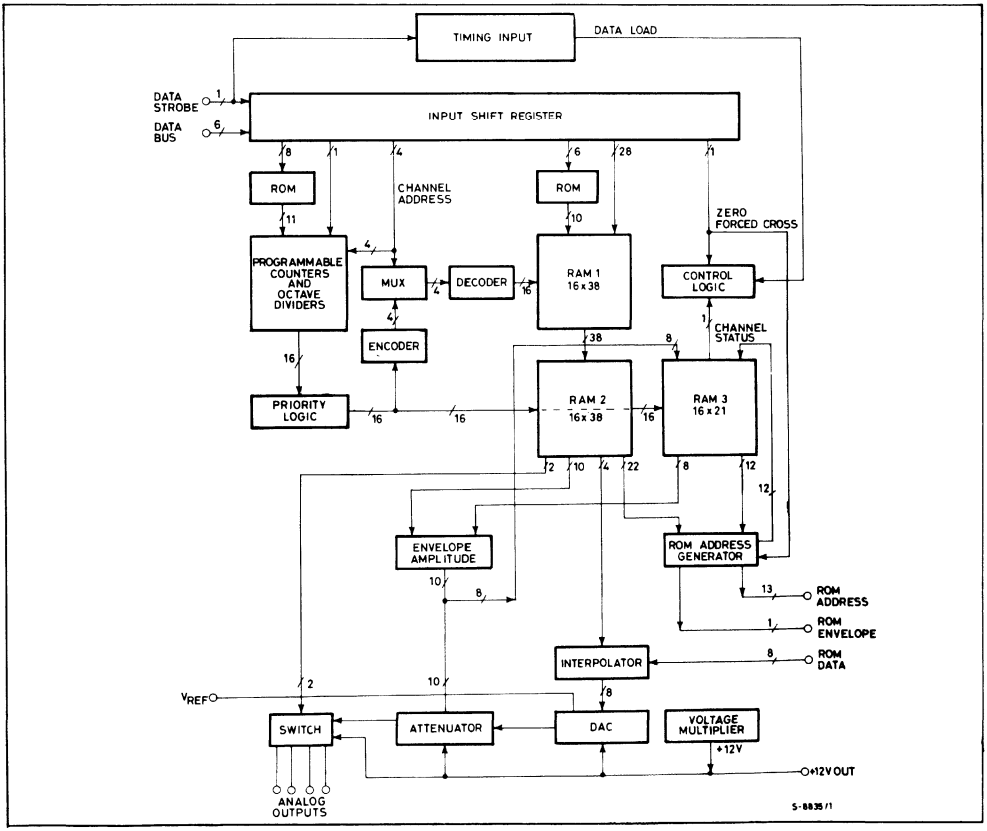
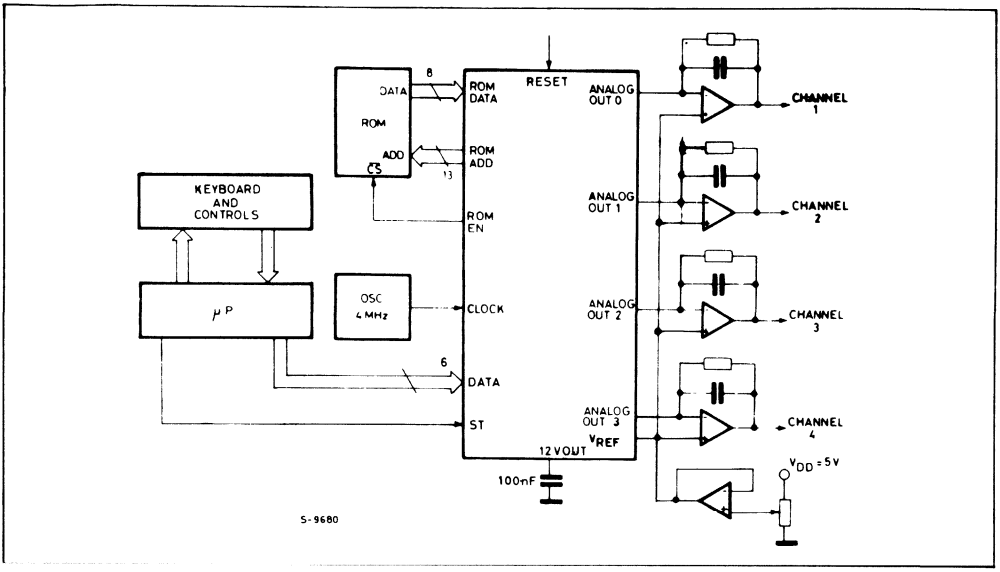


Fig. 2 - System Configuration



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 5%, V_{SS} = 0, T_{amb} = 0/70°C, V_{DD} DIG = V_{DD} Analog)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
INPUTS: RESET (pin 17), CLOCK (pin 16), ROM DATA (pins 26-33), DATA BUS (pins 34-39), DATA ST. (pin 40)						
V_{IL}	Low Input Level				0.8	V
V_{IH}	High Input Level		2.2			V
I_I	Input Leakage Current	$V_I = V_{DD}$ to V_{SS}			± 1	μA
DIGITAL OUTPUTS (HIGH IMPEDANCE* with 10KΩ pull-up): ROM-ADD (pins 2-14; 11-17), ROM EN (pin 25)						
V_{OL}	Low Output Level	I_{OL} = 1mA			0.4	V
V_{OH}	High Output Level	I_{OH} = 100μA	2.4			V
ANALOG OUTPUTS: (pins 21, 22, 23, 24), V_{REF} (pin 19)						
V_{REF}	Voltage Reference Output	I_O = ± 1mA		2.5		V
I_O	Output Current (current generator)	Zero attenuation Max input code to the DAC		± 1		mA
POWER DISSIPATION						
I_{DD}	Supply Current	V_{DD} = 5.25V			100	mA

* High impedance means that, when the addresses are off, the digital output is connected with an internal resistive pull-up.

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLOCK						
t_{CK}	Input Clock Frequency			4.000		KHz
t_r, t_f	Rise and Fall Time	10% to 90%			20	ns
t_{WH}, t_{WL}	High and Low Pulse Width		80			ns
RESET						
t_W	Pulse Width	Clock = 4 MHz	10			μs
t_f	Fall Time	10% to 90%			20	ns
DATA BUS						
t_W	Pulse Width		750			ns
t_{set-up}	Set-up Time to DATA Strobe		0			ns
t_{hold}	Hold time from DATA Strobe		750			ns
DATA STROBE						
t_W	Pulse width		1		128	μs
t_{WR}	Pulse Width for Internal Reset generation		128			μs
t_f, t_r	Pulse and Fall Times				100	ns
t_{LOW}				600		μs
t_{HIGH}				350		μs
t_{set-up}(*)	Set-up Time ROM-EM		70			μs

(*) t_{set-up} time means that the data coming from ext. ROM must be stable at least 70 μsec before the rising edge of ROM-EN.

PIN FUNCTIONS

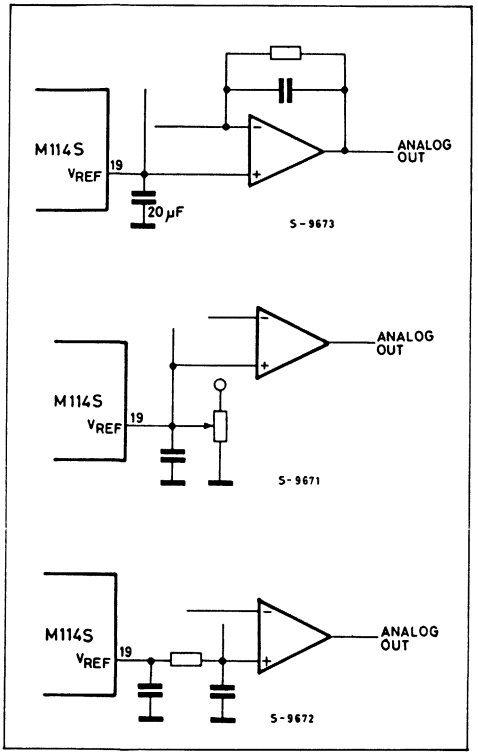
PIN 1 – GND (Analog and Digital)
Analog ground and digital ground are both linked to this pin.

Pins 21-24 – Analog Outputs
These outputs are under current with an output impedance of approximately 1 KΩ and the filter or external integrator must have a low input impedance. This means that the voltage drop between output pin and V_{REF} must be negligeable so as to obtain a good signal linearity.
An integrator together with a low pass filter are necessary if the tables have been "DELTA" coded. If on the other hand they have been coded in absolute values then only a low pass filter is needed.
If the channels do not have to be separated for stereophonic effects or otherwise, a single output may be used routing, by μP programming, all channels to this pin.

Pin 19 – Voltage Reference Output (V_{REF})
V_{REF} is the average value of the DAC output. With V_{supply}= 5V V_{REF} is nominally 2.5V but could vary by chip to chip (~10mV).
Even if the V_{REF} should be the optimum average value it is possible to use the EX. OP. AMP. or only a trimmer to adjust V_{REF}.
Instead of the external OP. AMP. it is possible to use one of the following circuitry (Fig. 3).

PIN FUNCTIONS (continued)

Fig. 3.



Pin 18 – Analog Power Supply
The power supply for all analog parts, i.e. DAC, attenuator, etc...., are linked to this pin.
It is therefore important that this power supply should be very stable and well smoothed.
The internal power supply chip separation requires a great improvement of signal/noise ratio.

Pin 15 – Digital Power Supply

The power supply for all digital parts, i.e. counters, memories, etc...., are linked to this pin.

Pin 17 – RESET
All channels are reset by raising this pin and the 13 external ROM address outputs together with the 4 sound outputs are placed in a high impedance state.

Pin 16 – CLOCK (4 MHz)
For correct functioning the generator must be external to the chip and the duty cycle must be very close to 50%.
The internal programmable counters switch on the positive leading edge.

Pin 20 (+12V out)
This pin is the output of an internal voltage elevator and it needs of an external filtering capacitance (min. 100 nF).
The performance of DAC and attenuator are very improved with an external zenze the clamps the voltage elevator output (see Fig. 4).

Pins 25 – ROM-ENABLE (Low active)
This is a PUSH-PULL type output and is used to set the external memory in stand-by so as to reduce consumption whenever it is not read.

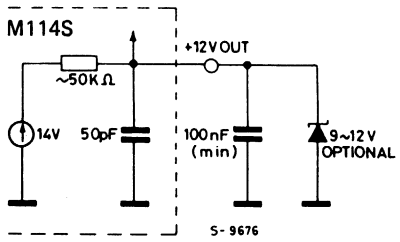
Pins 26 & 33 – ROM-DATA
8 input pins for data from external memory.

Pins 2 & 14 – ROM-ADDRESS
13 PUSH-PULL type output pins for external memory address.

Pins 34-39 – DATA-BUS
6 input pins for data from the microprocessor. 8 of these data groups make up a complete piece of information.

Pin 40 – DATA-BUS Strobe
A signal from the microprocessor must arrive at this input in order to memorise the present code onto the DATA-BUS.
Memorization occurs on both edges.

Fig. 4



GENERAL DESCRIPTION

The M114S is a device that allows digital sound synthesis.

The essential system needed consists of a microprocessor, an M114S and an external memory with a maximum of 8192 bytes.

Sound generation is based on cyclic reading of a table corresponding to a waveform of the timbre to be reproduced.

As the waveform and therefore also the spectrum frequently change, a series of tables of form and frequency appropriate to the sound are cyclically scanned during sound reproduction.

The effect caused by the sudden passage from one table to the next would be unpleasant unless there is such a large number of tables to allow a smooth unnoticeable change from one table to the following.

A favourable compromise between number of tables and quality of sound, that has been implemented in the M114S is the following: A limited number of tables which may even diverge from one another are chosen during an initial phase of analysis after which, during the reproduction phase, two adjoining tables are read simultaneously by extracting a percentage of one and the remaining percentage of the other.

Therefore by starting with 100% of one and zero of the other and successively increasing the second while decreasing the first, so that the sum of the percentages is always equal to 100, there will come a point at which there is a 100% of the second and zero of the first thus having achieved a smooth passage from one table to the next. In the M114S this passage is made up of a maximum of 16 steps.

The tables are stored in an external memory and may be of eight different lengths ranging from 16 to 2048 bytes. The M114S can handle up to a maximum of 8192 bytes.

The tables may be coded using each waveform's absolute value or by the difference between adjoining samples, that is, in a incremental manner (Delta Modulation).
The typical resolution in Delta Modulation is 12 bit with a sinusoidal wave coded in a 16-byte table.

A low pass filter at the output is sufficient in the first case to reconstruct the original signal but with this mode interpolation is impossible and very long tables would be necessary for low frequency sounds causing a waste of memory.

With the addition of an integrator at the output in the second case, the waveforms are coded thus allowing easy interpolation. By simply reading the same data n time and dividing the amplitude of each reading by n, a ramp of n small steps is obtained instead of a large single step.

The value of n may be 1, 2 or 4.
When a waveform is coded in this way (Delta-Modulation or incrementally), one must check that the sum of the samples in an entire period is always equal to zero or there would be a continuity which could even saturate the external integrator.

Always the M114S completes the reading of a table before the starting of another. This too avoids saturation of the external integrator. Whenever it is necessary to suddenly move from one table to another before the read cycle has been completed the FF forced-zero-cross code must be forwarded to the 8 frequency bits.

It is possible to drive the M114A in such a way that the programmed frequency becomes active immediately, without waiting for the running table to end (asynchronous mode); or that this change of frequency occurs only at the end of the running table (synchrounous-mode).

ASYNCHRONOUS MODE (SET UP AT RESET)
The frequency-information in a command causes the immediate change of the frequency, while the table and all the other parameters are changed only when the table has been completely scanned.

This type of operation is useful for producing vibrato effects on long tables or vibrato effects on low frequency sounds.

In fact in these cases it is useful to be able to vary continuously the scanning frequency of the same table, without being bound to execute the variation of frequency at the end of the table.

GENERAL DESCRIPTION (continued)

SYNCHROUNOUS MODE

The frequency-information in a command causes the synchronous change of table and frequency, this is obtained by delaying the frequency change until the running table has been completely scanned.

This command is very useful in same special effects (glide) because it avoids the reading of the table in part with the old frequency and in part with the new one, then causing on audible click.

This way-to-operate is useful in the reproduction of deep vibrato as notes placed at the octave boundary, for glide effects and in any case when it is necessary to go beyond the octave boundary without discontinuity.

In fact in these cases it is necessary to schedule in the M114S the length of table and table frequency scanning completely different from the previous programming.

To avoid clicks it is indispensable to finish the old table with the old frequency before starting the new one with new frequency.

The commands for synchronization are:

SSG **Set Global Sync.** (F9 Code). Activates the global synchronism also during normal working of the chip, without that the already active channels will be effected.

RSG **Reset Sync. Global** (F8 Code). This command disables global sync.

RSS **Reverse Sync. Status** (FA Code). This command inverts the synchronism state only for the next command.

Everyone of these three commands is accomplished by sending a complete command sequence with F9/FA/FB frequency codes, rispectively.

All the remaining bits are ignored.

Note that the **RSS** command can be obtained by sending eight times the 6-bit data 111110.

As shown in Tab. 3, there are six bit among the control bits that are dedicated to the choice of table pair length and n number of repeated readings of each table.

The frequency of sample readings is synchronous. This means that the frequency is a whole multiple of the table length.

In this way any problem caused by intermodulation is eliminated but a noise due to "collision" is produced. As there is a single output circuit for all channels, that is interpolator, D/A converter, attenuator, ecc., each time more than one channel requires access to this circuit one or more other channels must wait.

The amount of time necessary for the output circuit to process each table, that is the period of time for which each channel uses the circuit during each sample reading cycle, is of 2μs. The delay will therefore be proportional to the number of channels operating simultaneously and to the frequency that they are generating. As these parameters casually vary so will the delay thus producing a casual alteration of the original waveform.

Simulation has proved that under worst possible conditions the signal/noise ratio due to this problem is around 60dB.

In conclusion let us mention the envelope that has to be controlled by the microprocessor which, at suitable intervals, must forward the desired attenuation coefficient.

There are 64 possible attenuations each with steps of approximately 0.75dB;

The passage from one level to another may be immediate or to gradual increments of 1/256 of the maximum amplitude at a frequency proportional to external table reading frequency.

OPERATION

The M114S receives a single internal microprocessor instruction at a time. This instruction is made up of 48 bits per channel to be activated each time one or more parameters characterising the sound to be generated within a single channel are varied.

Each M114S channel continuously generates the same signal, that is it reads the same table, with the same mixing coefficient, with the same amplitude, ecc., until the microprocessor forwards a different instruction.

Timbre amplitude evolution and any other slight frequency changes must be handled in real-time by the microprocessor.

Often the microprocessor is unable to up-date the amplitude with sufficient frequency. For this reason the M114S carries out a gradual change from one amplitude to another at steps

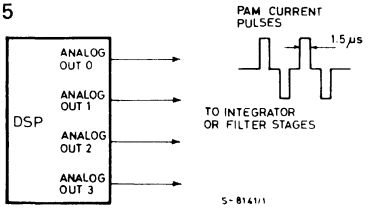
GENERAL DESCRIPTION (continued)

of 1/256 of maximum sample frequency amplitude if the change in level is greater than 128 steps, of 1/2 of this frequency if greater than 64, of 1/4 if greater than 32 and of 1/8 if smaller than or equal to 32 steps.

Each channel reads two samples at the sample frequency switch front by taking one from each table, sums them according to the mixing coefficient and forwards the result to the DAC whose suitably attenuated output goes to the previously selected output pin (Fig. 5).

This operation requires 2μs and as there is a single output circuit for all channels it is certain that one or more channels will simultaneously request the use of the circuit. Thus a priority order has been assigned to each channel. This order is fixed, channel zero being that of greatest priority followed in order by the others.

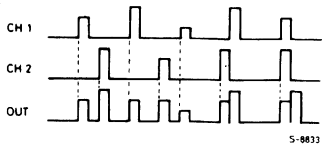
Fig. 5



When more than one channel is simultaneously active at the output pin there will be an overlap of impulse sequence of each channel.

The example of Fig. 6 shows an output signal with 2 active channels, CH1 has greater priority then CH2:

Fig. 6



The signal will change from impulsive to continuous by passing through:

- a low pass filter if the table have been coded using absolute values.
- an integrator if in delta modulation.

PROGRAMMING

48 bits subdivided into 8 groups of 6 bits each must be forwarded in order to programme a channel.

DATA PROGRAMMING ORDER

BYTE \ N. PIN	34	35	36	37	38	39
1st	ATTENUATION					
	A5	A4	A3	A2	A1	A0
2nd	4 OUTPUTS		TABLE 1 ADDRESS		TABLE 2 ADDRESS	
	1	0	7	6	7	6
3rd	TABLE 2 ADDRESS					
	5	4	3	2	1	0
4th	TABLE 1 ADDRESS					
	5	4	3	2	1	0
5th	TABLE ELNGTH			READING METHOD		
	L2	L1	L0	M2	M1	M0
6th	INTERPOLATION				IMMEDIATE CONNECTION	OCTAVE DIVISOR
	3	2	1	0	0	1
7th	CHANNEL ADDRESS				FREQUENCY	
	3	2	1	0	1	0
8th	FREQUENCY					
	7	6	5	4	3	2

GENERAL DESCRIPTION (continued)

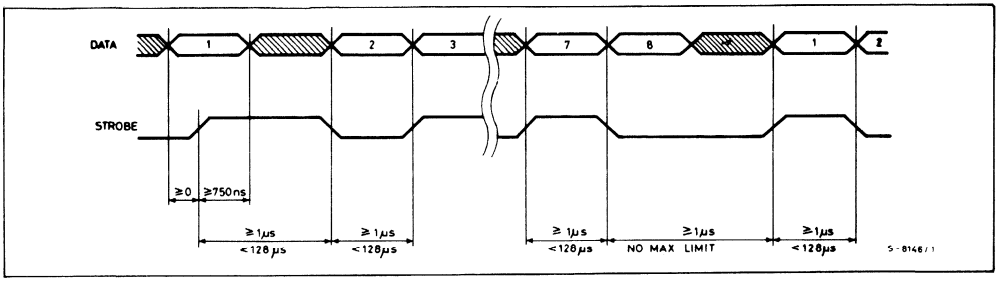
A group of 6 bits is memorised on every Data Strobe switch front.

As the data bus is read approximately 250ns after transition from the Data Strobe, the 6 data bits may simultaneously arrive with the Data Strobe switch.

The following graph shows the time lapse that must be assigned to these signal for correct functioning.

No more than 128μs must pass between one Data Strobe transition and the next during transmission of the 8 groups of data or else synchronisation is lost due to the internal automatic reset generated after 128μs from the last Data Strobe transition causing the data to be misinterpreted.

One should wait for at least 9μs after the forced-zero-cross command has been given between the last group of data of one instruction and the first group of the next.



The degree of priority of the channel and the number of channels in use at that moment must be taken into account in order to shorten this wait. If there is maximum priority the wait will be a minimum wait of approximately 2μs. The same holds if the priority is not maximum but there are no other channels in use. There will however be a maximum wait of 2μs for each active channel with greater priority than the channel in question.

If another instruction were to be transmitted without a sufficient wait, there would be the risk of losing the previous instruction of forced zero cross.

The wait is unnecessary after normal commands.

Every data group must be remain present for at least 1μs after Data Strobe transition.

The 48 bit functions are the following:

A) 8 address bits for the 1st table (ext. ROM)
B) 8 address bits for the 2nd table (ext. ROM)
C) 8 frequency bits (4-note and 4-twelfths of note and ± 1 or 2/1000)
D) 6 attenuation or amplitude address bits
E) 4 interpolation bits
F) 4 channel address bits
G) 6 reading mode and table length bits (ext. ROM)
H) 2 bits for choice between four outputs
I) 1 bit for a frequency octave change
J) 1 bit for gradual disenable of envelope

While waiting for the present 1st reading cycle to terminate, the above data (not immediately operational) is memorized into the internal RAM1).

The data is transfered to the addressed channel and made operational when the table address crosses through zero.

An exception is made by the 8 frequency bits and those varying the frequency octave as they operate immediately (See synchronization).

All data may be made operational by giving the forced-zero-cross command.

48 PROGRAMMING BIT FOR CHANNEL SELECTION

8 Address Bits 1st Table (ext. ROM)

These determine the most significant part of the 13 external memory address bits but according to the table length chosen by the 6 mode bits, some of the least significant of these 8 bits are suitably substituted by the M114S.

In the case of a maximum table length, 2048 bytes, there will only be 2 significant bits to address the table while the remaining 11 will address each single table word.

48 CHANNEL PROGRAMMING BIT DESCRIPTION (continued)

By already knowing the table length, the programmer will be able to programme the most significant bits needed for table address only and ignore the others.
As the maximum memory that can be handled is of 8Kbytes, if the table has a length of 1Kbyte it is sufficient to programme the three most signifícant bits and ignore the other five.

8 Address Bits 2nd Table (ext. ROM)
As above but refering to the second table.
One must consider that the zero-cross refers to the first table and that during table mixing the second table may assume a percentage value of zero while tha first table can only assume a minimum percentage value of 1/16 of the maximum value.

8 Frequency Bits
The 4 most significant bits characterize one of the 15 available notes with HEX. Codes from 0 to E. Eleven movements in twelfths of a semitone may be obtained with the remaining 4 bits as well as 4 ± 1/1000 and ± 2/1000 note frequency variations.
These permit the production of: Vibrato, Glissando, Effetto coro, etc...
The FF codes correspond to the forced-zero-cross command while FC maintains the previous frequency. F9, FA, FB are synchronization commands. The remaining codes are used for testing and therefore must not be used by the operator.
Table 1 shows the 240 frequencies obtainable by setting the external clock to 4MHz and the table length to 16 bytes, with single reading and without inserting an octave divisor. These are the highest octave frequencies obtainable with the M114S.
In practice double, quadruple, etc...frequencies may be obtained by writing 2, 4, etc. complete waveform periods in the table.

6 Attenuation Bits
These determine the attenuation addresses present at the output signal, to the internal table. The contents of this table follow a logarithmic pattern so as to produce a decrease of 0.75dB for each address unit increment. See table 2. The word length if of 10 bits.
Previous processing by a suitable circuit in order to obtain a gradual amplitude variation links the ten outputs of this table to the 10 bit output attenuator.
The gradual movement from the present level to that just programmed takes place by increasing or decreasing the 8 most significant bits of the attenuation table contents, with the same frequency with which the external memory tables are being scanned if the difference in level is greater than 128 steps, or with 1/2 of this frequency if greater than 64 steps, or 1/4 if greater than 32, or 1/8 if smaller than or equal to 32. In conclusion, output signal amplitude increases of decreases at each variation by 1/256 of the maximum value.
By setting the bit that deals with the gradual envelope there is an immediate passage from the present level to that programmed.

4 Interpolation Bits
These define the mixing coefficient between the two waveform tables.
It is possible in this way to sum the 1st waveform percentage with the remaining 2nd waveform percentage thus obtaining a third signal which will be forward to the output.
In greater detail, the operation carried out is the following:

$$D = (D1 * (K + 1)/16) + (D2 * (15 - K)/16)$$

where:
- D is the data at the output to the DAC (8 bits in complement with 2)
- D1 is the data read from the 1st table (8 bits in complement with 2)
- D2 is the data read from the 2nd table (8 bits in complement with 2)
- K is a 4 bit interpolation coefficient (from 0 to 15)

Obviously only the first waveform will be output if K = 15.

4 Channel Address Bits
These indicate to which of the 16 M114S channels the remaining 44 bits will be forwarded.

6 Mode Bits
These indicate the table couple reading mode (ext. ROM).
For each table there are 58 distinct combinations that include both table lengths and the number of repeated readings from the same address. (ext. ROM). See table N. 3.
The three most significant bits characterize the table lengths while the other three characterise the length ratio between tables and the number of repeated readings.

2 Output Address Bits
These indicate to which of the 4 output pins the corresponding channel signal must be forwarded. This is necessary in order to obtain stereophonic effect or to separate channels used for accompanyment from those of "SOLO", etc...

1 Octave Divisor Bit
This is used to pass from one octave to another without changing the table length.

1 Instant ENVELOPE Change Bit
This orders instant passage from the present amplitude to that programmed.

TABLE 1 – FREQUENCIES

NOTE	DEVIATION	-6/12	-5/12	-4/12	-3/12	-2/12	-1/12	-2/1000	-1/1000
	(Hex)	0	1	2	3	4	5	6	7
C	0	1016.78	1021.45	1026.69	1031.46	1036.27	1041.67	1044.39	1045.48
C#	1	1077.01	1082.25	1087.55	1092.90	1098.30	1103.14	1106.81	1107.42
D	2	1140.90	1146.79	1152.07	1158.08	1163.47	1168.91	1172.33	1173.71
D#	3	1209.19	1215.07	1221.00	1226.99	1232.29	1238.39	1242.24	1243.01
E	4	1281.23	1287.00	1293.66	1299.55	1305.48	1312.34	1315.79	1317.52
F	5	1356.85	1363.33	1369.86	1376.46	1383.13	1389.85	1393.73	1395.67
F#	6	1437.81	1445.09	1451.38	1458.79	1466.28	1472.75	1477.10	1478.20
G	7	1523.23	1530.22	1538.46	1545.60	1552.80	1560.06	1564.95	1566.17
G#	8	1614.21	1622.06	1629.99	1638.00	1644.74	1652.89	1658.37	1659.75
A	9	1709.40	1718.21	1727.12	1734.61	1743.68	1751.31	1755.93	1757.47
A#	A	1811.59	1819.84	1829.83	1838.24	1846.72	1855.29	1860.47	1862.20
B	B	1919.39	1928.64	1937.98	1947.42	1956.95	1966.57	1972.39	1974.33
2C	C	2032.52	2042.90	2053.39	2063.98	2072.54	2083.33	2089.86	2089.86
2C#	D	2155.17	2164.50	2176.28	2185.79	2195.39	2207.51	2212.39	2214.84
2D	E	2283.11	2293.58	2304.15	2314.81	2325.58	2339.18	2344.67	2347.42
	F	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing

NOTE	DEVIATION	0	+1/1000	+2/1000	+1/12	+2/12	+3/12	+4/12	+5/12
	(Hex)	8	9	A	B	C	D	E	F
C	0	1046.57	1047.67	1048.77	1051.52	1056.52	1061.57	1066.67	1071.81
C#	1	1108.65	1109.88	1111.11	1114.21	1119.19	1124.86	1130.58	1135.72
D	2	1174.40	1175.78	1177.16	1180.64	1186.24	1191.90	1197.60	1203.37
D#	3	1244.56	1246.11	1246.88	1250.78	1256.28	1262.63	1269.04	1274.70
E	4	1318.39	1320.13	1321.00	1324.50	1331.56	1337.79	1344.09	1350.44
F	5	1396.65	1398.60	1399.58	1403.51	1410.44	1417.43	1424.50	1430.62
F#	6	1480.38	1481.48	1482.58	1486.99	1494.77	1501.50	1508.30	1516.30
G	7	1567.40	1569.86	1571.09	1576.04	1583.53	1591.09	1598.72	1606.43
G#	8	1661.13	1662.51	1663.89	1669.45	1677.85	1684.92	1693.48	1702.13
A	9	1760.56	1762.11	1763.67	1768.35	1777.78	1785.71	1793.72	1803.43
A#	A	1863.93	1865.67	1869.16	1874.41	1883.24	1892.15	1901.14	1910.22
B	B	1976.28	1978.24	1980.20	1984.13	1994.02	2004.01	2014.10	2024.29
2C	C	2092.05	2094.24	2096.44	2103.05	2114.16	2123.14	2134.47	2143.62
2C#	D	2217.29	2219.76	2222.22	2227.17	2239.64	2249.72	2259.89	2272.73
2D	E	2350.18	2352.94	2352.94	2361.28	2372.48	2383.79	2395.21	2406.74
	F	For Testing	RSG	RSS	SSG	Previously Selected Frequency	For Testing	For Testing	Forced Zero Cross

TABLE 2 – ATTENUATION

ATTENUATION ADDRESS						OUTPUT ROM	ATTENUATION
A5	A4	A3	A2	A1	A0	DECIMAL	- dB
0	0	0	0	0	0	1024	0.00
0	0	0	0	0	1	939	0.75
0	0	0	0	1	0	862	1.50
0	0	0	0	1	1	790	2.25
0	0	0	1	0	0	725	3.00
0	0	0	1	0	1	665	3.75
0	0	0	1	1	0	610	4.50
0	0	0	1	1	1	559	5.26
0	0	1	0	0	0	513	6.00
0	0	1	0	0	1	471	6.75
0	0	1	0	1	0	432	7.50
0	0	1	0	1	1	396	8.25
0	0	1	1	0	0	363	9.01
0	0	1	1	0	1	333	9.76
0	0	1	1	1	0	306	10.49
0	0	1	1	1	1	281	11.23
0	1	0	0	0	0	257	12.01
0	1	0	0	0	1	236	12.75
0	1	0	0	1	0	216	13.52
0	1	0	0	1	1	199	14.23
0	1	0	1	0	0	182	15.00
0	1	0	1	0	1	167	15.75
0	1	0	1	1	0	153	16.51
0	1	0	1	1	1	141	17.22
0	1	1	0	0	0	129	17.99
0	1	1	0	0	1	118	18.77
0	1	1	0	1	0	108	19.54
0	1	1	0	1	1	99	20.29
0	1	1	1	0	0	91	21.03
0	1	1	1	0	1	84	21.72
0	1	1	1	1	0	77	22.48
0	1	1	1	1	1	70	23.30
1	0	0	0	0	0	65	23.95
1	0	0	0	0	1	59	24.79
1	0	0	0	1	0	54	25.56
1	0	0	0	1	1	50	26.23
1	0	0	1	0	0	46	26.95
1	0	0	1	0	1	42	27.74
1	0	0	1	1	0	38	28.61
1	0	0	1	1	1	35	29.32
1	0	1	0	0	0	32	30.10
1	0	1	0	0	1	29	30.96
1	0	1	0	1	0	27	31.58
1	0	1	0	1	1	25	32.25
1	0	1	1	0	0	23	32.97
1	0	1	1	0	1	21	33.76
1	0	1	1	1	0	19	34.63
1	0	1	1	1	1	17	35.60
1	1	0	0	0	0	15	36.68
1	1	0	0	0	1	14	37.28
1	1	0	0	1	0	13	37.93
1	1	0	0	1	1	12	38.62
1	1	0	1	0	0	11	39.38
1	1	0	1	0	1	10	40.21
1	1	0	1	1	0	9	41.12
1	1	0	1	1	1	8	42.14
1	1	1	0	0	0	7	43.30
1	1	1	0	0	1	6	44.64
1	1	1	0	1	0	5	46.23
1	1	1	0	1	1	4	48.16
1	1	1	1	0	0	3	50.66
1	1	1	1	0	1	2	54.19
1	1	1	1	1	0	1	61.21
1	1	1	1	1	1	0	Max.

TABLE 3 – READING MODES

MODE						Length		Length	N° of Table Reads	
M2	M1	M0	L2	L1	L0	1st Table		2nd Table	1st Table	2nd Table
0	0	0	0	0	0	16		16	2	2
0	0	0	0	0	1	32		32	2	2
0	0	0	0	1	0	64		64	2	2
0	0	0	0	1	1	128	(1/1)	128	2	2
0	0	0	1	0	0	256		256	2	2
0	0	0	1	0	1	512		512	2	2
0	0	0	1	1	0	1024		1024	2	2
0	0	0	1	1	1	2048		2048	2	2
0	0	1	0	0	0	16		16	1	1
0	0	1	0	0	1	32		32	1	1
0	0	1	0	1	0	64		64	1	1
0	0	1	0	1	1	128	(1/1)	128	1	1
0	0	1	1	0	0	256		256	1	1
0	0	1	1	0	1	512		512	1	1
0	0	1	1	1	0	1024		1024	1	1
0	0	1	1	1	1	2048		2048	1	1
0	1	0	0	0	0	16		16	4	4
0	1	0	0	0	1	32		32	4	4
0	1	0	0	1	0	64		64	4	4
0	1	0	0	1	1	128	(1/1)	128	4	4
0	1	0	1	0	0	256		256	4	4
0	1	0	1	0	1	512		512	4	4
0	1	0	1	1	0	1024		1024	4	4
0	1	0	1	1	1	1024		1024	4	4
0	1	1	0	0	0	16		16	1	1 *
0	1	1	0	0	1	32		16	1	1
0	1	1	0	1	0	64		32	1	1
0	1	1	0	1	1	128	(2/1)	64	1	1
0	1	1	1	0	0	256		128	1	1
0	1	1	1	0	1	512		256	1	1
0	1	1	1	1	0	1024		512	1	1
0	1	1	1	1	1	2048		1024	1	1
1	0	0	0	0	0	16		8	1	2
1	0	0	0	0	1	32		16	1	2
1	0	0	0	1	0	64		32	1	2
1	0	0	0	1	1	128	(2/1)	64	1	2
1	0	0	1	0	0	256		128	1	2
1	0	0	1	0	1	512		256	1	2
1	0	0	1	1	0	1024		1024	1	2
1	0	0	1	1	1	2048		1024	1	2
1	0	1	0	0	0	16		16	1	1 *
1	0	1	0	0	1	32		16	1	1 *
1	0	1	0	1	0	64		16	1	1
1	0	1	0	1	1	128	(4/1)	32	1	1
1	0	1	1	0	0	256		64	1	1
1	0	1	1	0	1	512		128	1	1
1	0	1	1	1	0	1024		256	1	1
1	0	1	1	1	1	2048		512	1	1
1	1	0	0	0	0	16		4	1	4
1	1	0	0	0	1	32		8	1	4
1	1	0	0	1	0	64		16	1	4
1	1	0	0	1	1	128	(4/1)	32	1	4
1	1	0	1	0	0	256		64	1	4
1	1	0	1	0	1	512		128	1	4
1	1	0	1	1	0	1024		256	1	4
1	1	0	1	1	1	2048		512	1	4

TABLE 3 – READING MODES (continued)

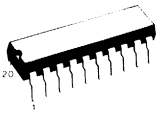
MODE						Length		Length	N° of Table Reads	
M2	M1	M0	L2	L1	L0	1st Table		2nd Table	1st Table	2nd Table
1	1	1	0	0	0	16		16	1	1 *
1	1	1	0	0	1	32		16	1	1 *
1	1	1	0	1	0	64		16	1	1 *
1	1	1	0	1	1	128	(8/1)	16	1	1
1	1	1	1	0	0	256		32	1	1
1	1	1	1	0	1	512		64	1	1
1	1	1	1	1	0	1024		128	1	1
1	1	1	1	1	1	2048		256	1	1

* Repetitions.

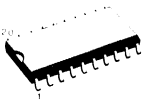
M3004
M3005

REMOTE CONTROL TRANSMITTERS

- FLASHED OR MODULATED TRANSMISSIONS (M3004 = $f_{osc/12}$, M3005 = f_{osc})
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (I_{OH} = -40mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- "LOCK-UP" PROTECTION TO PREVENT BATTERY DISCHARGE
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 2mA AT 6V SUPPLY
- WIDE SUPPLY VOLTAGE RANGE (4 TO 10.5V)
- CERAMIC RESONATOR CONTROLLED FREQUENCY (400 TO 600KHz)
- CMOS SI-GATE TECHNOLOGY
- PACKAGES: 20-LEAD PLASTIC DIL OR 20-LEAD PLASTIC SMALL OUTLINE (SO-20)



B
DIP-20 Plastic
(0.4)



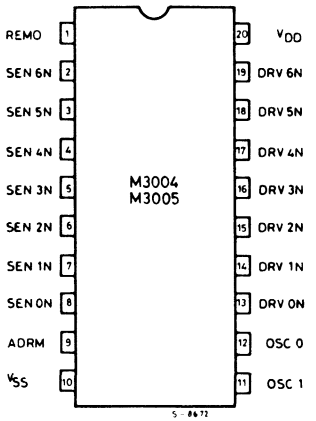
M
SO-20L

ORDERING NUMBERS: M3004 B1
M3005 B1
M3004 M1
M3005 M1

DESCRIPTION

The M3004/M3005 transmitter ICs are designed for infrared remote control systems. They have a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.
The M3004/M3005 generate the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated.
Modulated pulses allow receivers with narrowband preamplifier for improved noise rejection to be used. In the M3004 the modulation frequency is $f_{osc/12}$ about 38KHz with (f_{osc} = 455KHz) while in the M3005 the modulation frequency corresponds to f_{osc}. In flash mode the M3004 and M3005 are identical. Flashed pulses require a wideband preamplifier within the receiver.

PIN CONNECTIONS



PIN NAMES

1	REMO	Remote data output	11	OSCI	Oscillator input
2	SEN6N	Key matrix sense inputs	12	OSCO	Oscillator output
3	SEN5N		13	DRV0N	Key matrix drive outputs
4	SEN4N		14	DRV1N	
5	SEN3N		15	DRV2N	
6	SEN2N		16	DRV3N	
7	SEN1N		17	DRV4N	
8	SEN0N		18	DRV5N	
9	ADRM	Address mode control inputs	19	DRV6N	
10	V_{SS}	Ground	20	V_{DD}	Positive supply

ABSOLUTE MAXIMUM RATINGS

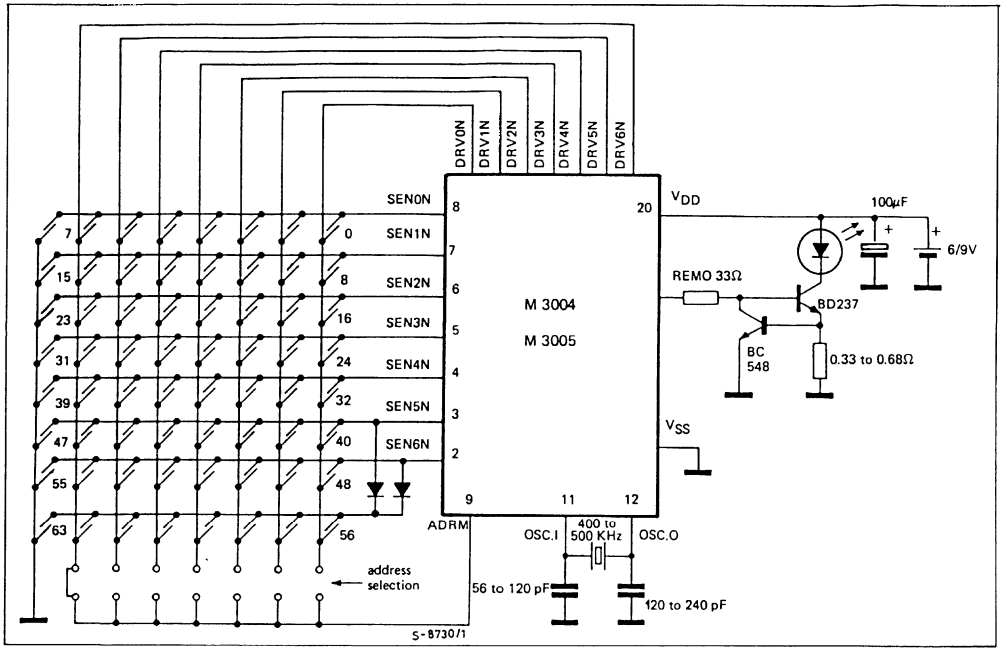
Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage range	-0.3 to + 12	V
V_i	Input voltage range	-0.3 to V_{DD} + 0.3	V
V_O	Output voltage range	-0.3 to V_{DD} + 0.3	V
± I	D.C. current into any input or output	max. 10	mA
I_{REMO}	Peak REMO output current during 10μs; duty factor = 1%	max. -300	mA
P_{tot}	Power dissipation per package for T_{amb} = 0 to 70°C	max. 200	mW
T_{stg}	Storage temperature range	-55 to 150	°C
T_{amb}	Operating ambient temperature range	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (V_{SS} = 0V; T_{amb} = 25°C; unless otherwise specified)

Symbol	V_{DD} (V)	Parameter	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	–	Supply voltage T_{amb} = 0 to +70°C	4	–	10.5	V
I_{DD}	6 9	Supply current; active f_{osc} = 455KHz; REMO output unloaded	– –	0.4 0.8	– –	mA
I_{DD}	6 9	Supply current; inactive (stand-by mode) T_{amb} = 25°C	– –	– –	2 2	µA
f_{osc}	4 to 11	Oscillator frequency (ceramic resonator)	400	–	600	KHz
KEYBOARD MATRIX						
		Inputs SEN0N to SEN6N				
V_{IL}	4 to 11	Input voltage LOW	–	–	0.2 x V_{DD}	V
V_{IH}	4 to 11	Input voltage HIGH	0.8 x V_{DD}	–	–	V
I_I	4 11	Input current V_I = 0V	-10 -30	– –	-100 -300	µA
I_I	11	Input leakage current $V_I = V_{DD}$	–	–	1	µA
		Outputs DRV0N to DRV6N				
V_{OL}	4 11	Output voltage "ON" I_O = 0.1mA I_O = 1.0mA	– –	– –	0.3 0.5	V
I_O	11	Output current "OFF" V_O = 11V	–	–	10	µA
CONTROL INPUT ADRM						
V_{IL}	–	Input voltage LOW	–	–	0.2 x V_{DD}	V
V_{IH}	–	Input voltage HIGH	0.8 x V_{DD}	–	–	V
		Input current (switched P and N-channel pull-pu/pull-down)				
I_{IL}	4 11	Pull-up active stand-by voltage: 0V	-10 -30	– –	-100 -300	µA
I_{IH}	4 11	Pull-down active stand-by voltage: V_{DD}	10 30	– –	100 300	µA
DATA OUTPUT REMO						
V_{OH}	6 9	Output voltage HIGH $-I_{OH}$ = 40mA	3 6	– –	– –	V
V_{OL}	6 9	Output voltage LOW I_{OL} = 0.3mA	– –	– –	0.2 0.1	V
t_{OH}	6	Pulse length oscillator stopped	–	–	1	ms
OSCILLATOR						
I_I	6	Input current OSCI at V_{DD}	0.8	–	2.7	µA
V_{OH}	6	Output voltage HIGH $-I_{OL}$ = 0.1mA	–	–	V_{DD} -1	V
V_{OL}	6	Output voltage LOW I_{OH} = 0.1mA	–	–	1	V

Fig. 1 - Transmitter with M3004/M3005



INPUTS AND OUTPUTS

KEY MATRIX INPUTS AND OUTPUTS (DRV0N TO DRV6N AND SEN0N TO SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE AND TRANSMISSION MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 5. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or con-

INPUTS AND OUTPUTS (continued)

nected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format are listed in Table 1 and 2 (M3004), 3 and 4 (M3005).

The information is defined by the distance t_B between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2, 3 and 4. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Table 5 and 6.

The REMO output is protected against "lock-up", i.e. the lenght of an output pulse is limited to $<$ 1ms even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (OSCI AND OSCO)

The external components must be connected to these pin when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400KHz and 600KHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

KEYBOARD OPERATION

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 5) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 6) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new

FUNCTIONAL DESCRIPTION (continued)

output at REMO (see Fig. 6). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

- The keys switching to ground (code numbers 7, 15. 23. 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line because this condition has been used for the definition of additional codes (code numbers 50 to 63).

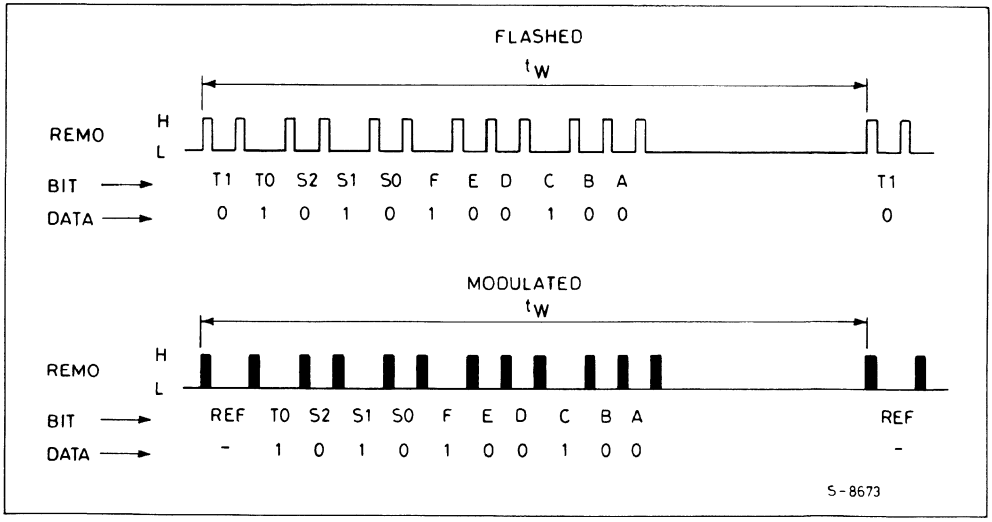
OUTPUT SEQUENCY (DATA FORMAT)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed.

The format of the output pulse train is given in Figs. 2, 3 and 4. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 5). The toggle bits remain unchanged within a multiple key-stroke sequence.

Fig. 2 - Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = sub-system address; A, B, C, D, E and F = command bits.



- Flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
- Modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

FUNCTIONAL DESCRIPTION (continued)

Fig. 3 - REMO output waveforms (M3004)

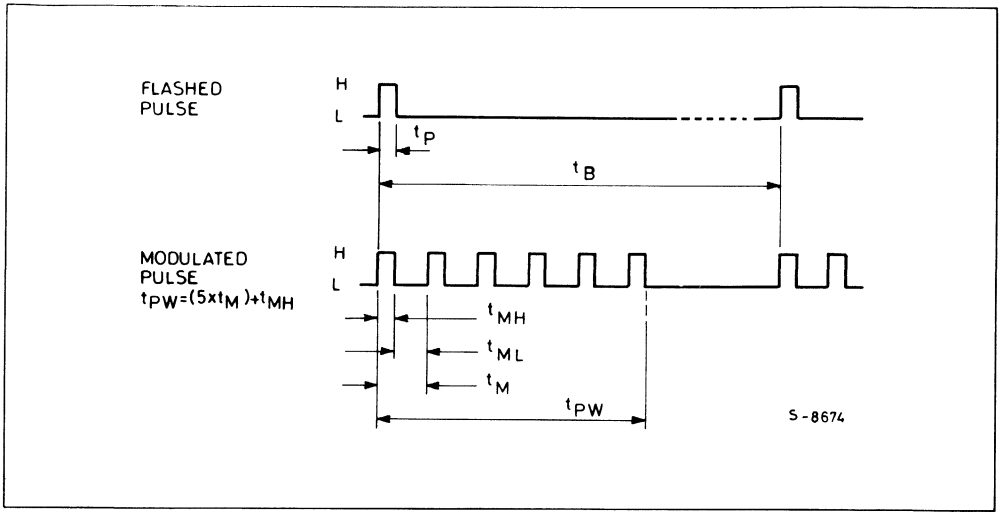


Table 1 - Pulse train timing (M3004); f_{osc} = 455KHz

Mode	T_o ms	t_P µs	t_M µs	t_{ML} µs	t_{MH} µs	t_W ms
Flashed (f_{osc} = 455KHz)	2.53	8.8	–	–	–	121
Modulated (f_{osc} = 455KHz)	2.53	–	26.4	17.6	8.8	121

f_{osc}	455KHz	t_{osc} = 2.2µs
t_P	4 x t_{osc}	flashed pulse width
t_M	12 x t_{osc}	modulation period
t_{ML}	8 x t_{osc}	modulation period LOW
t_{MH}	4 x t_{osc}	modulation period HIGH
T_o	1152 x t_{osc}	basic unit of pulse distance
t_W	55 196 x t_{osc}	word distance

Table 2 - Pulse train separation (t_B) (M3004)

Code	t_B
Logic "0"	2 x T_o
Logic "1"	3 x T_o
Reference time	3 x T_o
Toggle bit time	2 x T_o or 3 x T_o

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - REMO output waveforms (M3005)

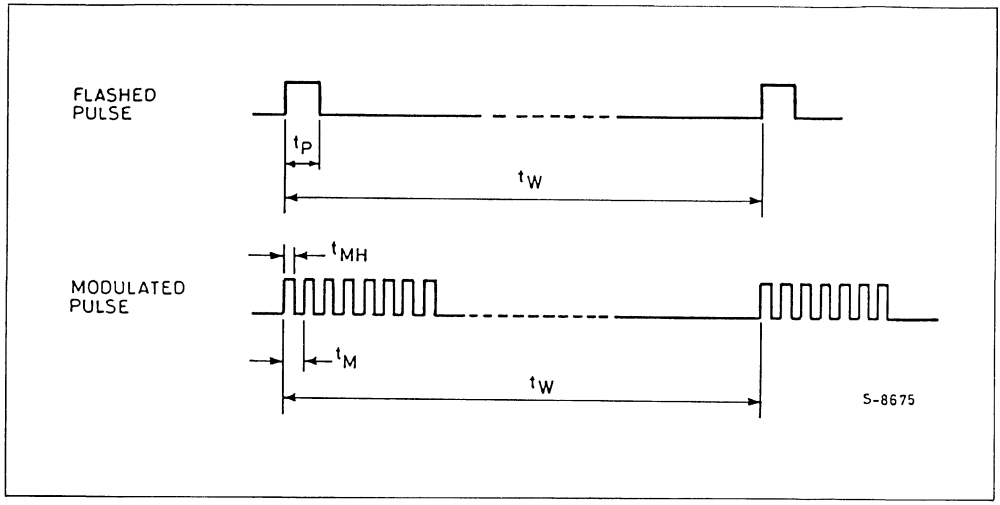


Table 3 - Pulse train timing (M3005)

Mode	T_o ms	t_P µs	t_M µs	t_W ms
Flashed (f_{osc} = 455KHz)	2.53	8.8	–	121
Modulated (f_{osc} = 600KHz)	2.53	–	1.66	121

Table 4 - Pulse train separation (t_B) (M3005)

Code	t_B
Logic "0"	2 x T_o
Logic "1"	3 x T_o
Reference time	3 x T_o
Toggle bit time	2 x T_o or 3 x T_o

	Flashed mode (455 KHz)	**Modulated mode** (600KHz)	
t_{osc}	2,2µs	1.66µs	
t_P	4 x t_{osc}	–	flashed pulse width
t_M	–	t_{osc}	modulation period
N	–	8	number of modulation pulses
T_o	1152 x t_{osc}	1536 x t_{osc}	basic unit of pulse distance
t_W	55296 x t_{osc}	73728 x t_{osc}	word distance
t_{MH}/t_M	–	0.4 to 0.6	pulse duty cycle during carrier mode

NOTE – The different dividing ratio for I_O and t_W between fashed mode and modulated mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during modulated mode. This allows the use of a 600KHz ceramic resonator during modulated mode to obtain a better noise immunity for the receiver without a significant change in T_o and t_W.

FUNCTIONAL DESCRIPTION (continued)

Fig. 5 - Single key-stroke sequence. Debounce time: t_{DB} = 4 to 9 x T_o. Start time: t_{ST} = 5 to 10 x T_o. Minimum release time: t_{REL} = T_o. Word distance: t_W.

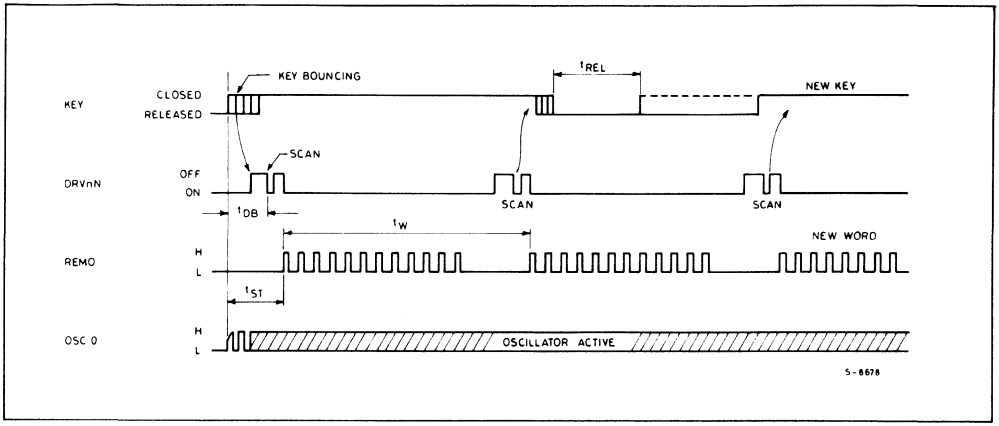


Fig. 6 - Multiple key-stroke sequence. Scan rate multiple key-stroke: t_{SM} = 8 to 10 x T_o. For t_{DB}, t_{ST} and t_W see Fig. 5.

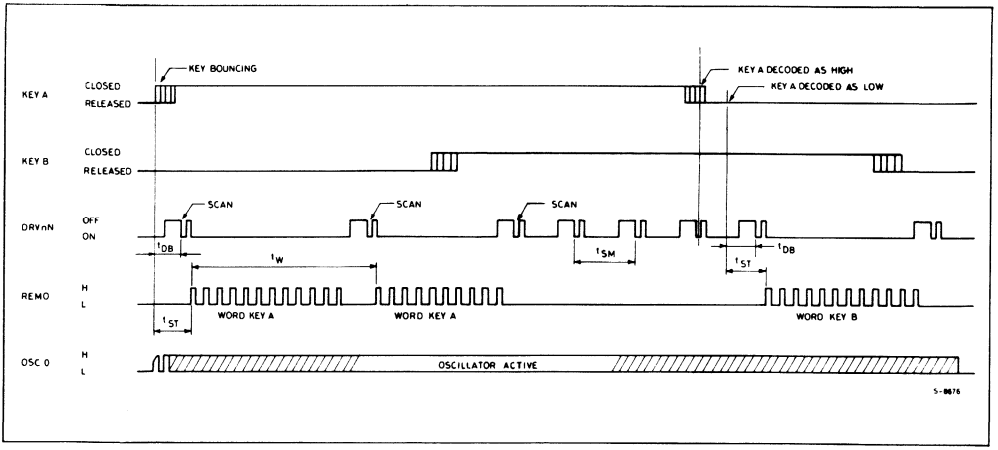


Table 5 - Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

Mode	Sub-system address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM blank = not connected to ADRM X = don't care

Table 6 - Key codes

Matrix drive	Matrix sense	Code F	E	D	C	B	A	Matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

M5450 M5451

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

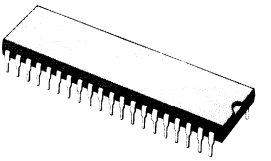
Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are pin-to-pin replacements of the NS MM 5450 and MM 5451.



DIP-40 Plastic

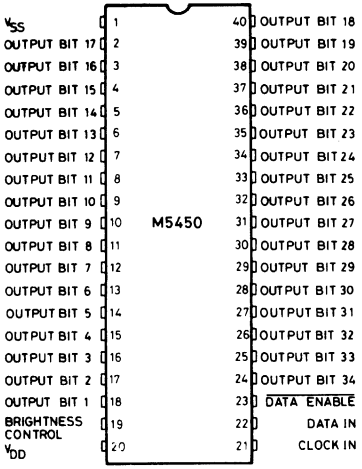
ORDERING NUMBERS: M5450 B7
M5451 B7

ABSOLUTE MAXIMUM RATINGS

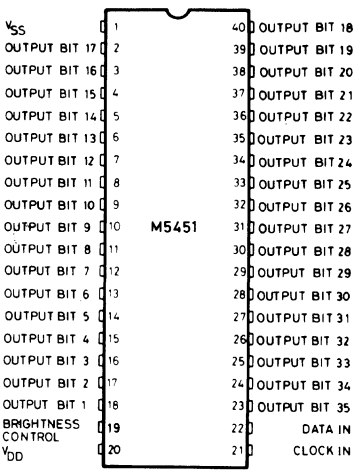
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAMS



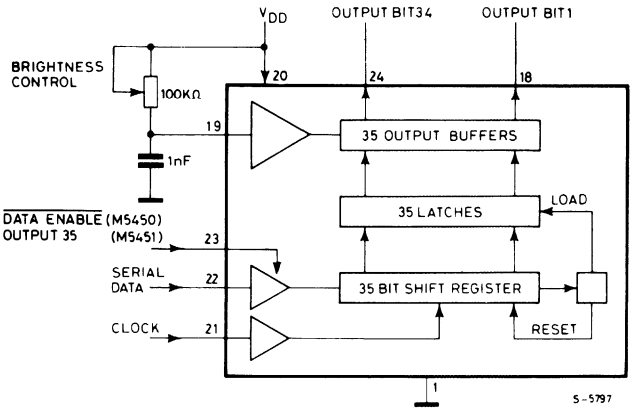
S-5795



S-5796

BLOCK DIAGRAM

Fig. 1



S-5797

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltage Logical "0" Level Logical "1" Level	± 10 μA input bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the M5450.

FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.
Figure 3 shows the timing relationship between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7\ \text{mA})\ ]\ (124\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
124°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

Fig. 2 - Input Data Format

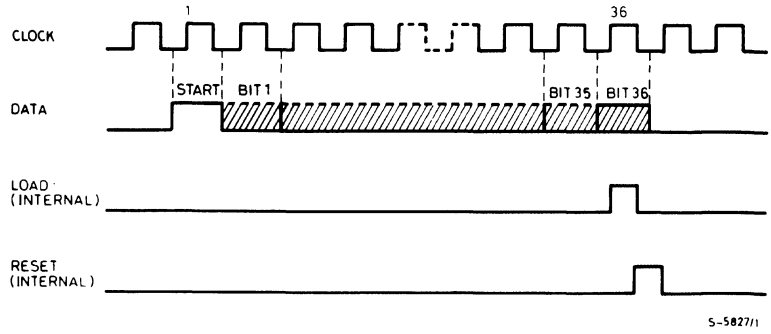


Fig. 3

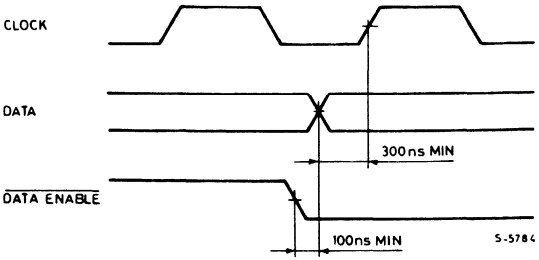


Fig. 4

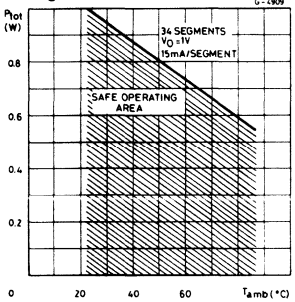


Fig. 5

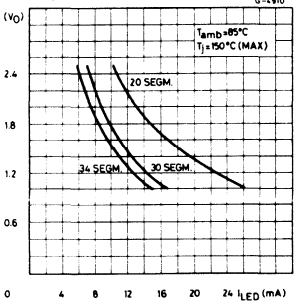
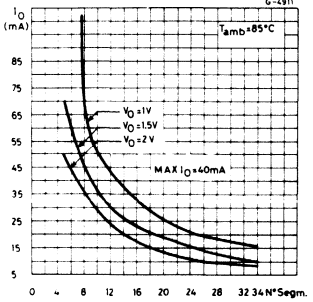
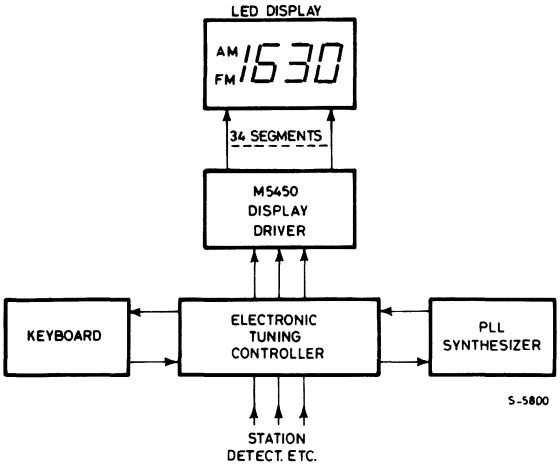


Fig. 6



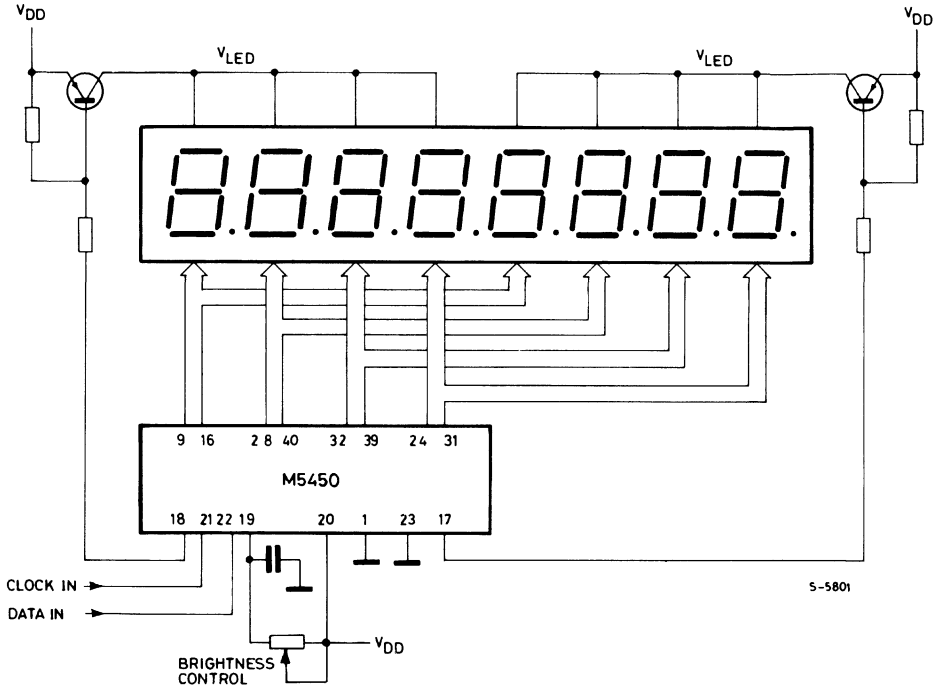
TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



TYPICAL APPLICATIONS (continued)

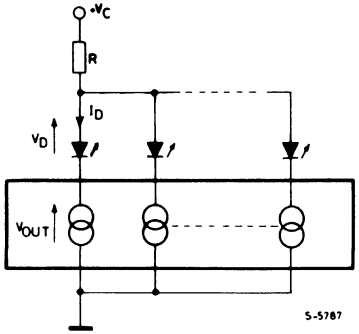
Duplexing 8 Digits with One M5450



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

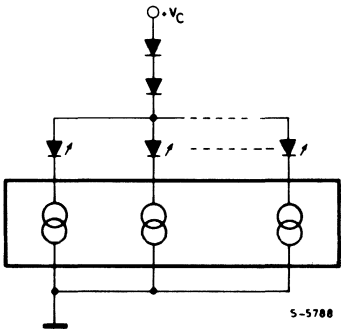


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

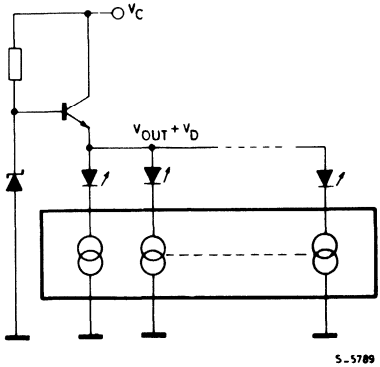
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

M5480

PRELIMINARY DATA

LED DISPLAY DRIVER

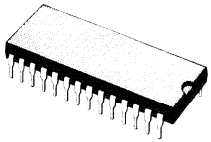
- 3½ DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5480 is a pin-to-pin replacement of the NS MM 5480.



DIP-28 Plastic

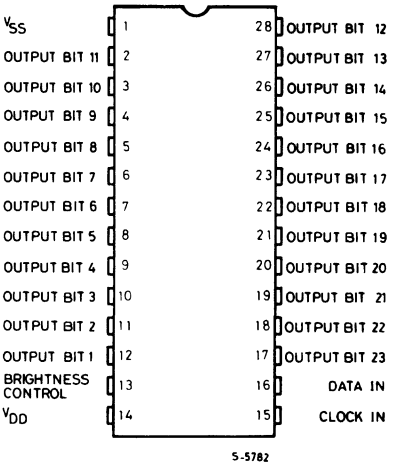
ORDERING NUMBER: M5480 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	940 mW
		at 85°C	490 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

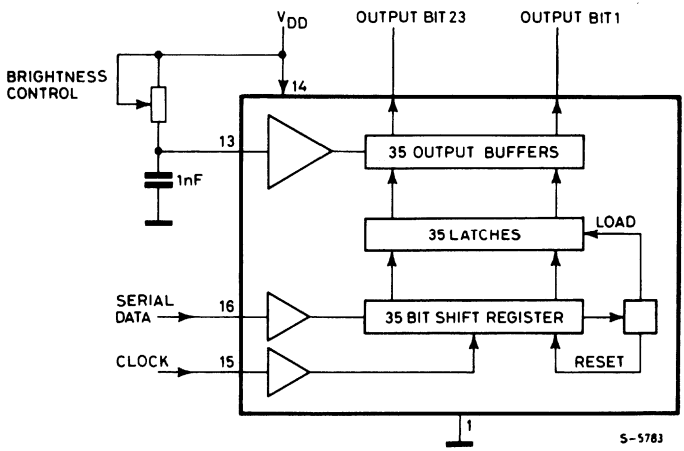
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3^1/_2$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (132\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

132°C/W = thermal coefficient of the package

T_{amb} = ambient temperature

Fig. 2 - Input Data Format

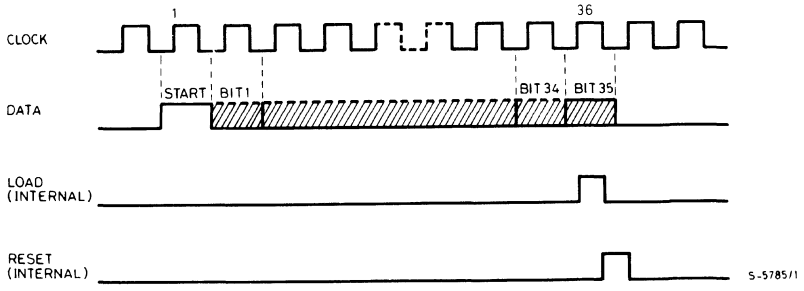


Fig. 3

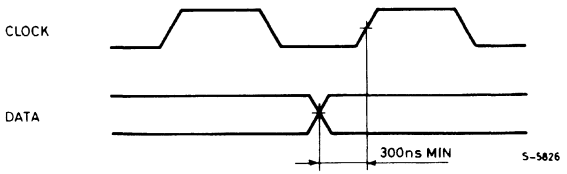
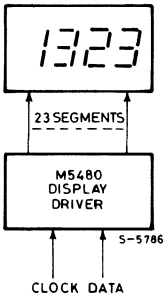


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

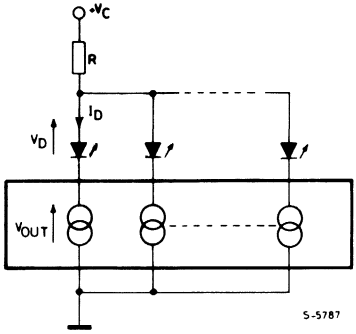
BASIC $3^1/_2$ Digit interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

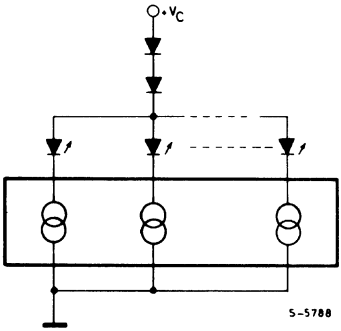


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{OUT\,MIN}}{N_{MAX} \cdot I_D}$$

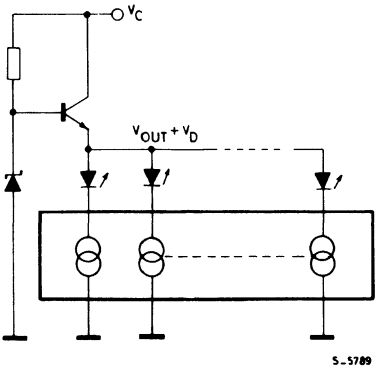
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

M5481

LED DISPLAY DRIVER

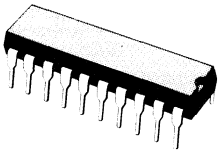
- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is a pin-to-pin replacement of the NS MM 5481.



DIP-20 Plastic
(0.25)

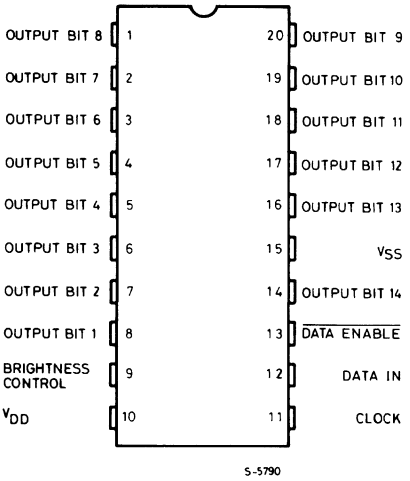
ORDERING NUMBER: M5481 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

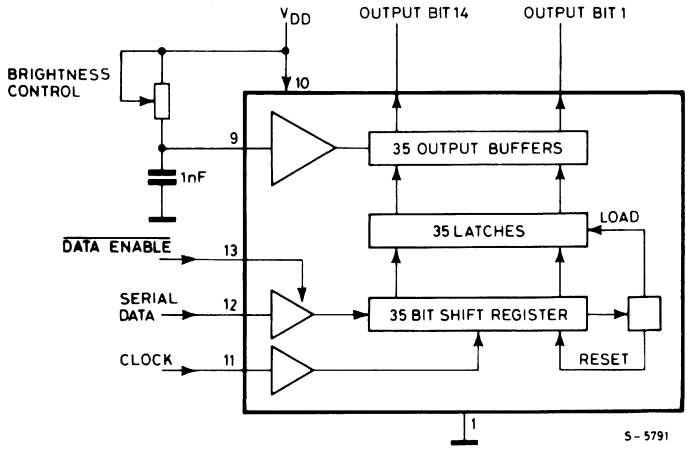
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculates as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
These is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ ^\circ\text{C/W}) + T_{amb}$$

where:
T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

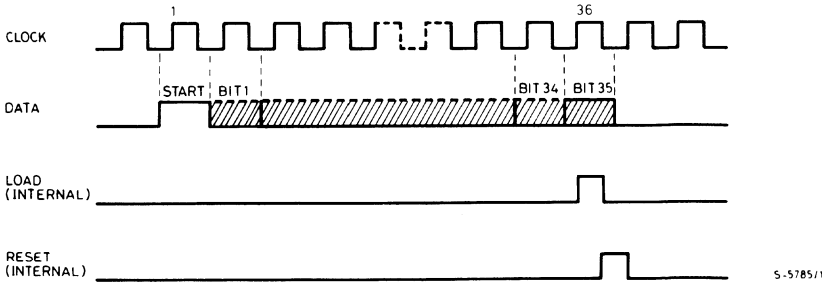


Fig. 3

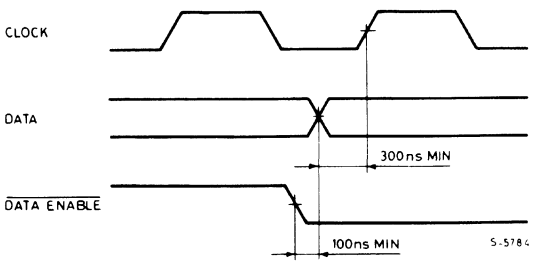
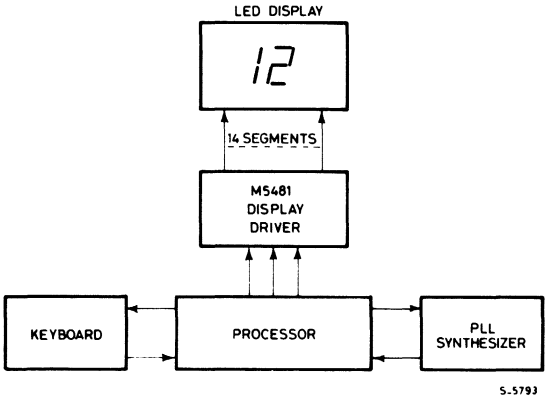


Fig. 4 - Serial Data Bus/Outputs Correspondence

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

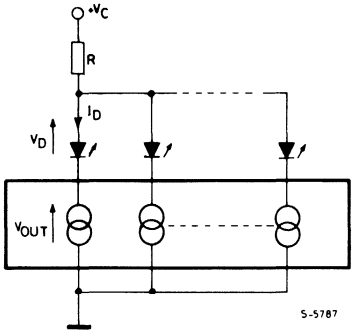
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

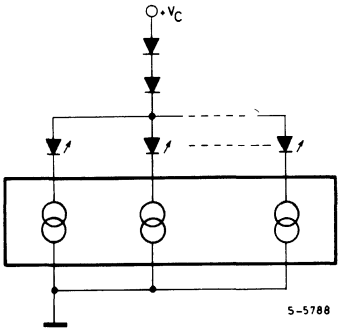


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{O\ MIN}}{N_{MAX} \cdot I_D}$$

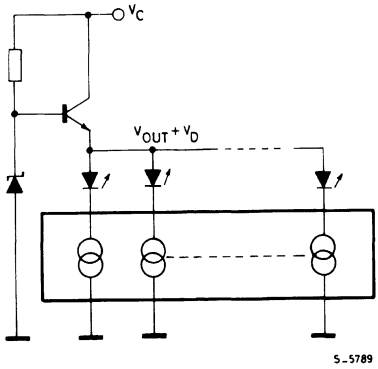
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

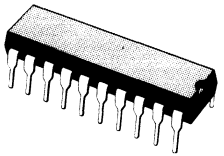
LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.



DIP-20 Plastic
(0.25)

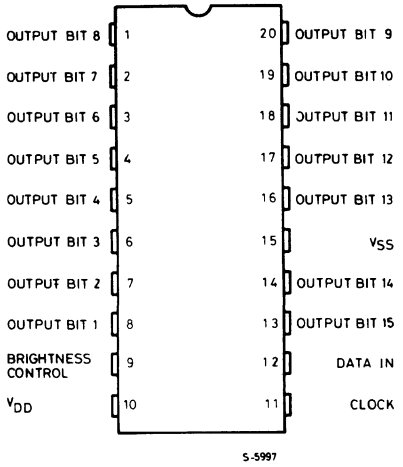
ORDERING NUMBER: M5482 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

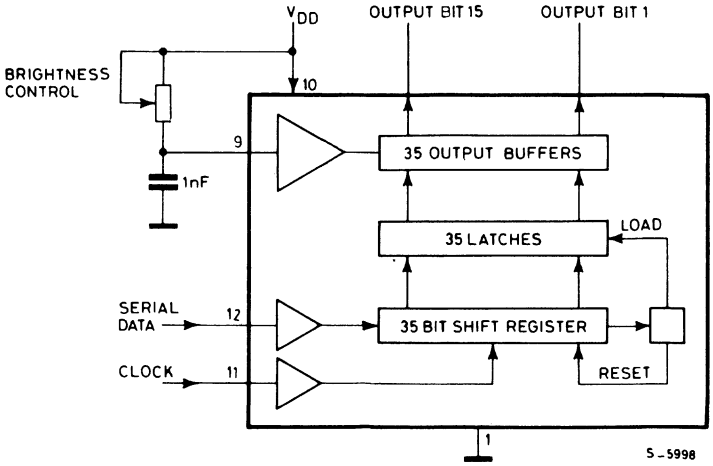
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ ^\circ\text{C/W}) + T_{amb}$$

where:
T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

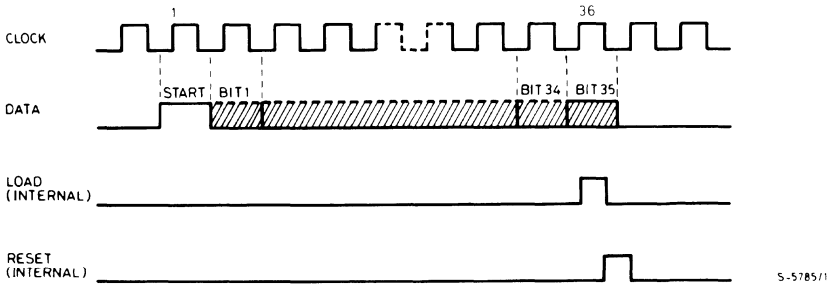


Fig. 3

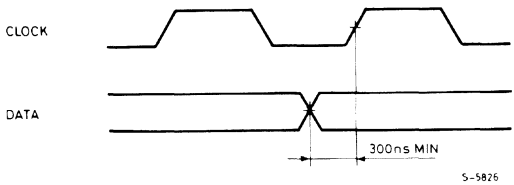
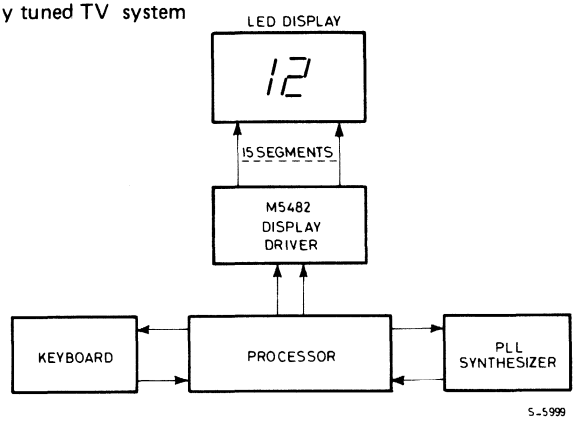


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

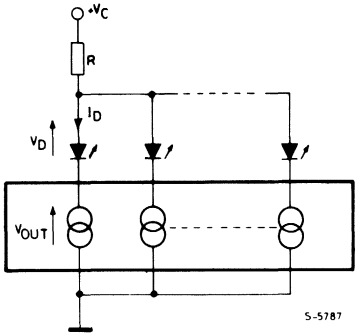
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

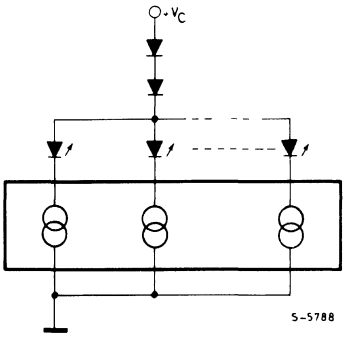


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{O\ MIN}}{N_{MAX} \cdot I_D}$$

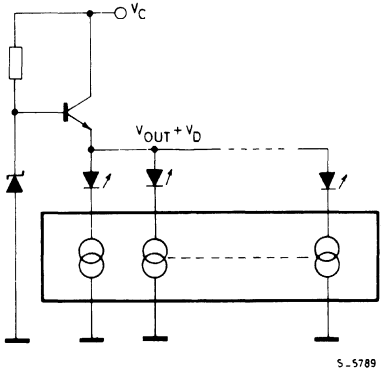
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



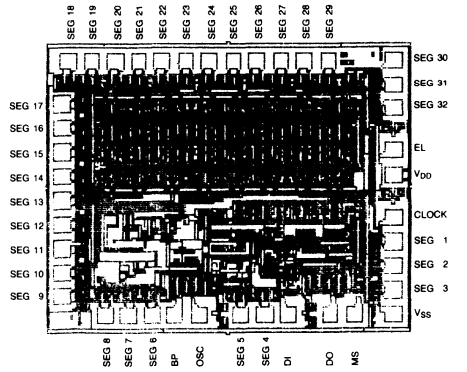
In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

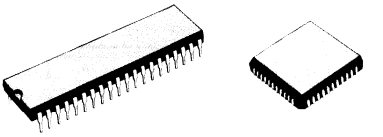
M8438A

SERIAL INPUT LCD DRIVER

- DATA TRANSFER: FIXED ENABLE MODE FOR DIP-40
- DRIVES UP TO 32 LCD SEGMENTS
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- CASCADABLE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- ON CHIP OSCILLATOR
- REQUIRES ONLY 3 CONTROL LINES
- −40 TO 85°C TEMPERATURE RANGE

The M8438A is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8438A can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8438A is available in DIE form, assembled in 40 pin dual-in line plastic or 44 PLCC packages.





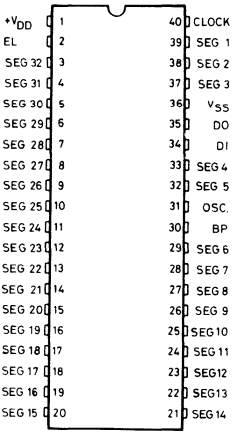
B DIP-40 Plastic

C 44 PLCC Plastic Chip Carrier

ORDERING NUMBERS: M8438A DIE 1
M8436A B6
M8436A C6

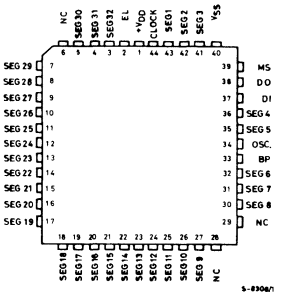
PIN CONFIGURATION

DUAL IN LINE



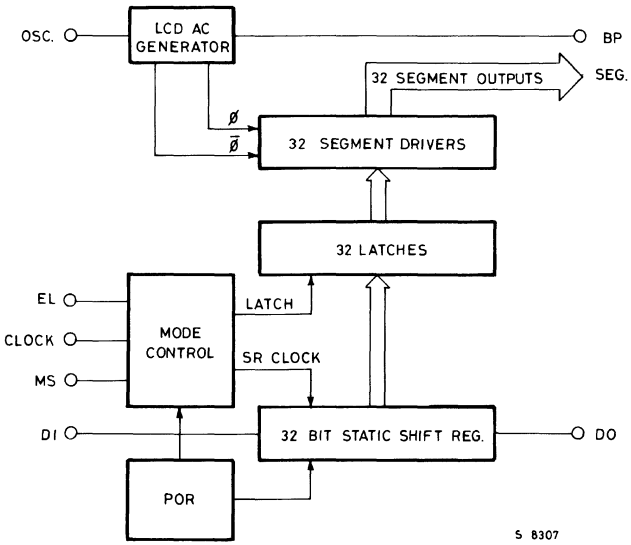
S-8309

CHIP CARRIER



S-8308/1

BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
MS :Mode select input (not available in 40 Pin DIL)
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	µA
I_Q	Quiescent Current		V_{DD} = 10V		10	µA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level	CLOCK DI EL		0	.2V_{DD}	V
I_{IN}	Input Current	CLOCK DI EL			±5	µA
C_I	Input Capacitance	CLOCK DI EL			5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level	OSC	Driven mode		.1V_{DD}	V
I_{IN}	Input Current	OSC	Driven mode		±10	µA
R_{ON}	Segment Output Impedance		I_{IL} = 10µA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100µA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100µA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

The circuit can operate in two different data transfer modes: Enable mode and latch mode. One of either mode can be chosen with the mode select input MS. An internal pull up device is provided between this input and VDD. Enable mode is selected if MS is left open or connected to VDD.
Latch mode is selected if MS is connected to VSS.
The input MS is not available, if the device is assembled in the 40 pin package, and is internally fixed to operate in ENABLE MODE.

ENABLE MODE

Fig. 3 shows a timing diagram of the enable mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted when the enable/latch control EL is high. When EL is low it causes the shift register clock to be inhibited and the content of the shift register to be loaded into the latches that control the segment drivers.

LATCH MODE

Fig. 4 shows a timing diagram of the latch mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

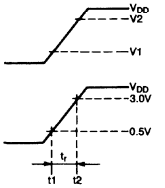
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s

c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 5 shows the connection scheme for a self oscillating configuration, figure 6 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of enable mode: set-up and hold time

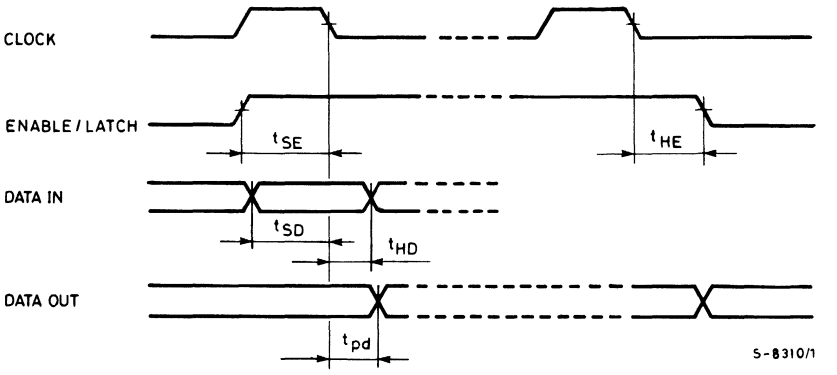


Fig. 2 - Timing diagram of latch mode: set-up and hold time

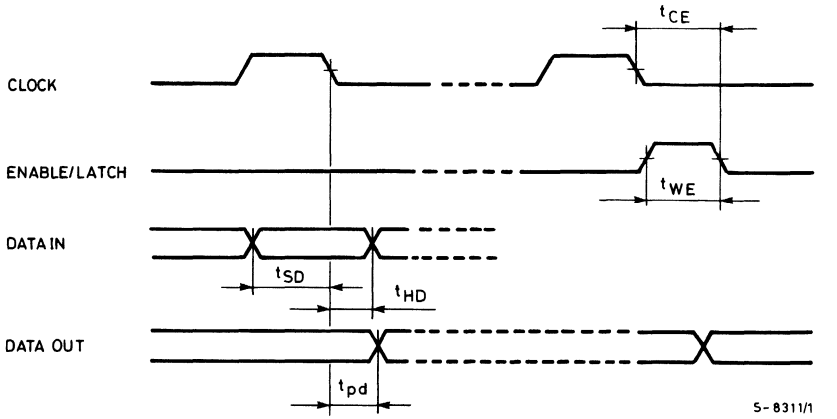


Fig. 3 - Timing diagram of enable mode: Serial load into SR and parallel transfer to LCD

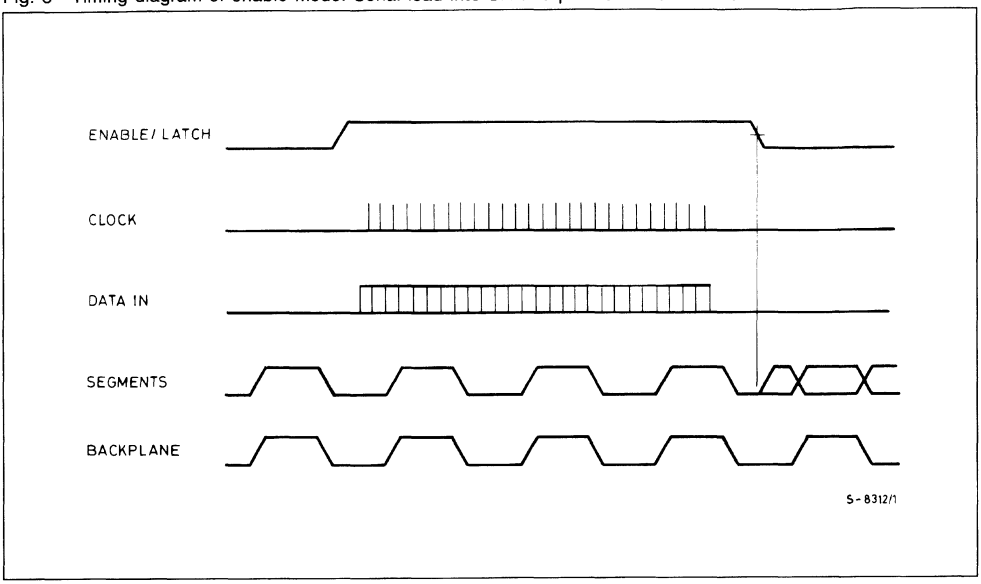


Fig. 4 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

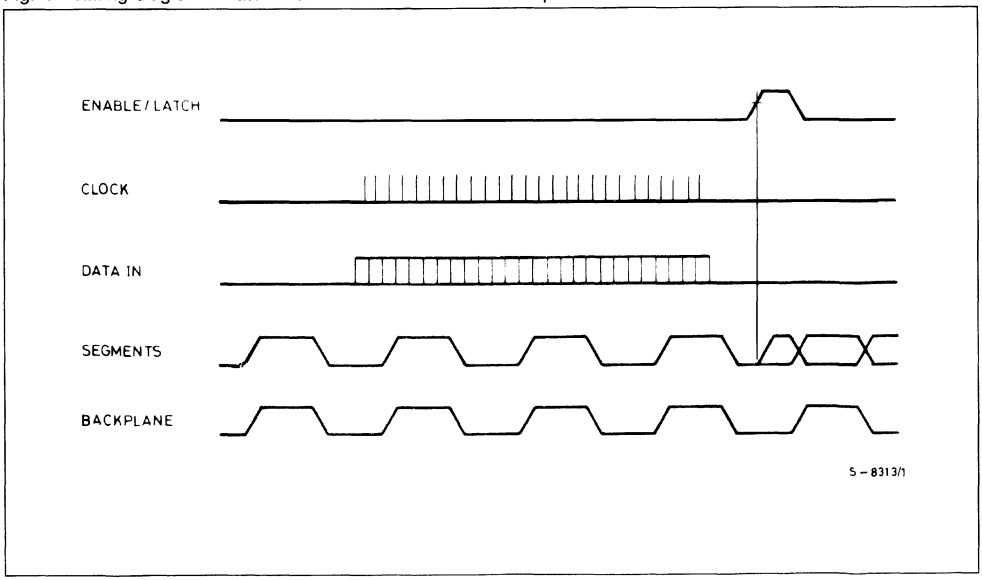


Fig. 5 - Cascade configuration, self oscillating

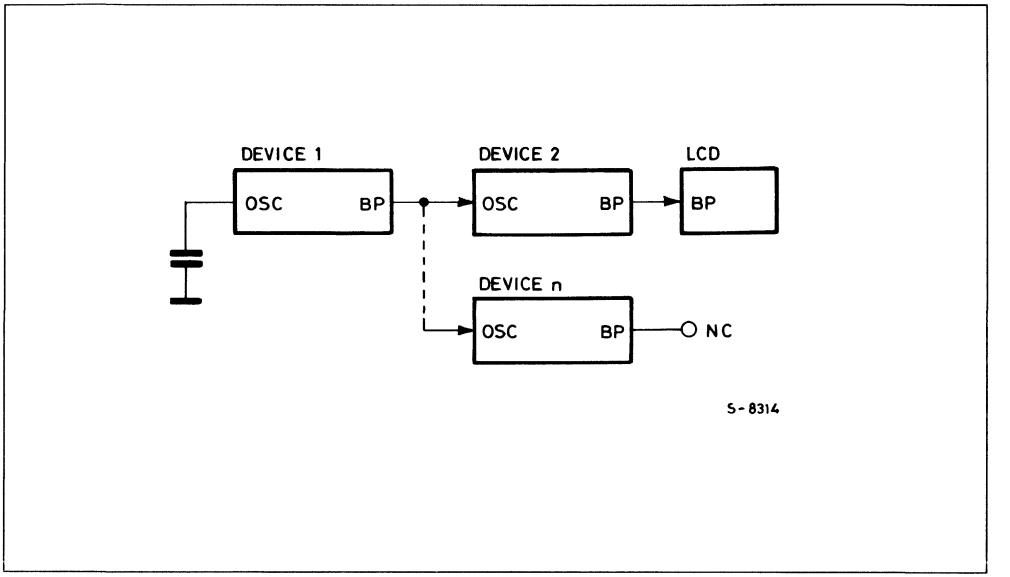
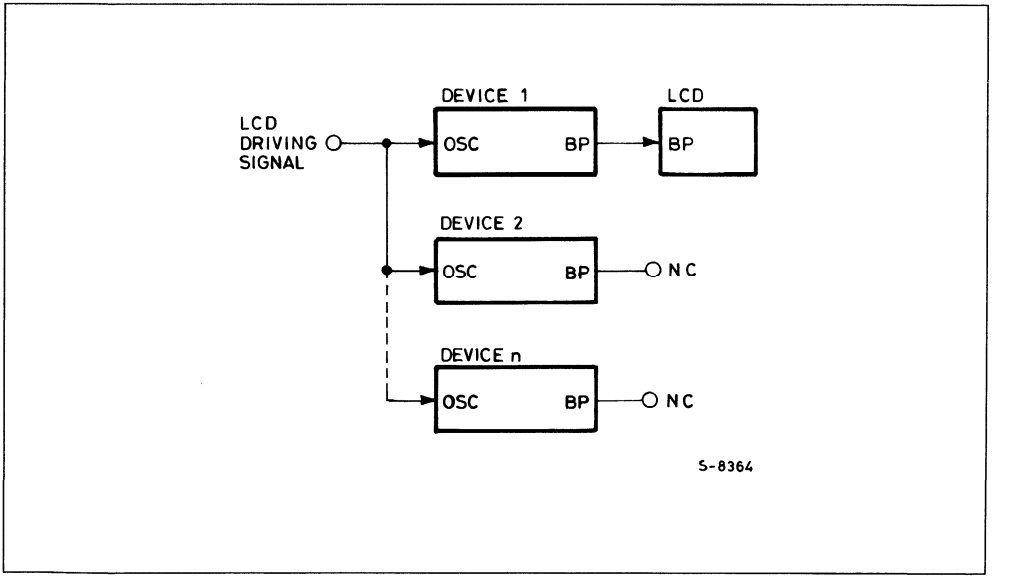


Fig. 6 - Cascade configuration, driven by external signal

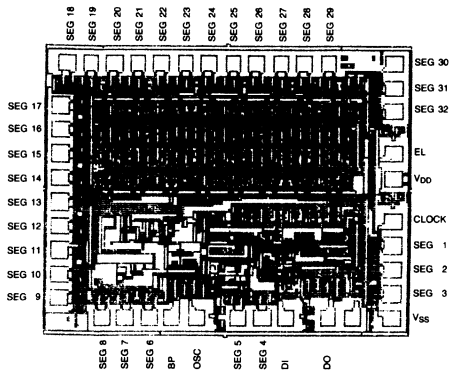


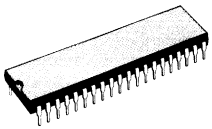
M8439

SERIAL INPUT LCD DRIVER

- **DATA TRANSFER: LATCH MODE**
- DRIVES UP TO 32 LCD SEGMENTS
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- CASCADABLE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- ON CHIP OSCILLATOR
- REQUIRES ONLY 3 CONTROL LINES
- −40 TO 85°C TEMPERATURE RANGE

The M8439 is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8439 can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8439 is available in DIE form and assembled in 40 pin dual-in line plastic.

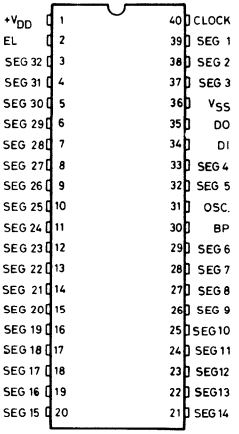




Plastic DIP-40

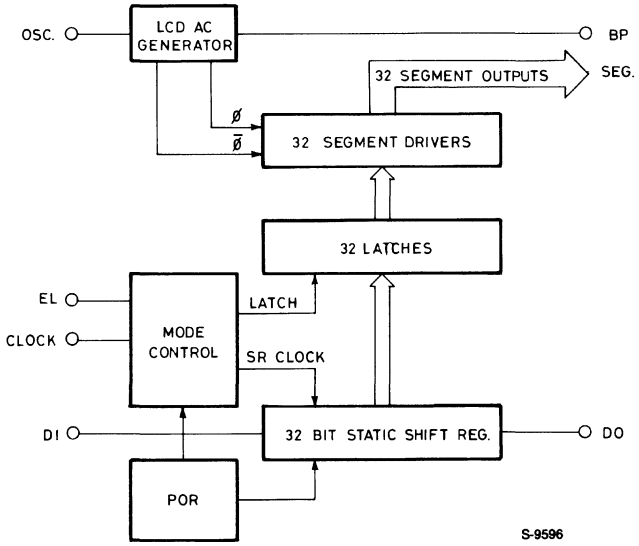
ORDERING NUMBERS: M8439 B6
M8439 DIE1

PIN CONNECTIONS



S-8309

BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	μA
I_Q	Quiescent Current		V_{DD} = 10V		10	μA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level	CLOCK DI EL		0	.2V_{DD}	V
I_{IN}	Input Current	CLOCK DI EL			±5	μA
C_I	Input Capacitance	CLOCK DI EL			5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level	OSC	Driven mode		.1V_{DD}	V
I_{IN}	Input Current	OSC	Driven mode		±10	μA
R_{ON}	Segment Output Impedance		I_{IL} = 10μA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100μA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100μA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

Fig. 2 shows a timing diagram.
Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

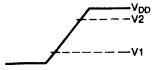
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

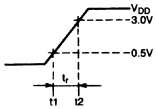
CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s



c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of latch mode: set-up and hold time

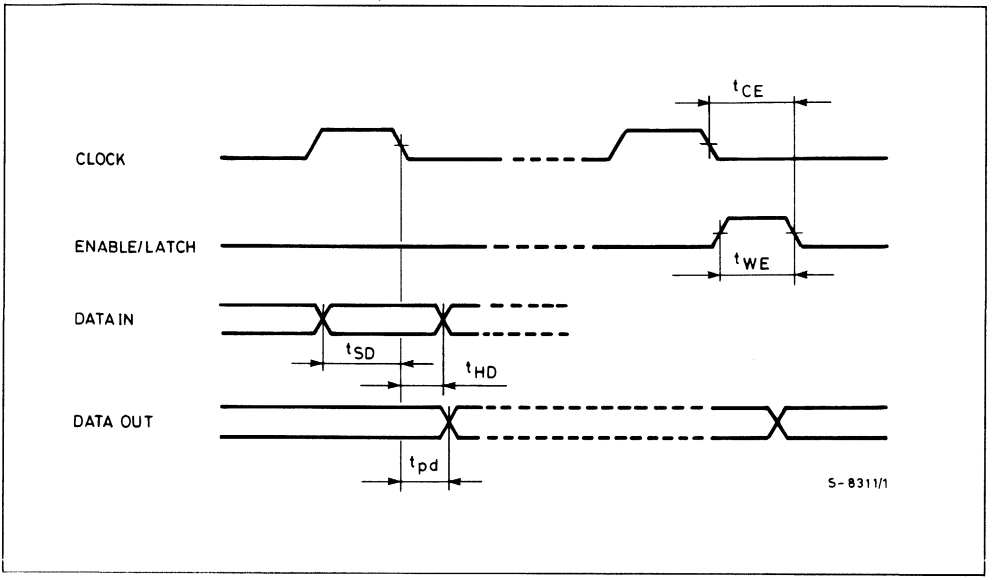


Fig. 2 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

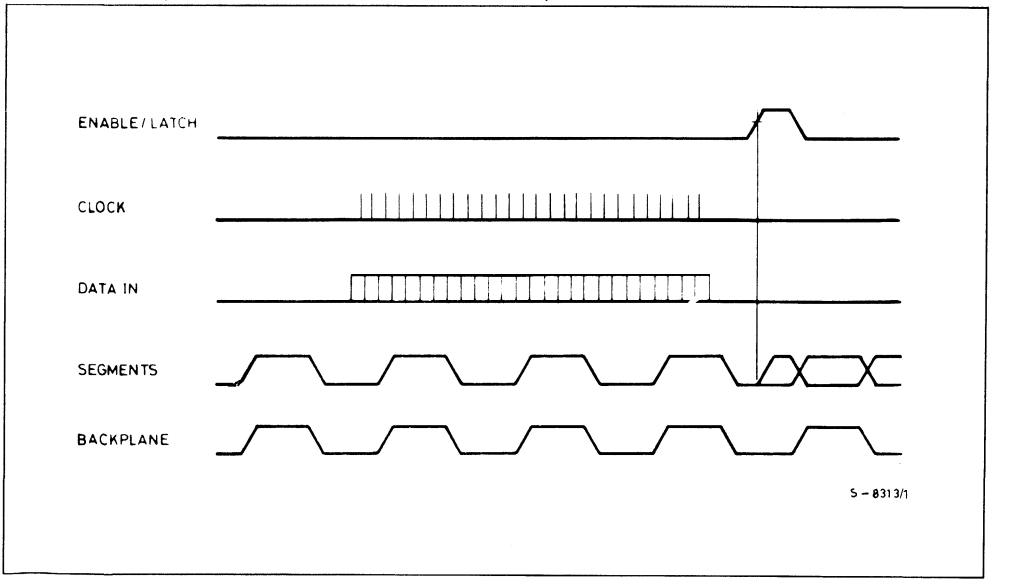


Fig. 3 - Cascade configuration, self oscillating

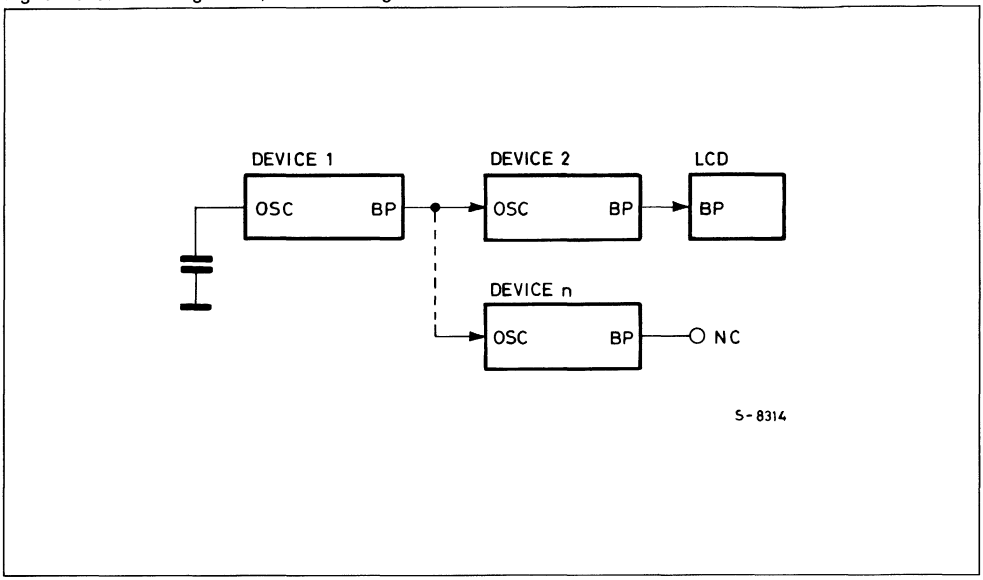
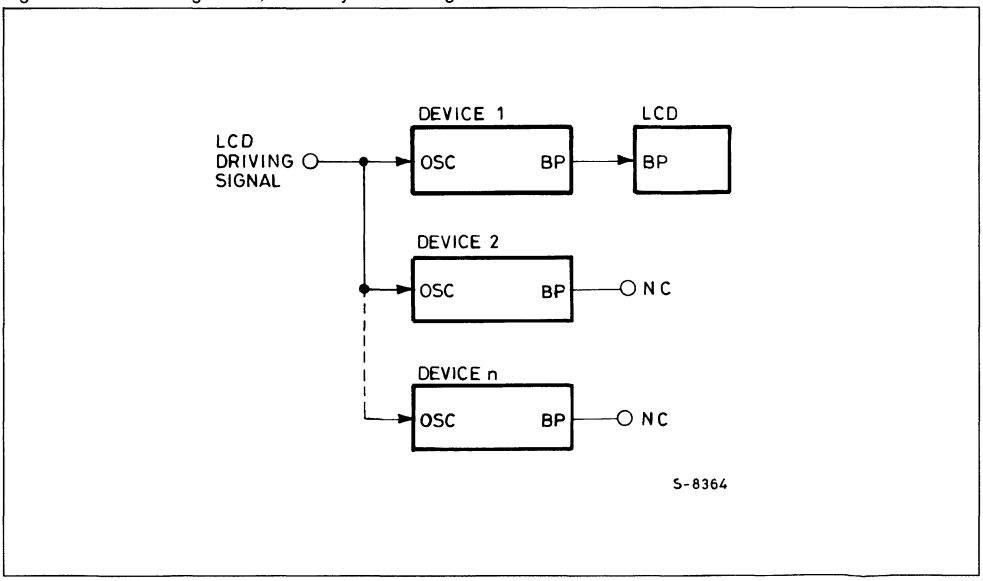


Fig. 4 - Cascade configuration, driven by external signal



M8571

1024 BIT SERIAL S-BUS EEPROM

- 10 YEAR DATA RETENTION
- SINGLE +5V POWER SUPPLY
- AUTOMATIC POWER DOWN
- INTERNAL HIGH VOLTAGE AND SHAPING GENERATOR
- SELF TIMED E/W OPERATION
- AUTOMATIC ERASE-BEFORE WRITE
- 3-WIRES S-BUS (I²C BUS COMPATIBLE)
- 2 CHIP SELECT FOR SIMPLE MEMORY EXTENSION
- SELF INCREMENTING ADDRESS REGISTER
- MULTI-MODE ADDRESSING (WHEN MS = V_{IH} ALLOWING:
  - PARTITIONING OF THE 1024BITS INTO:
    - 128 x 8bit
    - 64 x 16bit
    - 32 x 32bit
  - OPCODE-LIKE ADDRESSES FOR:
    - halting of a modify operation
    - reading of the device "busy" status
    - "block erase" operation
    - reloading of the address register with the pre-increment value

The M8571 is a 1024-bit Electrically Erasable Programmable Read Only Memory (EEPROM). It allows partitioning of the 1024-bit into: 128 x 8-bit (bytes); 64 x 16-bit (words); 32 x 32-bit (pages). The M8571 is manufactured with SGS's reliable floating gate technology. Addresses and data are transferred serially via a three-line bidirectional bus (S-BUS). When the MS pin is at V_{IL} the device works like the PCD 8571 CMOS RAM. The built-in address register is incremented automatically after writing or reading of each address partition.
The M8571 is available in 8-pin dual in-line plastic and ceramic packages.

PIN DESCRIPTION

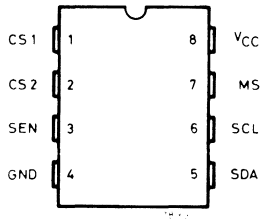
- V_{CC}; GND: Power supplies.
- SCL: Clock line for the S-BUS system.
- SEN: Start/Stop line for the S-BUS system.
- SDA: Data line for the S-BUS system (open drain).
- CS1/CS2: Chip Select inputs. In order to select a device the 2 bits (7th and 6th) in the first byte of the interface protocol, must match the CS values.
- MS: Mode Select input to determine the operating mode of the M8571 (this pin can recognize a non standard level, $V_{IN} \geq 7.5V$, to enable "Block Erase" operations).

Minidip Plastic **B**

Minidip Ceramic **F**

ORDERING NUMBERS: M8571B1
M8571F1

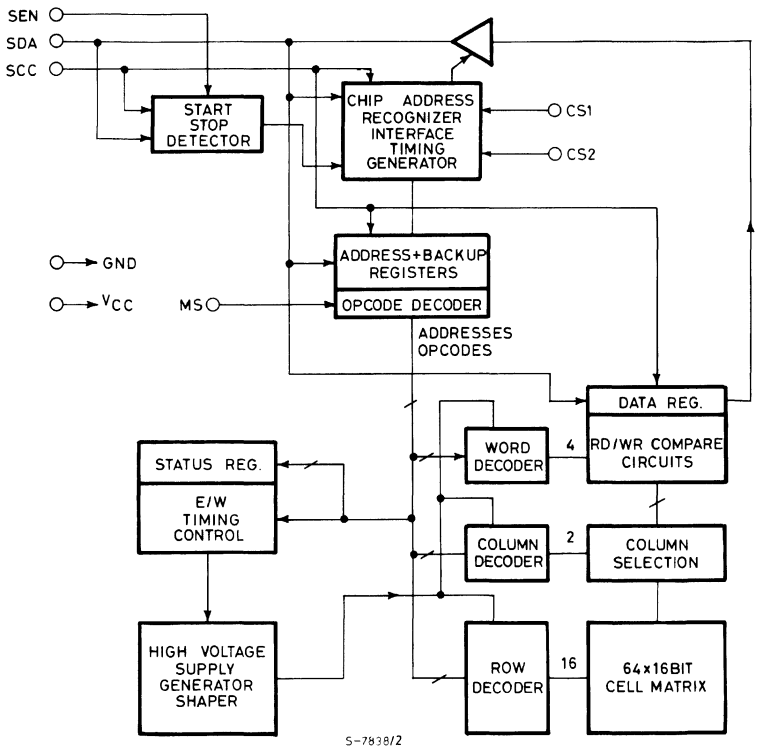
PIN CONNECTIONS



PIN NAMES

CS	CHIP SELECT INPUTS
SEN	START/STOP INPUT
SCL	CLOCK INPUT
SDA	DATA INPUT/OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND
MS	MODE SELECT INPUT

Fig. 1 - Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
T_{amb}	Ambient temperature under bias	−10 to + 80	°C
T_{stg}	Storage temperature range	−65 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

DC AND AC OPERATING CONDITIONS

Operating Temperature Range	0 to 70°C
V_{CC} Power Supply	5V ±5%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{CC1}	V_{CC} Current Standby			2	8	mA
I_{CC2}	V_{CC} Current Active			4	20	mA
V_{IL}	Input Low Voltage		−0.1		1.5	V
V_{IH}	Input High Voltage		3.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Unit
f_{SCL}	Clock frequency		0	125	KHz
t_{SW}	Tolerable spike width on bus			100	ns
t_{DH}	DAT Data hold time		0		μs
t_{SU}	DAT Data set-up time		250		ns
t_r	Signal Rise time			700	ns
t_f	Signal Fall time			300	ns

CAPACITANCE

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF

S-BUS DESCRIPTION

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I²C bus. In fact the S-BUS includes decoding of START/STOP conditions and the arbitration procedure in case of multimaster system configuration. Both different transmission modes are shown in figures 2a and 2b. As it can be seen, the SDA line, in the I²C bus, represents the AND combination of SDA and SEN lines in the S-BUS.
If the SDA and the SEN lines of the S-BUS one short-circuit connected, they appear as the SDA line of I²C bus.
The START/STOP conditions (respectively points 1 and 6) are detected (by the peripherals designed to work with S-BUS) by a transition of the SEN line (1 - - >0/0 - - >1) while the SCL line is at the high level.
The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the START information (point 1) the SEN line returns to the high level and remains unchanged for all the time the transmission is performed.
When the transmission is completed (point 5) the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the STOP information with a low to high transition; while the SCL line is at high level.
On the S-BUS, as on the I²C bus, each byte of eight bits is followed by one acknowledge bit which is a high level put on the SDA line by transmitter.
A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse as shown in Figure 3.

FIG. 2a - S-BUS CONFIGURATION

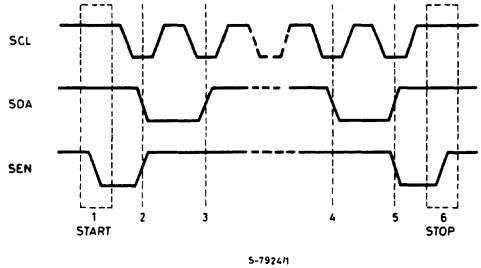


FIG. 2b - I²C BUS CONFIGURATION

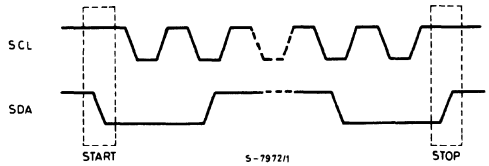
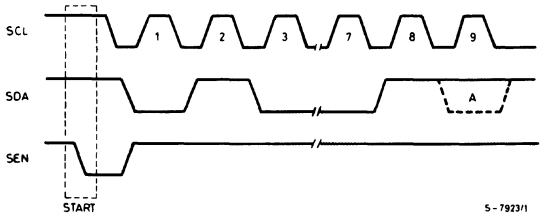


FIG. 3 - ACKNOWLEDGE



An addresses receiver has to generate an aknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time.
In this case the master transmitter can generate the STOP information, via the SEN line, in order to abort the transfer.

Compability S-BUS/I²C bus. Using the S-BUS protocol it's possible to implement "mixed" system including S-BUS/I²C bus peripherals.
In order to have the compability with the I²C bus peripherals, the devices including the S-BUS interface must have their SDA and SEN pins have to be connected together as shown in figure 5 and 5b.
It is also possible to use mixed S-BUS/I²C bus protocols as showed in figure 5c. S-BUS peripherals will only react to S-BUS protocol signals, while I²C bus peripheral will only react to I²C bus signals.

FIG. 4 - SYSTEM WITH S-BUS PERIPHERALS

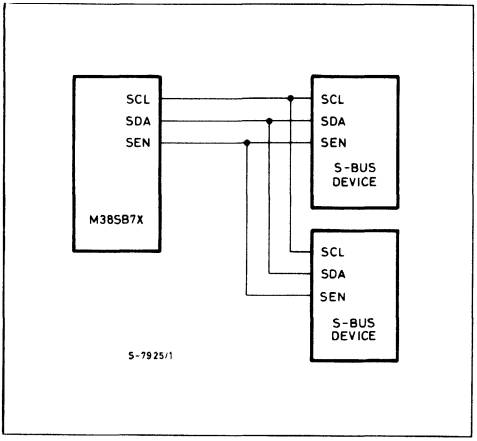
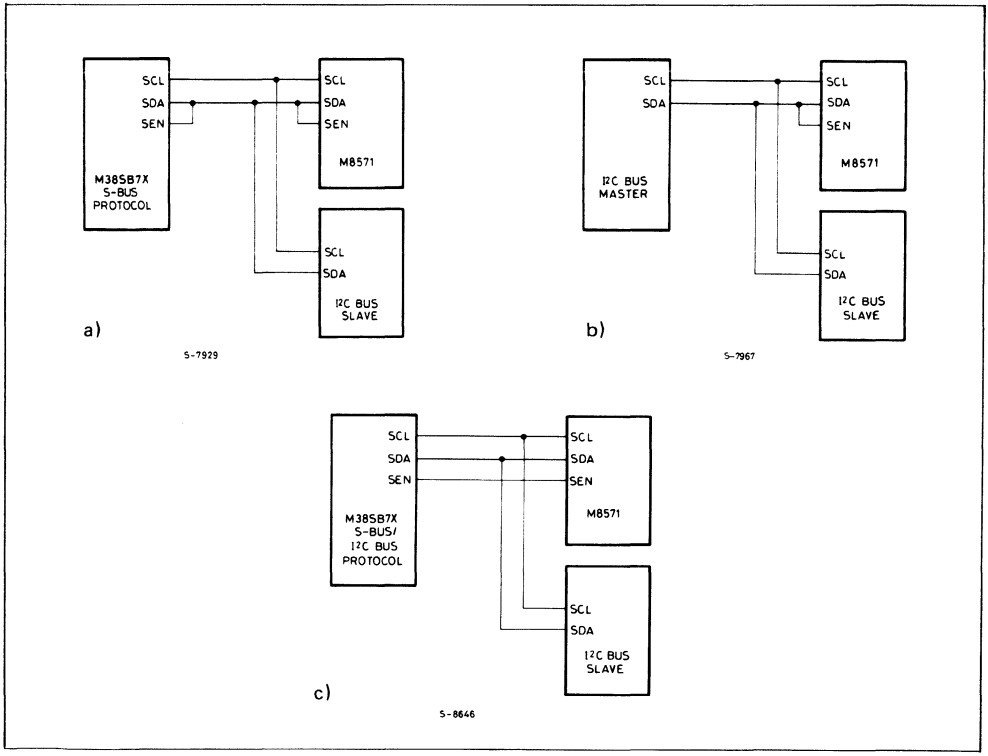


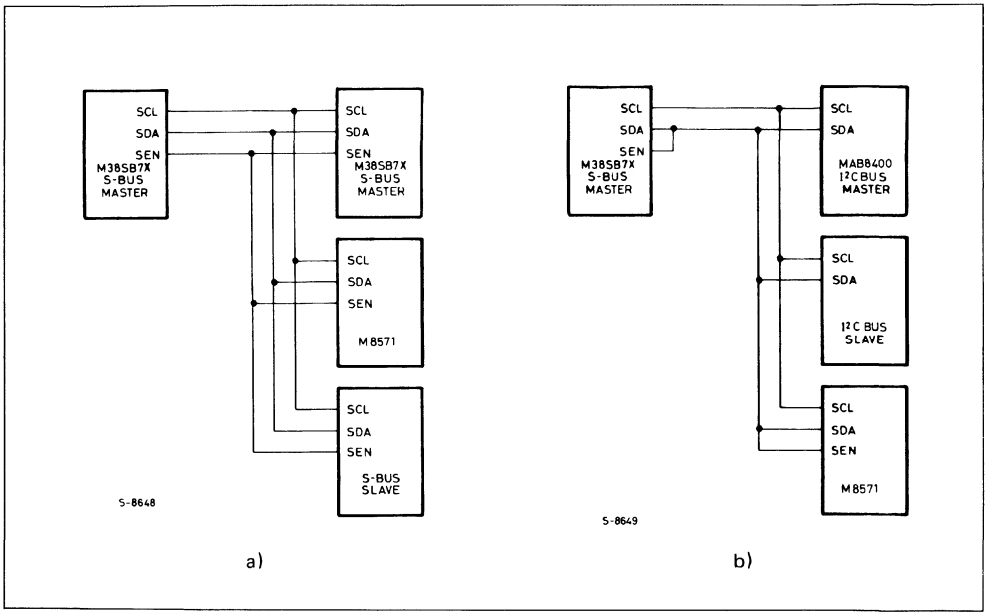
FIG. 5 - SYSTEM WITH "MIXED" S-BUS/I²C BUS PERIPHERAL



S-BUS DESCRIPTION (Continued)

Multimaster System. The S-BUS allows the implementation of the multimaster configuration (two or more master stations and slave peripherals). In such a system if two or more transmitter, through the SEN line (SEN 1 – – >0 while SCL = 1), require the bus at the same time, the arbitration procedure is performed as in the I²C bus.

FIG. 6 - MULTIMASTER SYSTEM



S-BUS INTERFACE

The serial, 3-wire, interface (SDA, SCL and SEN wires are open drain to allow "wired-and" operation) connects several devices which can be divided into "masters" and "slaves". A master is a device that can manage a data transfer; as such, it drives the Start and Stop (SEN), the clock (SCL) and the data (SDA) lines. The bus is "multimaster" in that more master devices can access it; arbitration procedures are provided in the bus management. Obviously, at least one master must be present on the bus. The M8571 is a hardware slave device. It can only answer the requests of the masters on the bus; therefore SDA is an I/O, while SCL and SEN are inputs. The S-BUS allows two operating speed: high (125KHz) and low (2KHz). The M8571 can work at both high and low speed.

START/STOP ACKNOWLEDGE

The timing specs of the S-BUS protocol require that data on the SDA and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of a data transfer.
A "high to low" transition on the SEN line, with SCL "high", is a start (STA).
A "low to high" transition on the SEN line, with SCL "high", is a stop.
Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmitter device place a "1" on the bus, the acknowledging receiver a "0").

INTERFACE PROTOCOL

The following description deals with 8-bits data transfers, so that it fully fits when the memory is "seen" as 128 x 8 array. Although the basic structure of the protocol remains the same the behaviour of the M8571 in 16 or 32 bit data transfers is somewhat different. The differencies are described later on.

The interface protocol comprises:
- A start condition (STA)
- A "chip address" byte, trasmitted by the master, containing two different informations.

  a) the code identifying the device the master wants to address (this information is present in the first seven bits); 4bits indicates the type of the device (i.e. memory, tuning, A/D, etc.; the code for memories is 1010); then there is a bit at low level and 2bits that are the Chip Select configuration that must match the hardware present on the 2 CS pins (this is the case of a device with 2 Chip Select like the M8571, for M8571 CS1 and CS2 must match respectively the 7th and the 6th bit of the byte).

  b) the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence, from now on, is different according to the value of the R/W bit.

1) R/$\overline{W}$ = "0" (WRITE)

   In all the following bytes the master acts as transmitter; the sequence follows with:

   a) a "word address" byte containing the address of the selected memory word and/or opcode (see word address/opcode section).
   b) a "data" byte which will be written at the address given in the previous byte.
   c) further data bytes which, due to the self incrementing address register, will be written in the "next" memory locations. At the end of each byte the M8571 acknowledges.
   d) a stop condition (STO)

After receiving and acknowledging a data byte or a set of data bytes to be written, the M8571 automatically erases the addressed memory locations and rewrites them with the received data. Since the E/W time for an EEPROM is in the order of 10-20 ms, the next operation can take place only after $t_{E/W}$ (what the master can and must do is described in the E/W TIME SPECS section).
An example of a write sequence is given bellow:

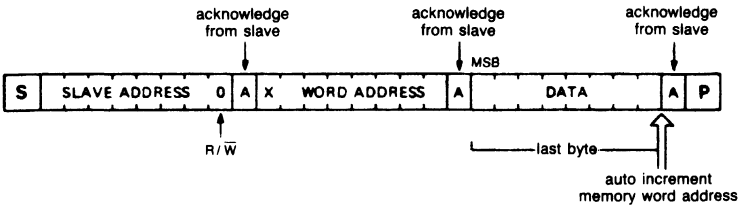
0. STA
1. 10100ss0 A (M8571 acknowledges only if "ss" matches its CS code)
2. xyyyyyyy A
3. zzzzzzzz A (at this moment the M8571 starts writing zzzzzzzz at the address yyyyyyy)

than after $t_{E/W}$:

4. tttttttt A (now the M8571 write data tttttttt at address yyyyyyy + 1)

The write sequence can be composed by an unlimited number of data bytes.

Master transmits to slave receiver (WRITE mode)



2) R/$\overline{W}$ = "1" (READ)

In this case the slave acts as transmitter and, therefore, the transmission changes direction. The second byte of the sequence will be sent by the M8571 and it will contain the data present in the memory present at the address pointed by the "current" value of the address register. Following bytes will be the data present at the "next" addresses. At the end of each byte, the M8571 places a "1" on the bus during acknowledge time and waits for the master to send a "0" (meaning "acknowledge"). When the master want to stop the transfer, it gives a "1" (not "acknowledged"): as a consequence, the M8571 leaves the bus high so that the master can give the stop condition. An example is given below:

0. STA
1. 10100ss1 A
2. xxxxxxxx H (xxxxxxxx is the data present in the currently addressed memory location; H is the high level placed on the bus by M8571)

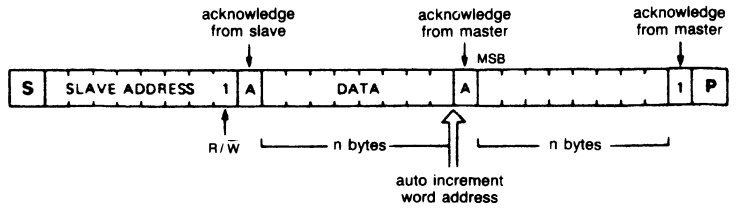
3) MIXED SEQUENCE

When the master wants to read a memory location different from the one currently addressed, a longer sequence is needed, which includes the writing of the address register. The sequence is as follows:

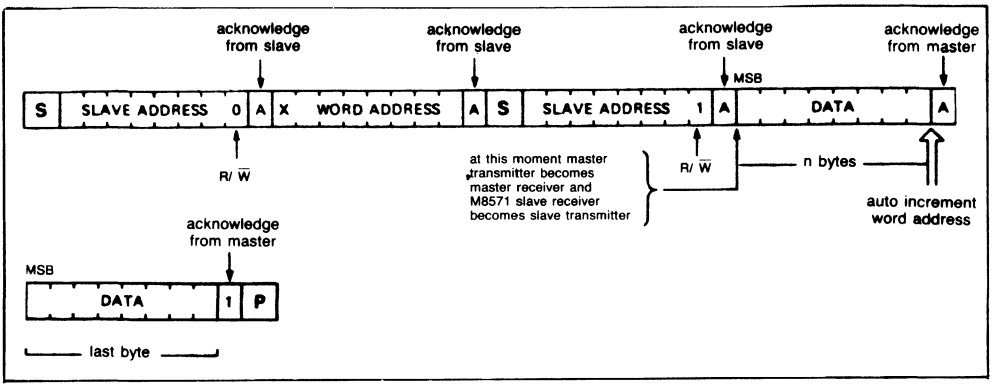
0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. STA
4. 10100ss1 A
5. xxxxxxxx H

Where xxxxxxxx is the data present in the yyyyyyy memory location
As appears from the example, a start condition can be given without a previous stop condition.

Master reads slave immediately after first byte (READ mode)



Master reads after setting word address (WRITE word address; READ data)



4) E/W TIME SPECS

After the beginning of an E/W operation at a certain location the M8571 is "busy" until the operation is finished. To show this busy state, the M8571 refuses acknowledge of the next data bytes until $t_{E/W}$ is over. The master device that wants to use the self-increment feature must therefore keep sending the next data byte and monitoring the acknowledge bit until it becomes active.

The communication sequence on the bus becomes, therefore.

0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. zzzzzzzz A
4a. tttttttt H (not acknowledged when $t<t_{E/W}$)
4b. tttttttt A (acknowledged after $t_{E/W}$)

Now the M8571 will write data tttttttt at address yyyyyyy+1
This usage mode keeps the bus unavailable for other tasks during the $t_{E/W}$ time. It is possible to free the bus by giving a stop condition (this condition stops only the bus sequence, not the E/W operation). After a stop condition the access sequence must be started again from the beginning (start).
The E/W circuitry in the M8571 performs automatically the "Erase before Write" sequence required by the technology. Furthermore, both erase and write last all (and only) the time needed for the required modification to happen (this is accomplished by an intelligent "compare and retry" circuitry). This optimizes E/W time but may have the drawback of "locking" the circuitry in case a memory location "breaks down" and can not be modified (in which case $t_{E/W}$ becomes infinite).
To overcome this drawback, it has been made possible to force the circuit out of the E/W status, that is to halt a modify operation. Two different modes are provided, depending on the value of the MS control pin:

$$MS \leqslant V_{IL}$$

The E/W operation is unconditionally stopped by a following valid chip address byte.

$$MS \geqslant V_{IH}$$

An opcode is provided to halt the operation (see "EEPROM mode" section).

5) WORD ADDRESS/OPCODE

The second byte transmitted in a write sequence can assume several meaning according to the value of the MS pin. In any case, it carries all the informations the M8571 needs to perform the desired operation.
MS can assume three different values:

- V_{IL} ($V_{IN} \leq 1.5V$)
- V_{IH} ($3.0V \leq V_{IN} < V_{CC}+1$)
- V_H ($9.0V \leq V_{IN} \leq 12V$)

With regards to the value of MS, the possible behaviours are:

a) MS = V_{IL} ("RAM mode")
In this mode the M8571 is compatible with the PCD 8571 RAM (128 x 8bit). The second byte of the sequence gives the address of the word to be selected, both for write and for read:
1. xyyyyyyy A
yyyyyyy is the word address; the first bit is "don't care; the main feature of this mode are the following:
. the memory appears as an 128 x 8 array
. only "byte operations are allowed;
. E/W operations are stopped by the following accesses.

b) MS = V_{IH} (EEPROM mode)

The word address-byte now must be regarded as mixed address-opcode byte; more precisely, the first three bits indicate the meaning to be attributed to the remainder of the byte. The possible combinations are:

0yyyyyyy	byte-mode (8 bits) RD or E/W at address yyyyyyy
10yyyyyy	word-mode (16 bits) RD or E/W at address yyyyyy
110yyyyy	page-mode (32 bits) RD or E/W at address yyyyy
11111111	E/W cycle stop
11100000	Read busy bit
11100100	Block Erase (see also BLOCK mode)
11110001	Reload Address Register with pre-increment data

In this mode, as well as in RAM mode, the "busy" information is transmitted from the M8571 to the master using the "no acknowledge" format. Furthermore, "Read busy bit" instruction, which is always answered by the M8571 no matter what it is doing, allows the master to know wheter the "no acknowledge" condition comes from a "busy" status or from a malfunction; the "busy" status is signalled by the byte 11100101; the "no busy" by 00011010.
Also in this mode the self-incrementing address register is available, both for read and for write, for each word length.
The M8571 is provided with a double register for storing the address that is sent during the second byte of a write sequence.
When athe self-incrementing is used, this address becomes the "starting address" of the modified string of bytes. The "reload" instruction allows the master to recover this address if it wants to read the modified string from the beginning, without the need for external storage of the "starting address".

c) MS = V_H (BLOCK mode)

The only instruction that can be executed in this mode is "Block Erase", which is useful to erase the whole array in a single shot. This can occur either during testing or at the set-up of a new system, when all the memory must be written anew. When this instruction is given, the self-timing circuitry is disabled, so that an E/W cycle stop instruction must be given after the proper E/W time, to stop the operation. The "enable" feature obtained with the non standard level on MS was added to avoid unintentional clearing of the whole memory, whenever the "Block Erase" code was erroneously sent.

6) 16-bit or 32-bit OPERATIONS

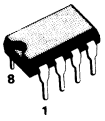
The obvious advantage of an operation on 16 bits (a word) or on 32 bits (a page) is that the E/W time is 10 to 20 ms for the whole word or page. When a word or page mode operation is required, the device behaviour undergoes some slight modifications:
- The M8571 waits for receiving all the bytes that compose the word or the page before starting an E/W operation;
- The self-incrementing address register keeps into account the word or page lenght so that, at the end of a word or page mode operation, it points to the next word or page.

M8716A

CLOCK/CALENDAR WITH SERIAL I²C BUS

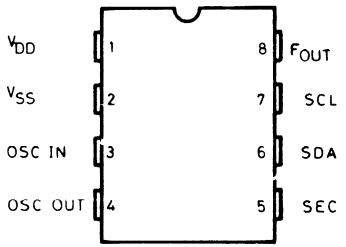
- 32kHZ QUARTZ TIMEBASE
- COUNTERS FOR SEC; MIN; HRS; DAY; MONTH OR SEC; MIN; HRS; DAY OF WEEK
- EXTREMELY LOW POWER CONSUMPTION IN STANDBY OPERATION (TYP. 5μA)
- 8 PIN DIP PACKAGE
- INTEGRATED POWER FAIL DETECTION AND POWER-ON RESET
- PULSE OUTPUT FOR SECONDS
- CMOS PROCESS

The integrated circuit M8716A contains a digital clock with a 32kHz quartz oscillator and a serial bus interface (I²C BUS). The circuit is programmable to count seconds, minutes, hours, days and month or seconds, minutes, hours and day of the week.
This circuit is intended for use within a microcomputer system.
The M8716A is available in a 8 lead dual in-line plastic package.



B1
Minidip Plastic
ORDERING NUMBER: M8716A B1

PIN CONNECTIONS



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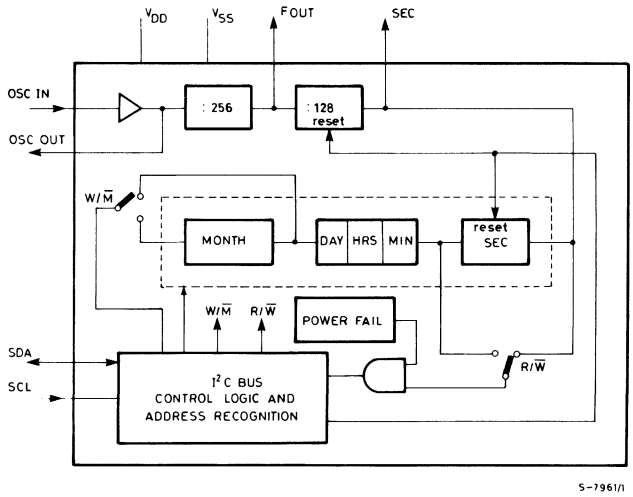
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}-V_{SS}	Supply voltage	−0.3 to +10	V
V_I/V_O	Input voltage, output voltage	V_{SS} −0.3 to V_{DD} +0.3	V
P_D	Total package power dissipation	300	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	0 to +70	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C: V_{DD} = 5V; F_{OSC} = 32.768kHz if not otherwise specified).

Symbol	Parameter	Test Condition	Values			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current				1	mA
V_{BAT}	Supply voltage (standby operation)	No Data Transfer	2.0	2.4		V
I_{BAT}	Supply current (standby operation)	Test circuit V_{BAT} = 2.4V		5	15	µA
I_{IN}	Input current SDA; SCL	$V_{IN} = V_{DD}$			5	µA
		$V_{IN} = V_{SS}$			−5	
I_{OUT}	Output current SDA	V_{OL} = 0.4V	4			mA
I_{OUT}	Output current F_{OUT}, SEC	V_{OUT} = 1V	0.1			mA
		V_{OUT} = 4V	−0.1			
C_{OUT}	Oscillator output-capacitance		16	20	24	pF

GENERAL DESCRIPTION

The integrated circuit M8716A contains a digital clock counting seconds, minutes, hours, days and months or seconds, minutes, hours and days of the week as an option. A 32.768kHz quartz oscillator serves as time-base. This circuit is intended for use within a microcomputer system.
Writing (time setting) and reading of the counters is done via a serial interface (I²C BUS). The microcomputer is used for controlling the data transfer and for generating the signals to drive a (7 segment) display. If a data transfer takes place between the M8716A and the microprocessor, a 5V supply voltage has to be provided. During standby the circuit is supplied by two NiCd-cells at a very low power consumption.

FUNCTIONAL DESCRIPTION

DIVIDERS AND COUNTERS

The oscillator frequency of 32.768kHz is first divided by 256 and then again by 128. The resulting output frequency of 1Hz then serves as clock pulse for the time counters.
The content of the counters for sec, min, hr, day and month of sec, min, hr, and day of week can be read or modified (written) via the I²C BUS interface. During a "write" cycle only the content of the counters starting from the minutes counter is modified: the seconds counter and the seconds divider block are reset to zero.
Selection between "calendar" operation (display of day and month) and "day of week" operation (display of day of week 1 to 7) is done as follows:
If the second bit in the first data byte is "1" during a "write" operation, the counters are set for the mode "day of week".
If this bit remains at "0" during a "write" operation the calendar mode is selected. In this case, carry of the "day" counter is performed automatically at positions 28, 30 or 31, depending on the month. In case of a leap year the day 29 (of February) can be set by a "write" operation.
In this case, carry takes place on 3-1 (March 1st).

I²C BUS INTERFACE GENERAL DESCRIPTION

Data transfer from the circuit M8716A to the microcomputer (reading) and vice versa (writing) takes place via the two lines SDA and SCL. Address and data are transmitted on SDA while at the same time clock pulses have to be provided on SCL for synchronization by the microcomputer.

I²C BUS INTERFACE ADDRESSING (see Fig. 1...3)

A data transfer (reading or writing) is initiated by a start condition ("1" -> "0" transition on SDA while SCL remains at "1") and a subsequent address byte. By assigning a unique address to each circuit, several circuits may be connected to the I²C BUS without interfering each other.
If the M8716A recognizes an address transmitted on the bus as its own address, the data transfer starts. The least significant bit of the address word controls the direction of data transfer (R/$\overline{W}$-control). If it is set to "0", data is transferred from the microcomputer to the circuit, i.e. the content of the time counters is modified. If it is set to "1" the time information is read out by the microcomputer. The clock frequency (SCL) may be from DC up to 100kHz. If a carry of the time counter should take place during a data transfer, the carry will be stored and made after the data transfer. As only one carry can be stored, the whole data transfer must not take a time longer than one second.

SYNCHRONIZATION

For easy of synchronization with an external time reference in case of small deviations (< +/− 30sec), only the address (with R/$\overline{W}$ = "0") has to be transmitted, followed immediately by a stop condition. No data is transmitted (see Fig. 4). The second divider block (128Hz to 1Hz) and the seconds counter are reset. If the seconds counter was at position 30 ... 59, a carry to the minutes counter takes place in addition to the reset.

POWER FAIL

In case of total power fail an internal register is set to "0". This register disables the data of the watch. So in a read cycle the µP recognizes "0" of the watch content. This is a unique situation appearing only in case of a power fail. The power fail register is automatically reset by the first "write" command.

PULSE OUTPUTS F_{OUT}, SEC

The output frequency of the first divider block (128Hz) is provided on the pin F_{OUT} and facilitates adjustment of the oscillator frequency without loading (and detuning) the oscillator.
The output SEC (1Hz) may be utilized for a blinking second indication.
Both pins F_{OUT} and SEC can also be used as input during the functional test. A Low impedance (50 to 100Ω) external signal source which overrides the internal output buffer can drive the circuit at a frequency higher than the normal rate. This allows to reduce test time.

Fig. 1 - Complete timing for an address/-read; resp. address/-write cycle

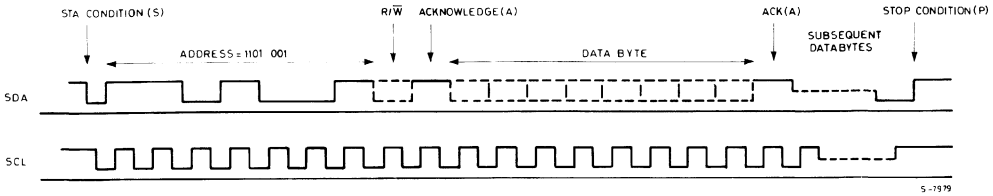


Fig. 2a - Data format for one cycle address/-read (with calendar)

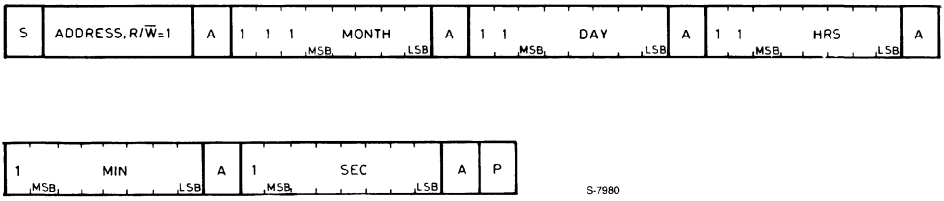


Fig. 2b - Data format for one cycle address/-write (with calendar)

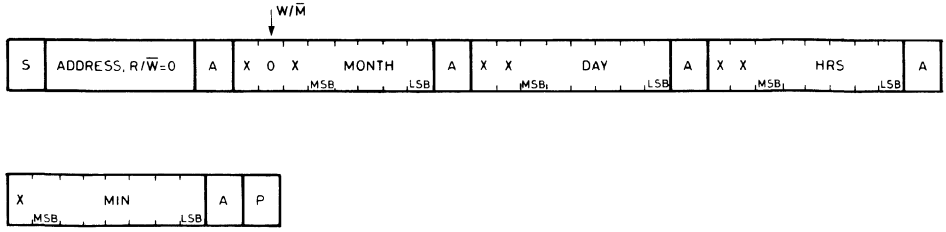


Fig. 3a - Data format for one cycle address/-read (with day of week indication)

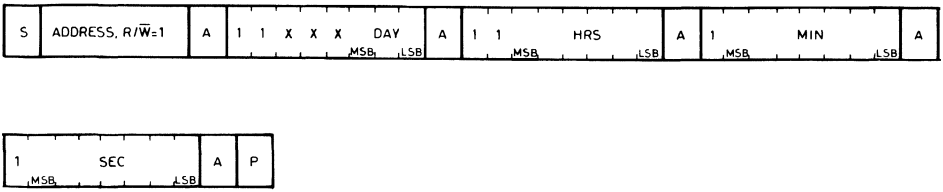


Fig. 3b - Data format for one cycle address/-write (with day of week indication)

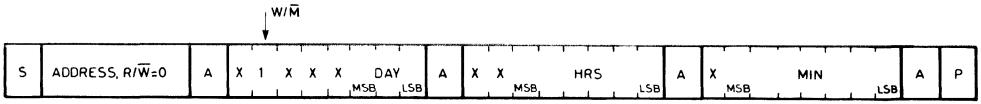
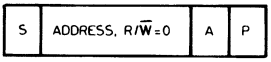


Fig. 4 - Data format for synchronisation (deviation <30sec)



S-7980

Fig. 5 - Test circuit

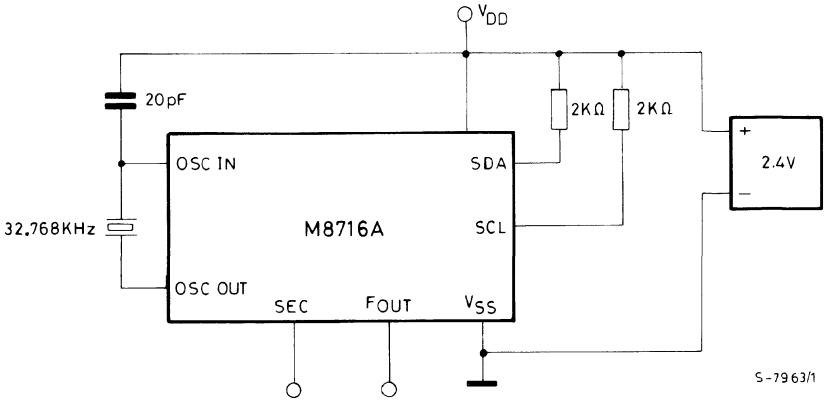
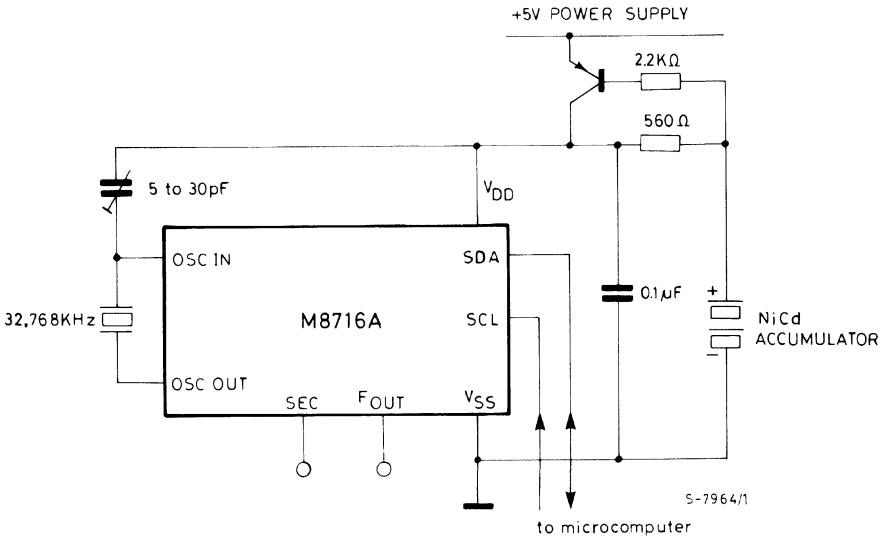


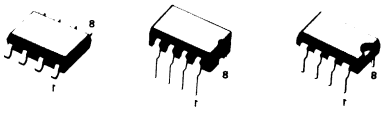
Fig. 6 - Typical application



M9306

256 BIT (16 x 16) SERIAL EEPROM

- SINGLE SUPPLY READ/WRITE/ERASE OPERATIONS (5V ± 10%)
- TTL COMPATIBLE
- 16 x 16 READ/WRITE MEMORY
- LOW STANDBY CURRENT
- NON-VOLATILE ERASE AND WRITE
- RELIABLE FLOTOX PROCESS
- EXTENDED TEMPERATURE RANGE



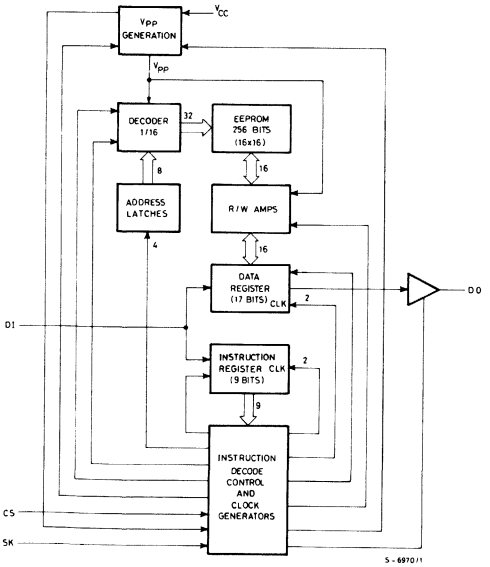
B	F	M
SO-8	Minidip Ceramic	Minidip Plastic

ORDERING NUMBERS: M9306B1
M9306B6
M9306F1
M9306F6
M9306M1
M9306M6

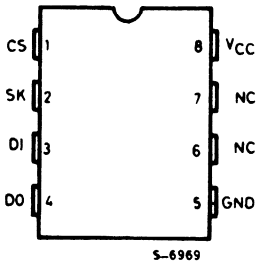
DESCRIPTION

The M9306 is a 256 bit non-volatile sequential access memory manufactured using SGS FLOATING GATE process. It is a peripheral memory designed for data storage and/or timing and is accessed via a simple serial interface. The device contains 256 bits organized as 16 x 16. The M9306 has been designed to meet application requiring up to 10000 E/W cycles per word. Written information has at least 10 years data retention. A power down mode allows consumption to be decreased.

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND

FUNCTIONAL DESCRIPTION

The input and output pins are controlled by separate serial formats. Seven 9-bit instruction can be executed. The instruction format as a logical "1" has a start bit, four bits as an op code, and four bits of address. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). The serial output (DO) pin is valid only during the read mode. During all other modes the DO pin is in high impedance state, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial out shift register. A dummy bit (logical "0") preceds the 16 bit data output string. The output data changes during the high state of the system clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction in executed. The programming disable instruction is provided to protect against accidental data disturbance.
Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most EEPROMs, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low power standby state may be achieved by dropping CS low.

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on chip high voltage section only generates high voltage during this programming mode, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycles ends. All programming mode should be ended with CS high for one SK period, or followed by another instruction.

CHIP WRITE

Entire chip can be written for ease of testing. Writing the chip means that all registers in the memory array have each bytes set as the byte sent with the instruction.

CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

INSTRUCTION SET

Instruction	SB	Op Code	Address	Data	Comments
READ	1	1000	A3A2A1A0		Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	0 0 0 0		Erase/write enable
EWDS	1	0000	0 0 0 0		Erase/write disable
ERAL	1	0010	0 0 0 0		Erase all registers
WRAL	1	0001	0 0 0 0	D15-D0	Write all registers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	Voltage Relative to GND	+6V to −0.3	V
T_{amb}	Ambient Operating Temperature: standard	0 to +70	°C
	extended	−40 to +85	°C
T_{stg}	Ambient Storage Temperature	−65 to +125	°C

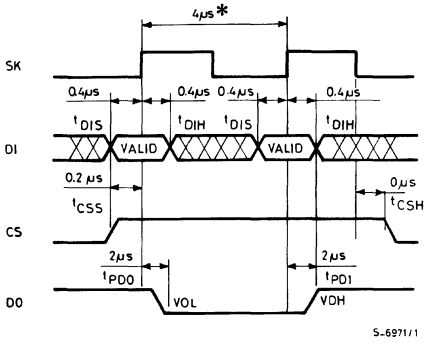
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (0°C to +70°C, for standard Temperature/ −40°C to +85°C for extended Temperature, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

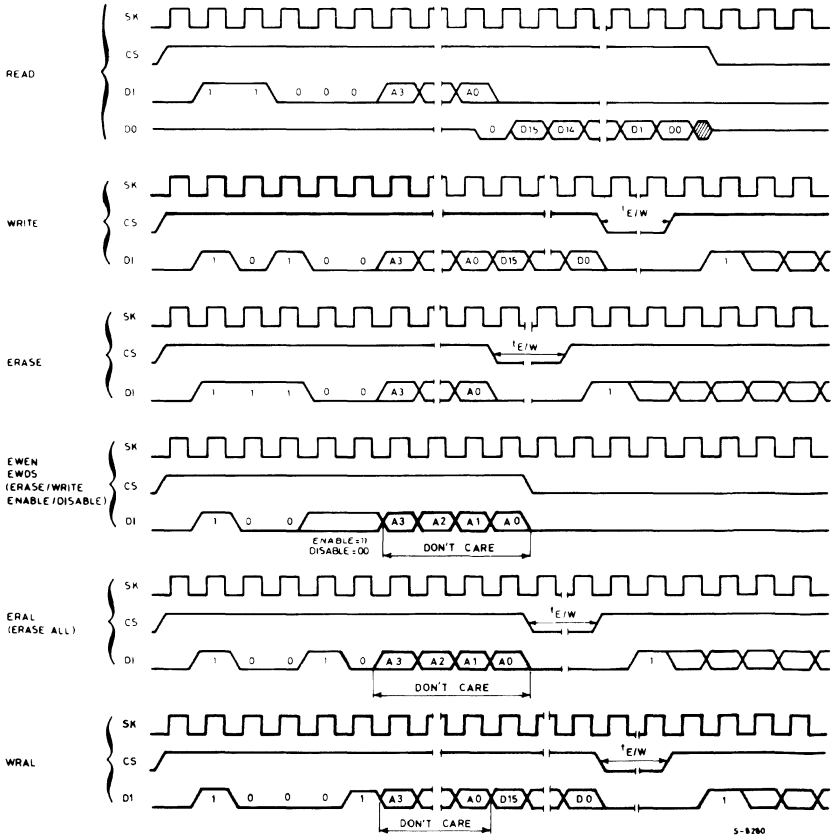
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1		1.5	5	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		1.2	3	mA
I_{CC3}	E/W Operating Current	$V_{CC} = 5.5V$		2.5	6	mA
V_{IL} V_{IH}	Input Voltage Levels		−0.1 2.0		0.8 $V_{CC}+1$	V
V_{OL} V_{OH}	Output Voltage Levels	$I_{OL} = 2.1$ mA $I_{OH} = -400\ \mu A$	 2.4		0.4	V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	μA
	SK Frequency				250*	kHz
	SK Duty Cycle		25		75	%
	Input Set-Up and Hold Times:					
t_{CSS}	CS		0.2			μs
t_{CSH}			0			
t_{DIS}	DI		0.2			
t_{DIH}			0.2			
t_{PD1}	Output Delay	CL = 100 pF			0.5	μs
t_{PD0}	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$			0.5	
$t_{E/W}$	Erase/Write Pulse Width		5		30	ms

* The maximum SK Frequency is 500 KHz when SK Duty Cycle is as 50%

TIMING DIAGRAMS



* THIS IS THE MAXIMUM SK FREQUENCY



M145026
M145027
M145028

ADVANCE DATA

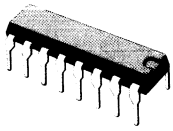
REMOTE CONTROL ENCODER/DECODER CIRCUITS

- M145026 ENCODER
- M145027/M145028 DECODERS
- MAY BE ADDRESSED IN EITHER BINARY OR TRINARY
- TRINARY ADDRESSING MAXIMIZES NUMBER OF CODES
- INTERFACES WITH RF, ULTRASONIC, OR INFRARED TRANSMISSION MEDIAS
- DOUBLE TRANSMISSIONS FOR ERROR CHECKING
- 4.5V TO 18V OPERATION
- ON-CHIP R/C OSCILLATOR, NO CRYSTAL REQUIRED
- HIGH EXTERNAL COMPONENT TOLERANCE, CAN USE 5% COMPONENTS
- STANDARD CMOS B-SERIES INPUT AND OUTPUT CHARACTERISTICS
- APPLICATIONS INCLUDE GARAGE DOOR OPENERS, REMOTE CONTROLLED TOYS, SECURITY MONITORING, ANTITHEFT SYSTEMS, LOW END DATA TRANSMISSIONS, WIRE LESS TELEPHONES

The M145026 encodes nine bits of information and serially transmits this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0, 1, open) to allow 3^9 (19,683) different codes.

Two decoders are presently available. Both use the same transmitter - the M145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The M145028 treats all nine bits as address. If no errors are received, the M145027 outputs the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output goes high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

All the devices are available in 16 lead plastic package.

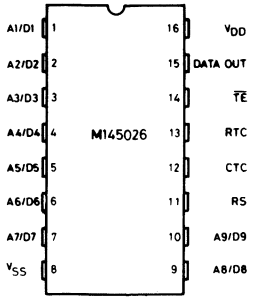


DIP-16 Plastic
(0.25)

ORDER CODE: M145026 B1
M145027 B1
M145028 B1

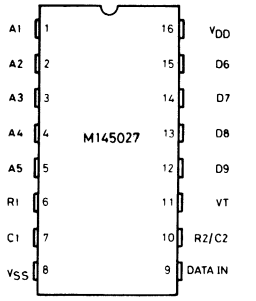
CONNECTION DIAGRAMS

Encoder



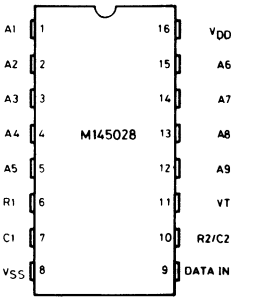
5-6172

Decoder



5-6173

Decoder



5-6174

ABSOLUTE MAXIMUM RATINGS

V_{DD}	DC Supply Voltage	-0.5 to +18	V
V_I	Input Voltage, All Inputs	-0.5 to V_{DD} +0.5	V
I_I	DC Current Drain Per Pin	10	mA
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_{op}	Operating Temperature Range	-40 to +85	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_{amb} = 25°C)

	Parameter	V_{DD}	Min	Typ	Max	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time	5 10 15	– – –	100 50 40	200 100 80	ns
t_{TLH} t_{THL}	Data In Rise and Fall Time (M145027, M145028)	5 10 15	– – –	– – –	15 15 15	µs
f_{CL}	Encoder Clock Frequency	5 10 15	0 0 0	– – –	2 5 5	MHz
f_{CL}	Maximum Decoder Frequency (Referenced to Encoder Clock) (See Figure 9)	5 10 15	– – –	– – –	240 410 450	kHz
t_{WL}	$\overline{TE}$ Pulse Width	5 10 15	65 30 20	– – –	– – –	ns
	System Propagation Delay ($\overline{TE}$ to Valid Transmission)	–	–	182	–	Clock Cycles
	Tolerance on Timing Components (ΔRTC + ΔCTC + ΔR1 + ΔC1) (ΔR2 + ΔC2)	– –	– –	– –	±25 ±25	%

ELECTRICAL CHARACTERISTICS

Parameter			V_{DD}	-40°C		25°C			+85°C		Unit
			V	Min	Max	Min	Typ	Max	Min	Max	
V_{OL}	Output Voltage V_I = V_{DD} or 0	"0" Level	5 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
V_{OH}	V_I = 0 or V_{DD}	"1" Level	5 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5 10 15	– – –	4.95 9.95 14.95	– – –	V
V_{IL}	Input Voltage (V_O = 4.5 or 0.5V) (V_O = 0.9 or 1V) (V_O = 13.5 or 1.5V)	"0" Level	5 10 15	– – –	1.5 3 4	– – –	2.25 4.50 6.25	1.5 3 4	– – –	1.5 3 4	V
V_{IH}	(V_O = 0.5 or 4.5V) (V_O = 1.0 or 9V) (V_O = 1.5 or 13.5V)	"1" Level	5 10 15	3.5 7 11	– – –	3.5 7 11	2.75 5.50 8.25	– – –	3.5 7 11	– – –	V
I_{OH}	Output Drive Current (V_{OH} = 2.5V) (V_{OH} = 4.6V) (V_{OH} = 9.5V) (V_{OH} = 13.5V)	Source	5 5 10 15	-2.5 -0.52 -1.3 -3.6	– – – –	-2.1 -0.44 -1.1 -3	-4.2 -0.88 -2.25 -8.8	– – – –	-1.7 -0.36 -0.9 -2.4	– – – –	mA
I_{OL}	(V_{OL} = 0.4V) (V_{OL} = 0.5V) (V_{OL} = 1.5V)	Sink	5 10 15	0.52 1.3 3.6	– – –	0.44 1.1 3	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mA
I_I	Input Current $\overline{TE}$ (M145026, Pullup Device)		5 10 15	– – –	– – –	3 16 35	4 20 45	7 26 55	– – –	– – –	µA
I_I	Input Current RS (M145026) Data In (M145027, M145028)		15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
I_I	Input Current A1/D1-A9/D9 (M145026) A1-A5 (M145027) A1-A9 (M145028)		5 10 15	– – –	– – –	– – –	±55 ±300 ±650	±80 ±340 ±725	– – –	– – –	µA
C_I	Input Capacitance (V_I = 0)		–	–	–	–	5	7.5	–	–	pF
I_{DD}	Quiescent Current - M145026		5 10 15	– – –	– – –	– – –	0.0050 0.0100 0.0150	0.10 0.20 0.30	– – –	– – –	µA
I_{DD}	Quiescent Current M145027, M145028		5 10 15	– – –	– – –	– – –	30 60 90	50 100 150	– – –	– – –	µA
I_T	Total Supply Current M145026 (f_{CL} = 20 kHz)		5 10 15	– – –	– – –	– – –	100 200 300	200 400 600	– – –	– – –	µA
I_T	Total Supply Current M145027, M145028 (f_{CL} = 20 kHz)		5 10 15	– – –	– – –	– – –	200 400 600	400 800 1200	– – –	– – –	µA

OPERATING CHARACTERISTICS

M145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0, 1, open) allowing $3^9 = 19683$ possible codes. The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).
Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.
The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

M145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. If this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.
Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

M145028

This receiver operates in the same manner as the M145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.
Although address information normally is encoded in trinary, the designer should be aware that, for the M145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only $2 \times 3^8 = 13{,}122$ different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the transmitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words for error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figure 7 and 8.

Fig. 1 - Encoder block diagram M145026

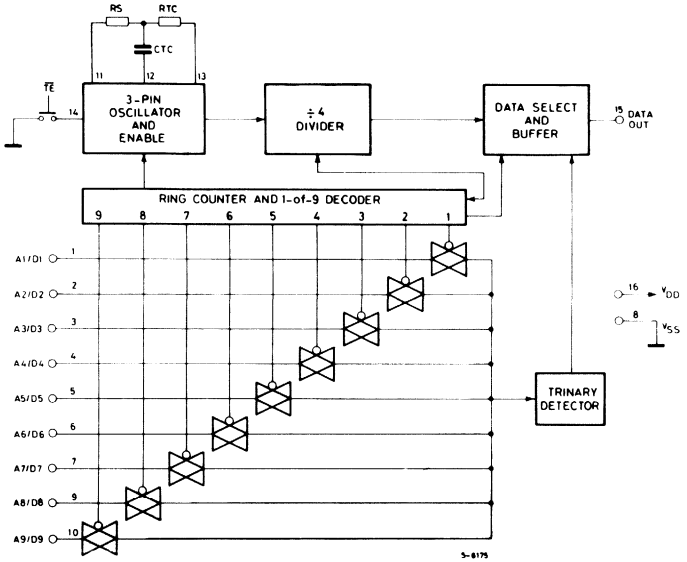


Fig. 2 - Decoder block diagram M145027

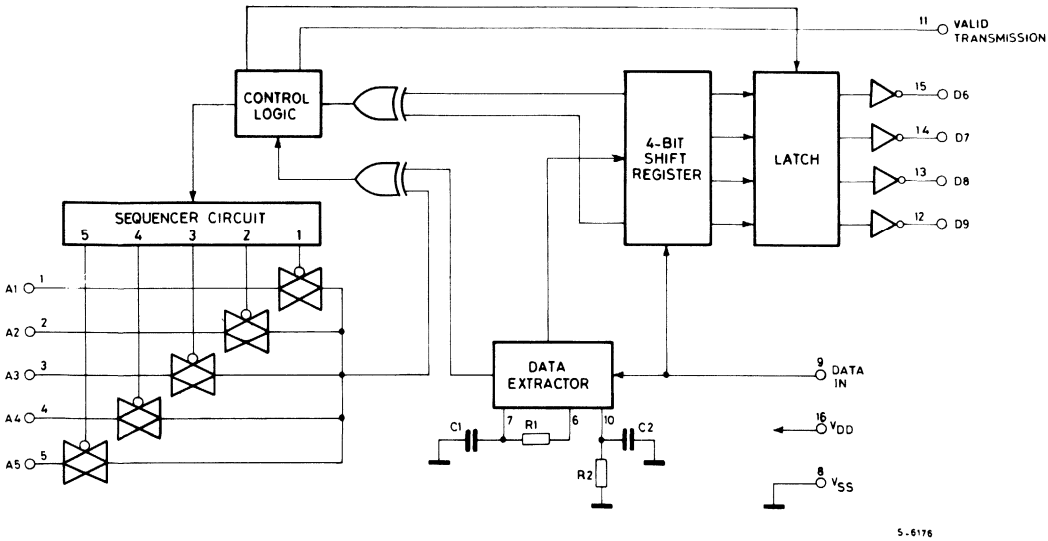
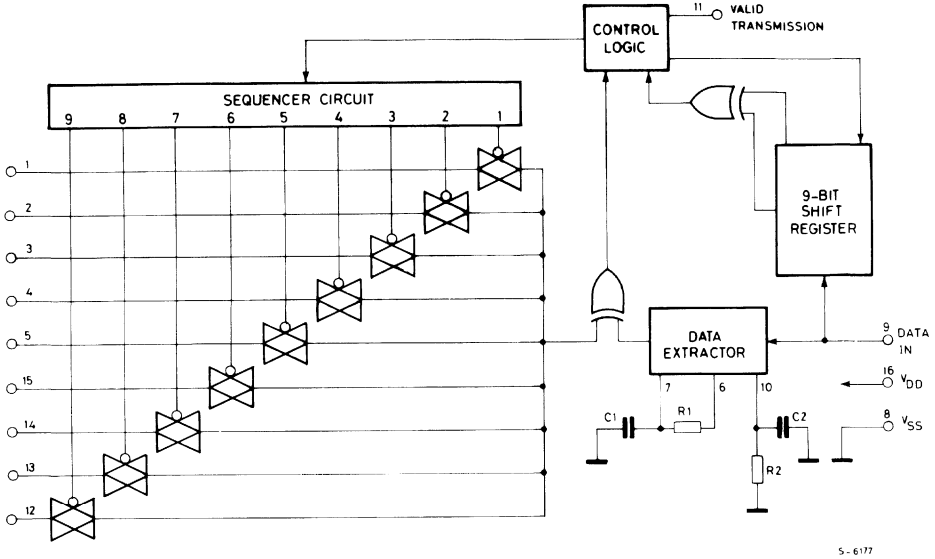


Fig. 3 - Decoder block diagram M145028



PIN DESCRIPTION

M145026 ENCODER

A1/D1-A9/D9
These inputs will be encoded and the data serially output from the encoder.

V_{SS}
The most negative supply (usually ground).

RS, CTC, RTC
These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

$\overline{TE}$
This Transmit-Enable (active low) input will initiate transmission when forced low. A pullup device will keep this input high normally.

Data Out
This is the output of the encoder that will present the serially encoded signals.

V_{DD}
The most positive supply.

M145027/M145028 DECODERS

A1-A5 (M145027) / A1-A9 (M145028)
These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in the case of M145027 or A1/D1-A0/D9in the case of M145028, in order for the decoder to output data.

D6-D9 (M145027)
These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9.
Note: Only binary data will be acknowledged, a trinary open will be decoded as logic one.

R1, C1
These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant R1 x C1 should be set to 1.72 transmit clock periods. R1C1 = 3.95 RTC x CTC.

R2/C2
This pin accepts a resistor to V_{SS} and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant R2 x C2 should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R2C2) to detect the dead time between transmitted words.
R2C2 = 77 x RTC x CTC.

Valid Transmission, VT
This output will go high when the following conditions are satisfied:

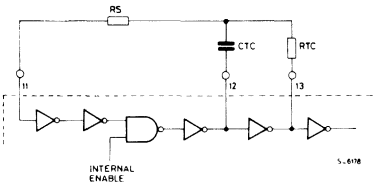
1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (M145028 only).

VT will remain high until either a mismatch is received, or no input signal is received for four data data bit times.

V_{DD}
The most positive supply

V_{SS}
The most negative supply (usually ground).

Figure 4 - Encoder Oscillator Information



This oscillator will operate at a frequency determined by the external RC network; i.e..

$$f \cong \frac{1}{2.3 \times RTC \times CTC} \text{ (Hz)}$$

for 1 kHz $\leq f \leq$ 400 kHz

where: CTC = CTC + C layout + 12 pF

RS $\approx$ 2 RTC
RS $\geq$ 20 k
RTC $\geq$ 10 k
400 pF $<$ CTC $<$ μF

The value for RS should be chosen to be about 2 times RTC. This range will ensure that current through RS is insignificant compared to current through RTC. The upper limit for RS must ensure that RS x 5 pF (input capacitance) is small compared to RTC x CTC.

For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1 Hz to over 1 MHz.

Figure 5 - Encoder/Decoder Timing Diagram

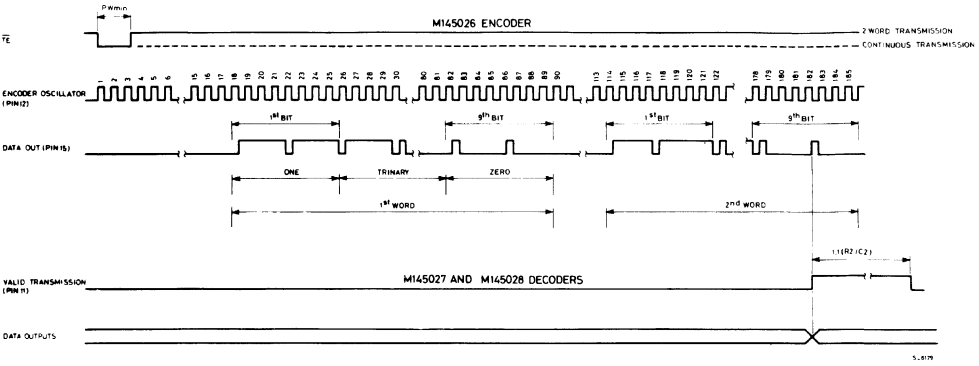


Figure 6 - Encoder Data Waveforms (M145026)

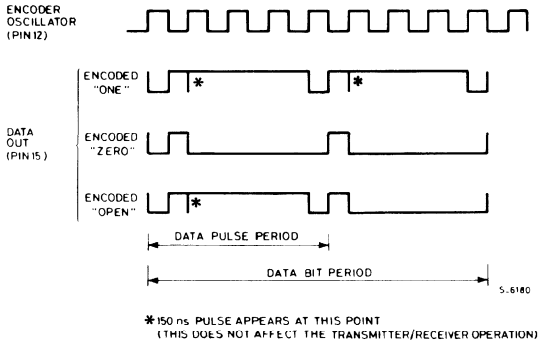


Figure 7 - M145027 Flowchart

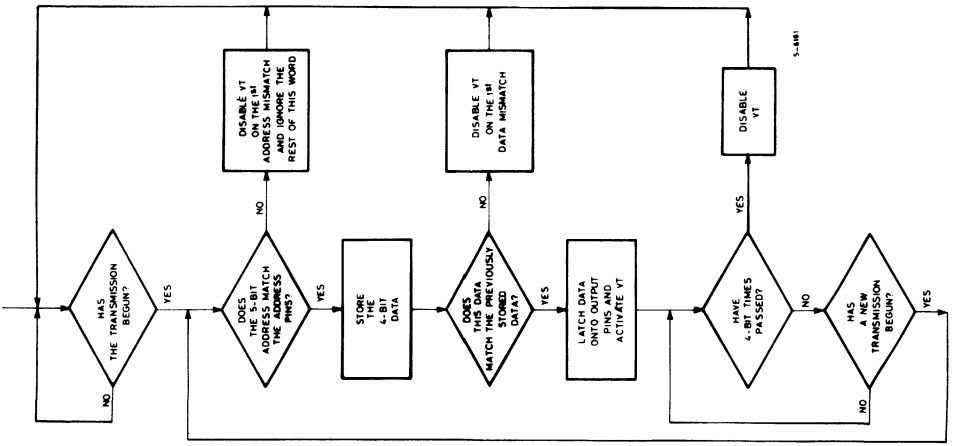


Figure 8 - M145028 Flowchart

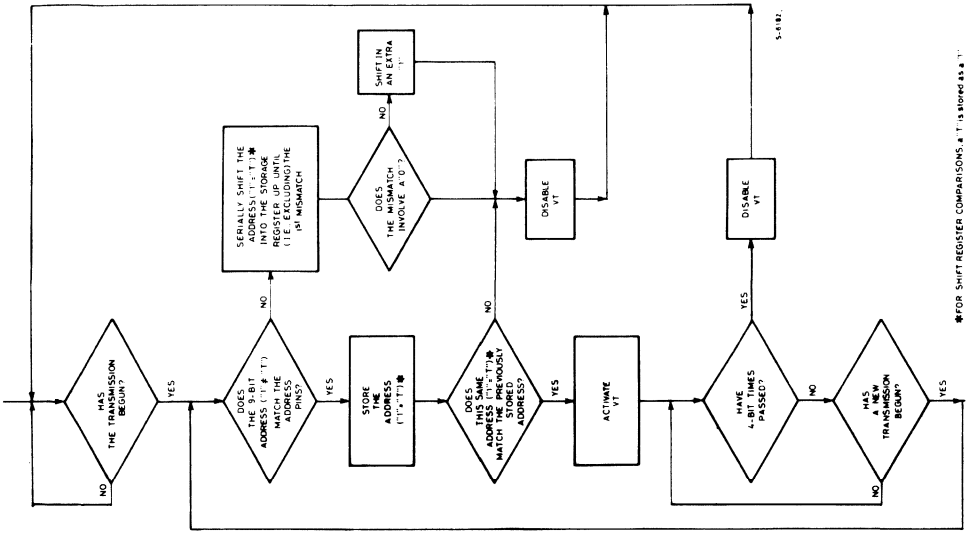


Figure 9 - M145027/M145028 (f_{max} vs. C_{layout})

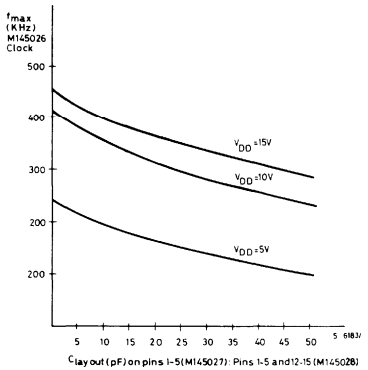
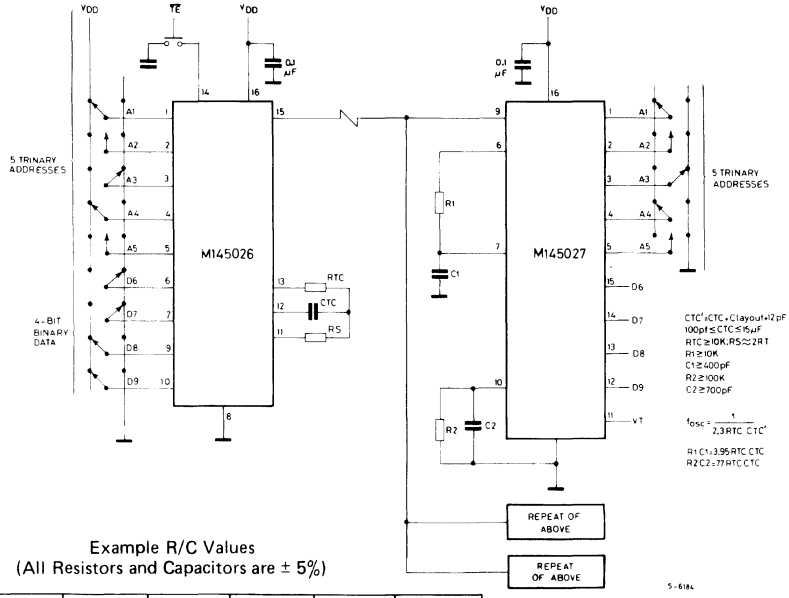


Figure 10 - Typical Application



Example R/C Values
(All Resistors and Capacitors are ± 5%)

(CTC' = CTC + 20 pF)

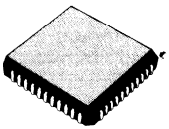
f_{osc}(kHz)	RTC	CTC'	RS	R1	C1	R2	C2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

S6040

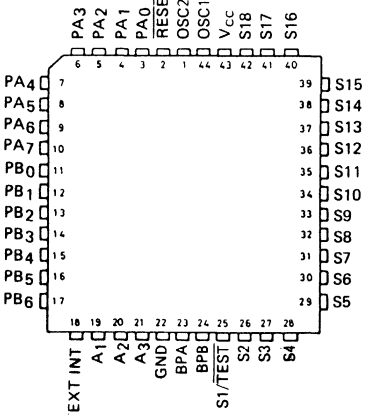
ADVANCE DATA

8 Bit MCU with 4K ROM A/D Converter and LCD Driver

- Single Chip HCMOS Microcomputer
- 4K Bytes Program ROM
- 64 Bytes Data ROM
- 64 Bytes Data RAM
- 3V to 6V Supply Voltage
- Fully Static CMOS Operation
- Power-On Reset
- External Interrupt Line
- 44 Pin PLCC Package
- Two On-Chip 8-Bit Timers with 7-Bit Prescaler
- On-Chip Watchdog Timer
- On-Chip 8-Bit A/D Converter with 3 Analog Inputs
- On-Chip Clock Oscillator
- 15 I/O Lines with Buffer Outputs (± 5 mA)
- 18 Lines LCD Driver for Max 36 Segments
- Standard and Extended Temperature Range



C
PLCC44 (Plastic)



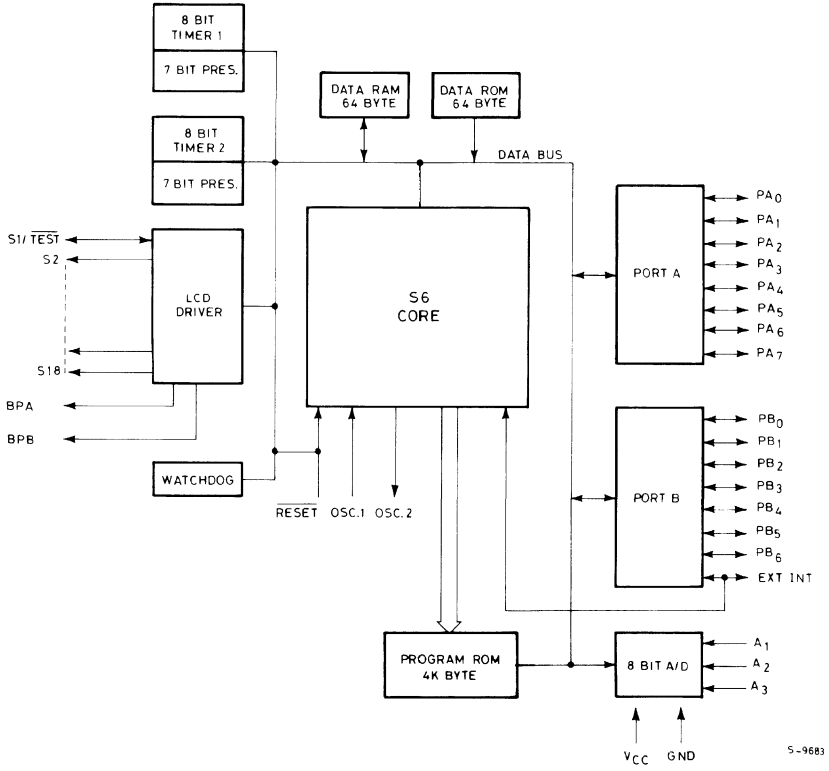
Chip Carrier Pin Configuration

General Description

The S6040 is a powerful member of the S6 single chip HCMOS microcomputer family, a series of devices oriented to low-medium complexity applications.
All S6 members are based on a building block approach: a common "core" is surrounded by a combination of dedicated functions (macrocells), e.g., A/D converter, timers, LCD drivers, etc.
The S6 Core is characterized by an 8-bit serial architecture that, minimizing the silicon area, is reflected in the economical solution offered to the customer.
The ALU is reduced to a 1-bit adder, and most of Data Bus connections are 1-bit rather than 8-bit wide.
The S6 Core includes a 12-bit Program Counter, a 4-level hardware Stack, an Accumulator, Control Logic and an Oscillator.

General Description (Continued)

The program ROM, data RAM and data ROM are of variable size to meet different application complexities.
The S6 instruction set is designed for byte-efficient program storage and inciudes relative jumps, call, arithmetic, load, store and bit manipulation instructions. To reduce power consumption in the stand-by mode, STOP and WAIT instructions are implemented.
The combination of the serial architecture with the HCMOS technology, and with the application specific dedicated macrocells, is reflected on a cost effective solution offered to the user.



S6040 - Block Diagram

Pin Descriptions

V_{CC}, GND. Power Supply Pins.
Power is supplied to the MCU using these two pins.

OSC1, OSC2. On Chip Oscillator Pins (OSC1-input, OSC2-output).
These pins permit connection to the on-chip clock oscillator circuit. A user can connect to these pins a crystal quartz, a ceramic resonator or an external signal to provide the selected system clock.

$\overline{\text{RESET}}$. External Reset Pin (input active low).
Reset initializes the S6040 and restarts the processor at the beginning of the program.

A1, A2, A3. Analog Inputs.
Analog inputs for the 8-bit A/D converter.

BPA, BPB. Backplane Output Pins.
These pins are the outputs of on-chip backplane voltage generator used to permit multiplexing by 2 of 18 LCD driver lines (36 segments).

S1/$\overline{\text{TEST}}$. LCD Segment 1/Test Mode.
This pin is the LCD segment driver 1 but also enables the factory test mode when tied low when the system reset is active.

S2 - S18. LCD Segments 2 to 18.
LCD segments driver outputs 2 to 18.

PA_0, PA_7, PB_0, PB_6. Digital I/O lines.
Port A and Port B lines are programmable to be either input or output. High drive capability (+5 mA) is also guaranteed. These lines have schmitt trigger inputs.

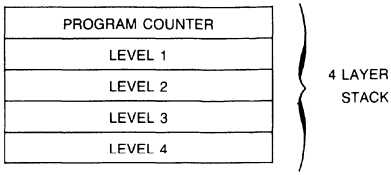
EXT INT. External Interrupt (rising edge sensitive).
This pin acts as an external interrupt line. A low to high transition on this pin causes an external intempt. This pin gives the possibility to asynchronously apply on external interrupt to the S6040.

Functional Description

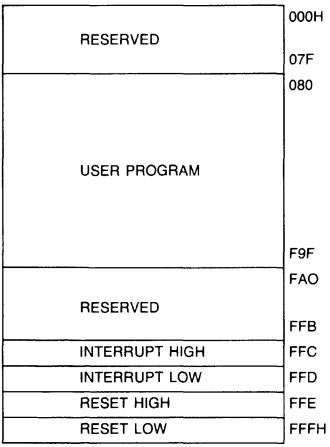
The S6040 has three different memory spaces:

- the program space
- the data space
- the stack space

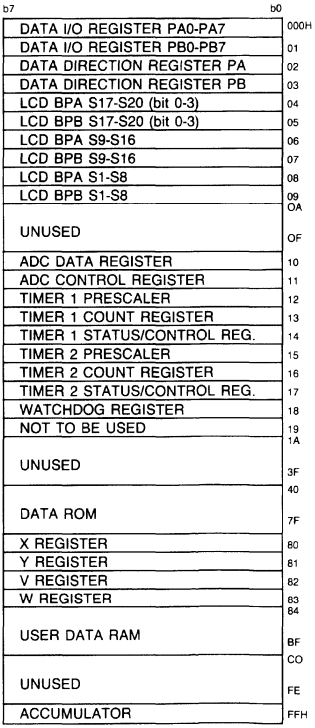
The program space holds the user program to be executed by the MCU and also contains the interrupt and restart vectors. This memory is of a ROM nature and the S6040 offers a size of 4K bytes.
The data space consists of RAM locations and ROM locations used for the storage of constants and tables, accumulator register, I/O data and control register, on-chip dedicated macrocell control registers, -Y-V-W registers.



S6040 - Stock Space



S6040 - Program Memory Space



S6040 - Data Memory Space

Absolute Maximum Ratings

Operating temperature S6040 B1 ..... 0 to +70 °C
B6 ..... −40 to 85 °C
Storage temperature ..... −55 to +125 °C
Supply Voltage ..... −0.5 to +7 V
Voltage on any I/O pins ..... −0.5 to V_{CC} +0.5 V
Total power dissipation ..... 300 mW
DIP $R_{th\ j\text{-}amb}$ on test board ..... 70 °C/W
Oscillator frequency ..... 0 to 4 MHz

Note: Stresses above those listed as "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

V_{CC} = 5V ± 10% T_A = 25 °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{IL}	Input Low Voltage			1.6	V	
V_{IH}	Input High Voltage	3.4			V	
V_{ILR}	Input Low Voltage Reset			1.6	V	
V_{IHR}	Input High Voltage Reset	3.4			V	
V_{OL}	Output Low Voltage			0.8	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −5mA
I_L	Input Leakage Current			−1.0	μA	V_I = GND
	Input Leakage Current			+1.0	μA	V_I = V_{CC}
I_{CC}	Supply Current		3.5		mA	f_{osc} = 4MHz C_L = 0pF
	Supply Current		1.0		μA	STOP Mode

Power-On Reset Characteristics

V_{CC} = 5V ± 10% T_A = 25 °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{TON}	Trigger Level ON	1.4			V	
V_{TOFF}	Trigger Level OFF			3.0	V	
t_{rise}	Supply Rise Time	.01		1000	mS	
t_{rec}	Supply Recovery Time	1.0			S	

Oscillator Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
f_{osc}	Oscillator Frequency			4.0	MHz	
t_{BU}	Built up time			200	mS	
C_{osc1}	Input Capacitance OSC1 pin			9	pF	
C_{osc2}	Output Capacitance OSC2 pin			9	pF	

A/D Converter Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = 25$ °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
I_{LA1}	Input Leakage Current Analog			−0.1	μA	GND on all analog inputs
I_{LA2}	Input Leakage Current Analog			+0.1	μA	V_{CC} out all analog inputs
RES	Resolution	20			mV	$V_{CC} = 5V \pm 10mV$
LIN	Linearity			±1	LSB	$V_{CC} = 5V \pm 10mV$
t_{con}	Conversion Time		132	150	μS	fosc = 4MHz (1)
C_{AN}	Analog Input Capacitance			4.0	pF	
R_{AN}	Analog Input Impedance			30	KΩ	

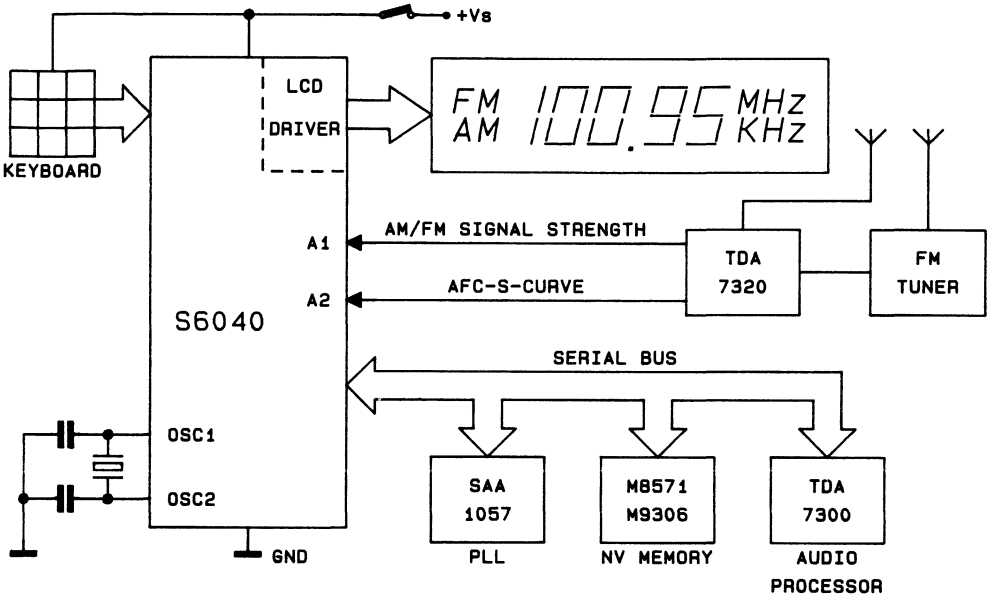
(1) With Clock frequencies less than 1 MHz, the A/D converter accuracy decrease.

LCD Driver Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = 25$ °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
f_{BP}	Backplane Frequency		80		Hz	fosc = 4 MHz
V_{OF}	DC Offset Voltage			50	mV	
V_{OHBP}	Output Voltage High	4.5			V	I = 100 μA on BPA, BPB
V_{OLBP}	Output Voltage Low			0.5	V	I = − 100 μA on BPA, BPB
V_{OHS}	Output Voltage High	4.5			V	I = 50 μA S1-S18
V_{OLS}	Output Voltage Low			0.5	V	I = 50 μA S1-S18

Typical Application



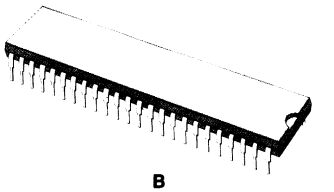
S-9747

S6041

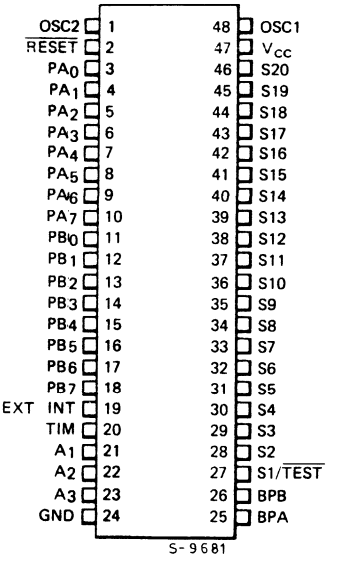
ADVANCE DATA

8 Bit MCU with 4K ROM A/D Converter and LCD Driver

- Single Chip HCMOS Microcomputer
- 4K Bytes Program ROM
- 64 Bytes Data ROM
- 64 Bytes Data RAM
- 3V to 6V Supply Voltage
- Fully Static CMOS Operation
- Power-On Reset
- External Interrupt Line
- 48 Pin DIP Package
- Two On-Chip 8-Bit Timers with 7-Bit Prescaler
- On-Chip Watchdog Timer
- On-Chip 8-Bit A/D Converter with 3 Analog Inputs
- On-Chip Clock Oscillator
- 16 I/O Lines with Buffer Outputs (± 5 mA)
- 20 Lines LCD Driver for Max 40 Segments.
- Standard and Extended Temperature Range



B
DIP-48 (Plastic)



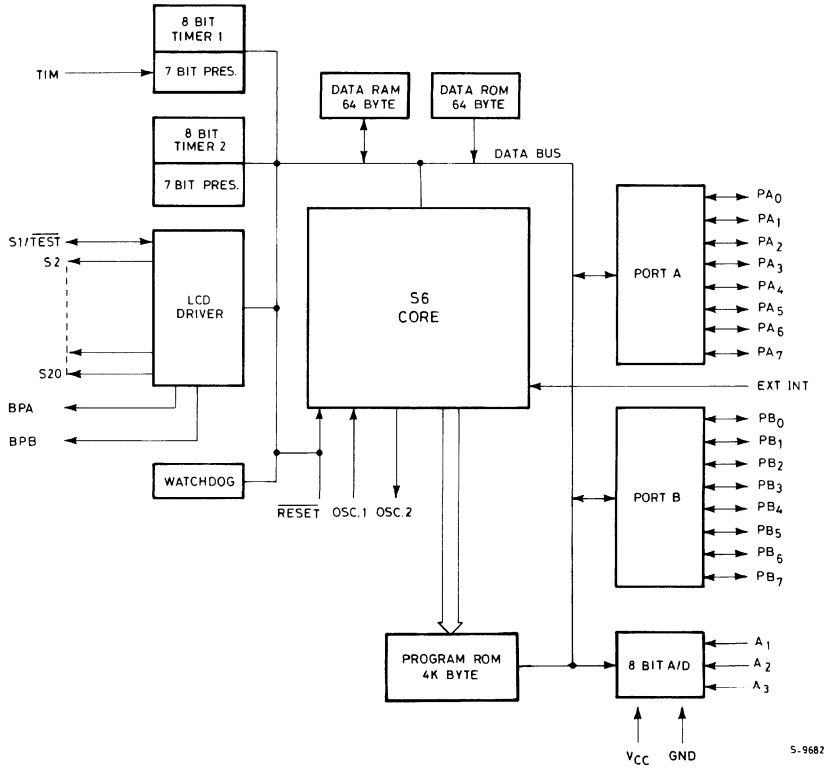
Dual In Line Pin Configuration

General Description

The S6041 is a powerful member of the S6 single chip HCMOS microcomputer family, a series of devices oriented to low-medium complexity applications.
All S6 members are based on a building block approach: a common "core" is surrounded by a combination of dedicated functions (macrocells), e.g., A/D converter, timers, LCD drivers, etc.
The S6 Core is characterized by an 8-bit serial architecture that, minimizing the silicon area, is reflected in the economical solution offered to the customer.
The ALU is reduced to a 1-bit adder, and most of Data Bus connections are 1-bit rather than 8-bit wide.
The S6 Core includes a 12-bit Program Counter, a 4-level hardware Stack, an Accumulator, Control Logic and an Oscillator.

General Description (Continued)

The program ROM, data RAM and data ROM are of variable size to meet different application complexities.
The S6 instruction set is designed for byte-efficient program storage and includes relative jumps, call, arithmetic, load, store and bit manipulation instructions. To reduce power consumption in the stand-by mode, STOP and WAIT instructions are implemented.
The combination of the serial architecture with the HCMOS technology, and with the application specific dedicated macrocells, is reflected on a cost effective solution offered to the user.



S6041 - Block Diagram

Pin Descriptions

V_{CC}, GND. Power Supply Pins.
Power is supplied to the MCU using these two pins.

OSC1, OSC2. On Chip Oscillator Pins (OSC1-input, OSC2-output).
These pins permit connection to the on-chip clock oscillator circuit. A user can connect to these pins a crystal quartz, a ceramic resonator or an external signal to provide the selected system clock.

$\overline{\text{RESET}}$. External Reset Pin (input active low).
Reset initializes the S6041 and restarts the processor at the beginning of the program.

A1, A2, A3. Analog Inputs.
Analog inputs for the 8-bit A/D converter.

BPA, BPB. Backplane Output Pins.
These pins are the outputs of on-chip backplane voltage generator used to permit multiplexing by 2 of 20 LCD driver lines (40 segments).

S1/$\overline{\text{TEST}}$. LCD Segment 1/Test Mode.
This pin is the LCD segment driver 1 but also enables the factory test mode when tied low when the system reset is active.

S2 - S20. LCD Segments 2 to 20.
LCD segments driver outputs 2 to 20.

PA_0, PA_7, PB_0, PB_7. Digital I/O lines.
Port A and Port B lines are programmable to be either input or output. High drive capability (+5 mA) is also guaranteed. These lines have schmitt trigger inputs.

EXT INT. External Interrupt (falling edge sensitive).
This pin allows to apply an external falling edge interrupt to the S6041.

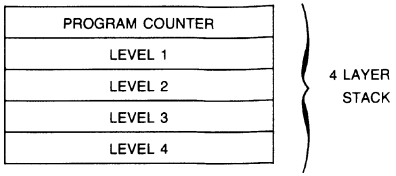
TIM. Timer I/O Pin (Timer 1).
In the input mode this pin is connected to the prescaler and acts as timer 1 clock. In the output mode the timer pin inform that a time out has occurred.

Functional Description

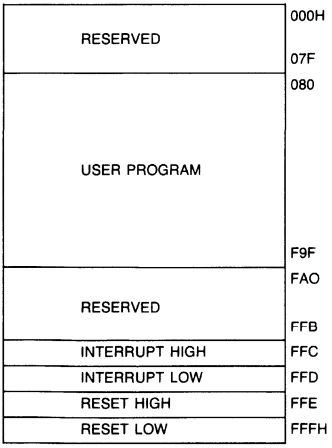
The S6041 has three different memory spaces:

- the program space
- the data space
- the stack space

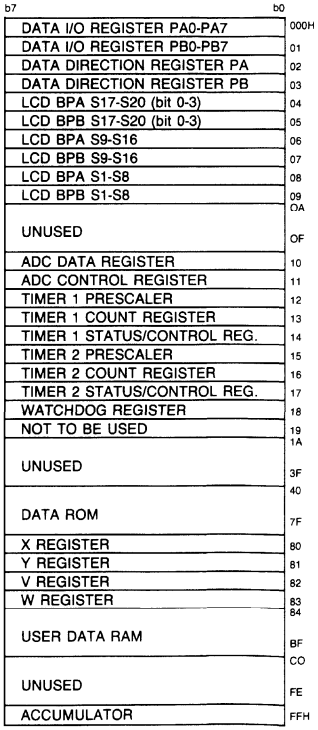
The program space holds the user program to be executed by the MCU and also contains the interrupt and restart vectors. This memory is of a ROM nature and the S6041 offers a size of 4K bytes.
The data space consists of RAM locations and ROM locations used for the storage of constants and tables, accumulator register, I/O data and control register, on-chip dedicated macrocell control registers, -Y-V-W registers.



S6041 - Stock Space



S6041 - Program Memory Space



S6041 - Data Memory Space

Absolute Maximum Ratings

Operating temperature S6041 B1	0 to +70 °C
B6	−40 to 85 °C
Storage temperature	−55 to +125 °C
Supply Voltage	−0.5 to +7 V
Voltage on any I/O pins	−0.5 to V_{CC} +0.5 V
Total power dissipation	300 mW
DIP $R_{th\ j\text{-}amb}$ on test board	70 °C/W
Oscillator frequency	0 to 4 MHz

Note: Stresses above those listed as "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

V_{CC} = 5V ± 10% T_A = 25 °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{IL}	Input Low Voltage			1.6	V	
V_{IH}	Input High Voltage	3.4			V	
V_{ILR}	Input Low Voltage Reset			1.6	V	
V_{IHR}	Input High Voltage Reset	3.4			V	
V_{OL}	Output Low Voltage			0.8	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −5mA
I_L	Input Leakage Current			−1.0	µA	V_I = GND
	Input Leakage Current			+1.0	µA	V_I = V_{CC}
I_{CC}	Supply Current		3.5		mA	f_{osc} = 4MHz C_L = 0pF
	Supply Current		1.0		µA	STOP Mode

Power-On Reset Characteristics

V_{CC} = 5V ± 10% T_A = 25 °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{TON}	Trigger Level ON	1.4			V	
V_{TOFF}	Trigger Level OFF			3.0	V	
t_{rise}	Supply Rise Time	.01		1000	mS	
t_{rec}	Supply Recovery Time	1.0			S	

Oscillator Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
f_{osc}	Oscillator Frequency			4.0	MHz	
t_{BU}	Built up time			200	mS	
C_{osc1}	Input Capacitance OSC1 pin			9	pF	
C_{osc2}	Output Capacitance OSC2 pin			9	pF	

A/D Converter Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = 25$ °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
I_{LA1}	Input Leakage Current Analog			−0.1	μA	GND on all analog inputs
I_{LA2}	Input Leakage Current Analog			+0.1	μA	V_{CC} out all analog inputs
RES	Resolution	20			mV	$V_{CC} = 5V \pm 10mV$
LIN	Linearity			±1	LSB	$V_{CC} = 5V \pm 10mV$
t_{con}	Conversion Time		132	150	μS	fosc = 4MHz (1)
C_{AN}	Analog Input Capacitance			4.0	pF	
R_{AN}	Analog Input Impedance			30	KΩ	

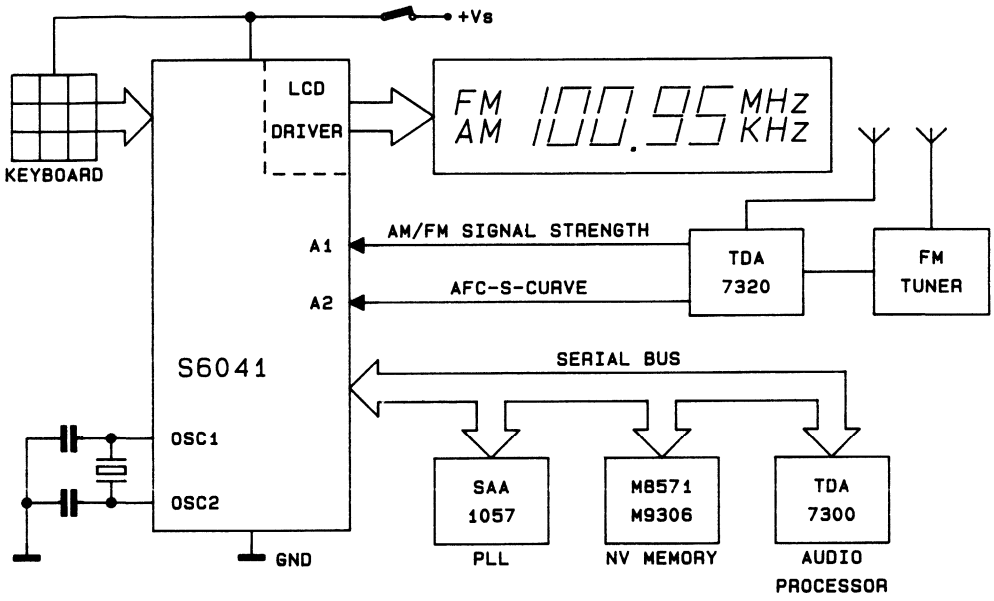
(1) With Clock frequencies less than 1 MHz, the A/D converter accuracy decrease.

LCD Driver Characteristics

$V_{CC} = 5V \pm 10\%$ $T_A = 25$ °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
f_{BP}	Backplane Frequency		80		Hz	fosc = 4 MHz
V_{OF}	DC Offset Voltage			50	mV	
V_{OHBP}	Output Voltage High	4.5			V	I = 100 μA on BPA, BPB
V_{OLBP}	Output Voltage Low			0.5	V	I = −100 μA on BPA, BPB
V_{OHS}	Output Voltage High	4.5			V	I = 50 μA on S1-S20
V_{OLS}	Output Voltage Low			0.5	V	I = 50 μA on S1-S20

Typical Application



S-9747

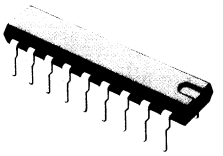
SAA1057

ADVANCE DATA

PLL RADIO TUNING SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

- ON-CHIP PRESCALER WITH UP TO 120 MHz INPUT FREQUENCY.
- ON-CHIP AM AND FM INPUT AMPLIFIERS WITH HIGH SENSITIVITY (30 mV AND 10 mV RESPECTIVELY).
- LOW CURRENT DRAIN (TYPICALLY 16 mA FOR AM AND 20 mA FOR FM) OVER A WIDE SUPPLY VOLTAGE RANGE (3.6 V TO 12 V).
- ON-CHIP AMPLIFIER FOR LOOP FILTER FOR BOTH AM AND FM (UP TO 30 V TUNING VOLTAGE
- ON-CHIP PROGRAMMABLE CURRENT AMPLIFIER (CHARGE PUMP) TO ADJUST THE LOOP GAIN
- ONLY ONE REFERENCE FREQUENCY FOR BOTH AM AND FM
- HIGH SIGNAL PURITY DUE TO A SAMPLE AND HOLD PHASE DETECTOR FOR THE IN-LOCK CONDITION.
- HIGH TUNING SPEED DUE TO A POWERFUL DIGITAL MEMORY PHASE DETECTOR DURING THE OUT-LOCK CONDITION.
- TUNING STEPS FOR AM ARE: 1 kHz OR 1.25 kHz FOR A VCO FREQUENCY RANGE OF 512 kHz TO 32 MHz
- TUNING STEPS FOR FM ARE: 10 kHz OR 12.5 kHz FOR A VCO FREQUENCY RANGE OF 70MHz TO 120 MHz
- SERIAL 3-LINE BUS INTERFACE TO A MICROCOMPUTER
- TEST/FEATURES.



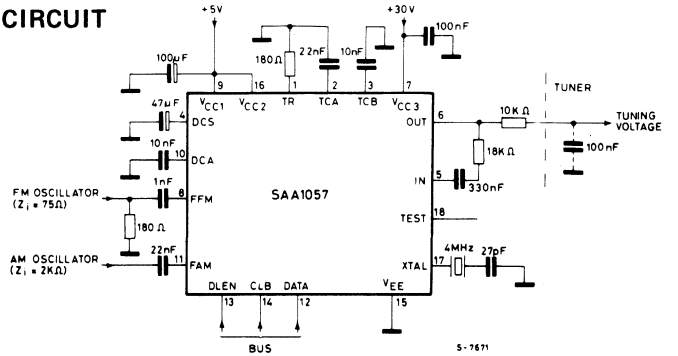
DIP-18 Plastic

ORDER CODE: SAA 1057

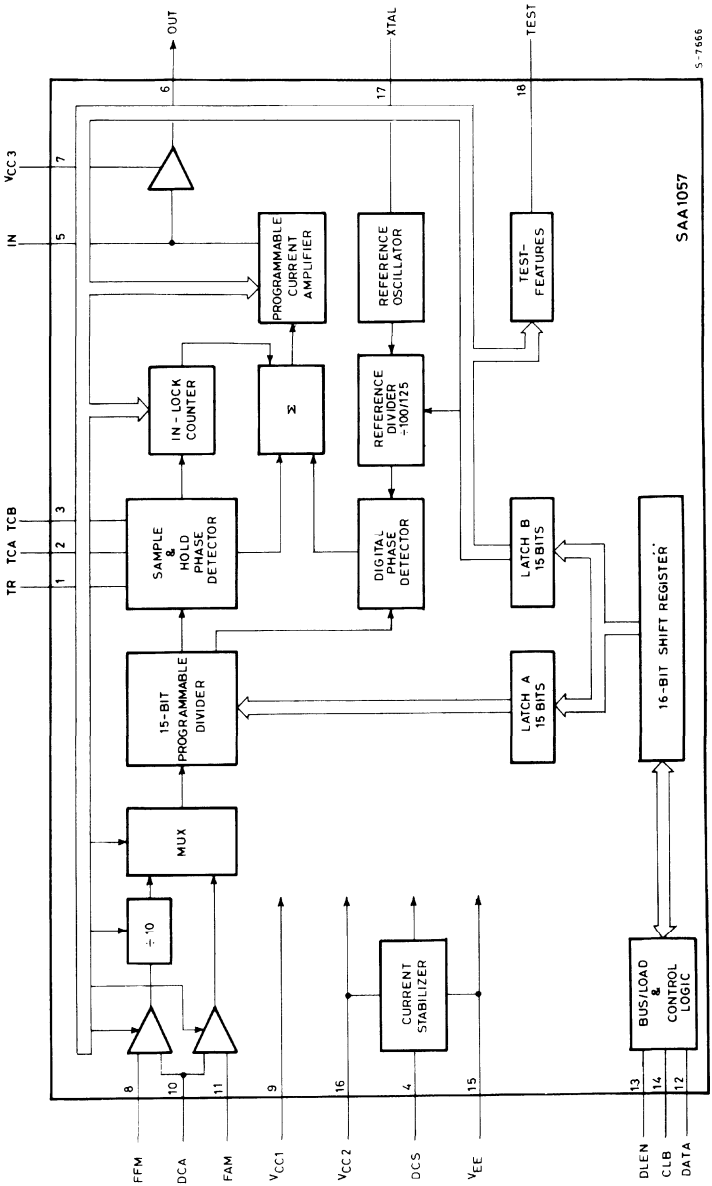
QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3.6 to 12	V
	V_{CC2}	3.6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0.8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	F_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	-25 to +80	°C

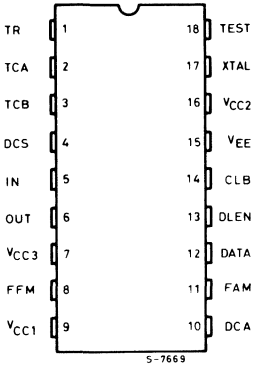
APPLICATION CIRCUIT



BLOCK DIAGRAM



CONNECTION DIAGRAM



PINNING

1	TR	resistor/capacitors
2	TCA	for sample and
3	TCB	hold circuit
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	
13	DLEN	BUS
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

ABSOLUTE MAXIMUM RATINGS

V_{CC1}; V_{CC2}	Supply voltage; logic and analogue part	-0.3 to 13.2	V
V_{CC3}	Supply voltage; output amplifier	V_{CC2} to + 32	V
P_{tot}	Total power dissipation	max. 800	mW
T_{amb}	Operating ambient remperature range	-30 to + 85	°C
T_{stg}	Storage temperature range	-65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25°C; unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{CC1}	Supply voltages		3.6	5	12	V
V_{CC2}			3.6	5	12	V
V_{CC3}			V_{CC2}	–	31	V
	Supply currents *					
I_{tot}	AM mode	$I_{tot} = I_{CC1} + I_{CC2}$	–	16	–	mA
I_{tot}	FM mode	in-lock; BRM = '1';	–	20	–	mA
I_{CC3}		$I_{OUT} = 0$	0.3	0.8	1.2	mA
T_{amb}	Operating ambient temperature		-25	–	+80	°C

* When the bus is in the active mode (see BRM in Control Information), 4.5 mA should be added to the figures given.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
	RF inputs (FAM, FFM)					
f_{FAM}	AM input frequency		512 kHz	–	32	MHz
f_{FFM}	FM input frequency		70	–	120	MHz
$V_{i(rms)}$	Input voltage at FAM		30	–	500	mV
$V_{i(rms)}$	Input voltage at FFM		10	–	500	mV
R_i	Input resistance at FAM		–	2	–	kΩ
R_i	Input resistance at FFM		–	135	–	Ω
C_i	Input capacitance at FAM		–	3.5	–	pF
C_i	Input capacitance at FFM		–	3	–	pF
V_s/V_{ns}	Voltage ratio allowed between selected and non-selected input		–	-30	–	dB
	Crystal oscillator (XTAL)	see note 1				
f_{XTAL}	Maximum input frequency		4	–	–	MHz
R_s	Crystal series resistance		–	–	150	Ω
	BUS inputs (DLEN, CLUB, DATA)					
V_{IL}	Input voltage LOW		0	–	0.8	V
V_{IH}	Input voltage HIGH		2.4	–	V_{CC1}	V
$-I_{IL}$	Input current LOW	V_{IL} = 0.8 V	–	–	10	μA
I_{IH}	Input current HIGH	V_{IH} = 2.4 V	–	–	10	μA
	BUS inputs timing (DLEN, CLB, DATA)	see also Fig. 2 and note 2				
$t_{CLBlead}$	Lead time for CLB to DLEN		1	–	–	μs
t_{Tlead}	Lead time for DATA to the first CLB pulse		0.5	–	–	μs
$t_{CLBlag1}$	Set-up time for DLEN to CLB		5	–	–	μs
t_{CLBH}	CLB pulse width HIFH		5	–	–	μs
t_{CLBL}	CLB pulse width LOW		5	–	–	μs
$t_{DATAlead}$	Set-up time for DATA to CLB		8	–	–	μs
$t_{DATAhold}$	Hold time for DATA to CLB		0	–	–	μs
$t_{DLENhold}$	Hold time for DLEN to CLB		2	–	–	μs
$t_{CLBlag2}$	Set-up time for DLEN to CLB load pulse		2	–	–	μs
t_{DIST}	Busy time from load pulse to next start to transmission	next transmission after word 'B' to other device	5	–	–	μs
t_{DIST}	Busy time	or	0.3	–	–	ms
	asynchronous mode	next transmission to SAA1057 after word 'A'	1.3	–	–	ms
	Sample and hold circuit (TR, TCA, TCB)	see also notes 3; 4				
$V_{TCA,VTCB}$	Minimum output voltage		–	1.3	–	V
$V_{TCA,VTCB}$	Maximum output voltage		–	–	V_{CC2}-0.7	V
C_{TCA}	Capacitance at TCA	REFH = '1'	–	–	2.2	nF
CTA	(external)	REFH = '0'	–	–	2.7	nF
t_{DIS}	Discharge time at TCA	REFH = '1'	–	–	5	μs
		REFH = '0'	–	–	6.25	μs
R_{TR}	Resistance at TR	external	100	–	–	Ω

ELECTRICAL CHARACTERISTICS (continued)

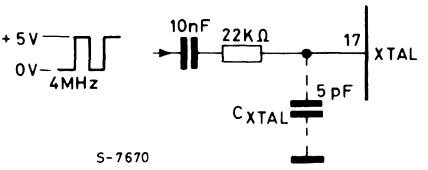
Parameter						Test Conditions	Min.	Typ.	Max.	Unit
V_{TR}	Voltage at TR during discharge						–	0.7	–	V
C_{TCB}	Capacitance at TCB					external	–	–	10	nF
I_{bias}	Bias current into TCA, TCB					in-look	–	–	10	nA
	Programmable current amplifier (PCA)									
$\pm I_{dig}$	Output current of the dig. phase detector						–	0.4	–	mA
	Current gain of PCA	CP3	CP2	CP1	CP0					
G_{P1}	P1	0	0	0	0	$V_{CC2} \geq 5$ V (only for P1)	–	0.023	–	
G_{P2}	P2	0	0	0	1		–	0.07	–	
G_{P3}	P3	0	0	1	0		–	0.23	–	
G_{P4}	P4	0	1	1	0		–	0.7	–	
G_{P5}	P5	1	1	1	0		–	2.3	–	
	Ratio between the output current of S/H into PCA and the voltage on									
S_{TCB}	C_{TCB}						–	1.0	–	μA/A
ΔV_{TCB}	Offset voltage on TCB					in lock	–	–	1	V
	Output amplifier (IN, OUT)									
V_{IN}	Input voltage					in-lock; equal to internal reference voltage	–	1.3	–	V
V_{OUT}	Output voltages minimum					$-I_{OUT}$ = 1 mA	–	–	0.5	V
V_{OUT}	Output voltages maximum					I_{OUT} = 1 mA	V_{CC3}-2	–	–	V
V_{OUT}	Output voltages maximum					I_{OUT} = 0.1 mA	V_{CC3}-1	–	–	V
$\pm I_{OUT}$	Maximum output current					V_{OUT} = ½ V_{CC3}	5	–	–	mA
	Test output (TEST) *									
V_{TL}	Output voltage LOW						–	–	0.5	V
V_{TH}	Output voltage HIGH						–	–	12	V
I_{Toff}	Output current OFF					V_{TH}	–	–	10	μA
I_{Ton}	Output current ON					V_{TL}	150	–	–	μA
	Ripple rejection **									
	at f_{ripple} = 100 Hz									
	$\Delta V_{CC1}/\Delta V_{OUT}$						–	77	–	dB
	$\Delta V_{CC2}/\Delta V_{OUT}$						–	70	–	dB
	$\Delta V_{CC3}/\Delta V_{OUT}$					$V_{OUT} \leq V_{CC3}$-3	–	60	–	dB

* Open collector output ** Measured in Fig. 6

NOTES

1. Pin 17 (XTAL) can also be used as an input for an external clock.
   The values given in Fig. 1 are a typical application example.
2. See BUS information in section 'operation description .
3. The output voltage at TCB and TCA is typically ½V_{CC2}+0.3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½V_{CC2}+0.3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.

Fig. 1 - Circuit configuration showing external 4 MHz clock



SAA1057

GENERAL DESCRIPTION

The SAA1057 performs the entire PPL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signal.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An-in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1.25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1.25 kHz for AM, and 10 kHz and 12.5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the runing system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B, For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1.25 kHz, '0' = 1 kHz (sample and hold phase (detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Electrical Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B;
'1' enables '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

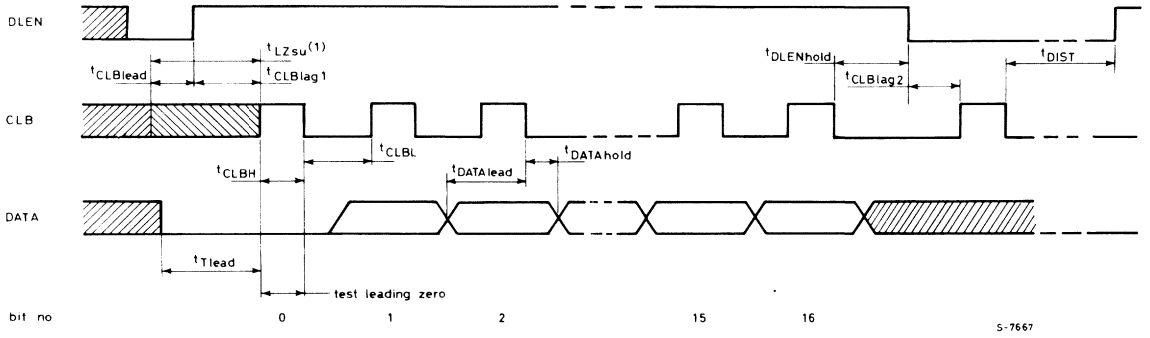
T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

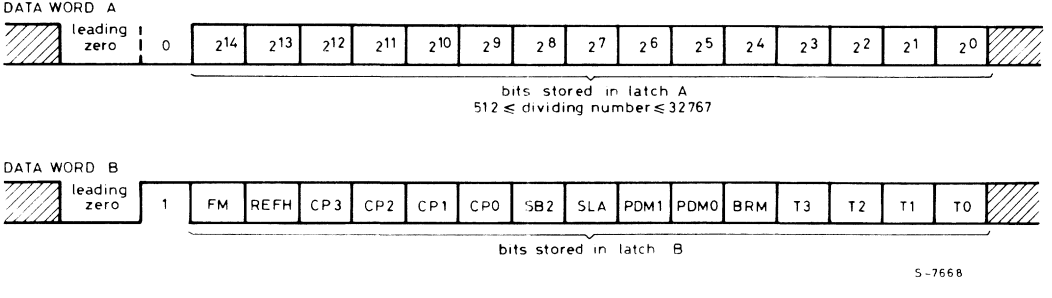
T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output progrrammable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

Fig. 2 - BUS format



(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I²C bus is used for other devices on the same data and clock lines

Fig. 3 - Bit organization of data words A and B



APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.

For the complete initialization (defining all control bits) a transmission of word B should follow. This menas that the IC is ready to accept word A.

Synchronous/asynchronous operation

Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

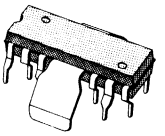
The lowest current gain (0.023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Electrical Characteristics').

NOT FOR NEW DESIGN

FULLY-PROTECTED 7W AUDIO AMPLIFIER

- HIGH OUTPUT POWER (7W AT 16V/4Ω; 14.4V/2Ω)
- HIGH OUTPUT CURRENT (3A REPETITIVE)
- LOAD DUMP PROTECTION UP TO 40V
- LOAD SHORT CIRCUIT PROTECTION UP TO V_s = 15V
- POLARITY INVERSION PROTECTION
- THERMAL PROTECTION

The TBA810CB is a monolithic integrated circuit in a 12-lead quad in-line plastic package, expressly designed for use as a power audio amplifier in CB radios.



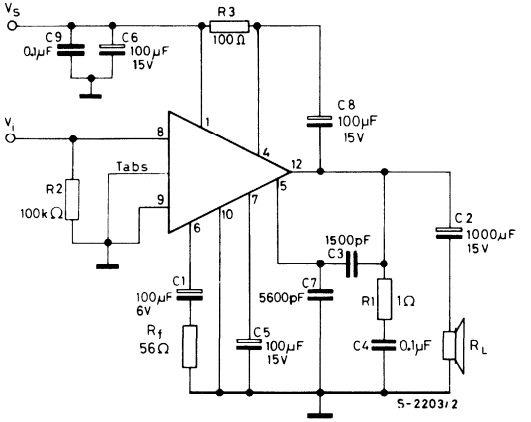
Findip

ORDERING NUMBER: TBA810CB

ABSOLUTE MAXIMUM RATINGS

$V_{s\ (peak)}$	Peak supply voltage (50ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	20	V
I_o	Output peak current (non repetitive)	4	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation at $T_{amb} \leqslant 80°C$	1	W
	at $T_{tab} \leqslant 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

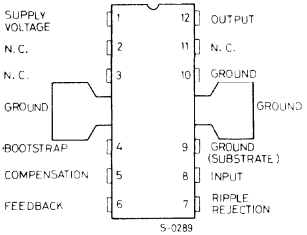
TEST AND APPLICATION CIRCUIT



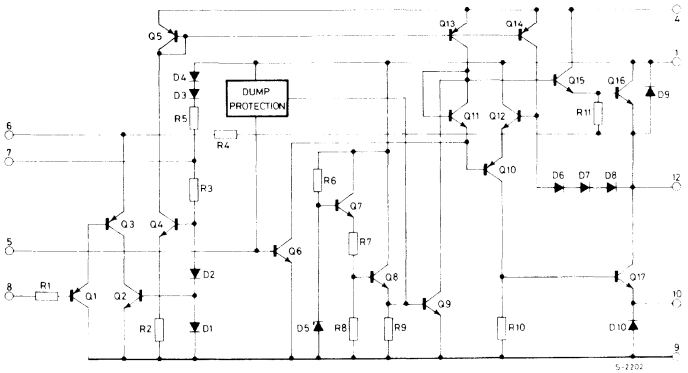
*C3, C7 SEE FIG.6

TBA810CB

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambeint	max	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)		6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Input bias current (pin 8)			0.4		μA
P_o	Output power	d = 10% f = 1 kHz R_L = 4Ω R_L = 2Ω	 5.5 5.5	 6 7		 W W
$V_{i(rms)}$	Input saturation voltage		220			mV
V_i	Input sensitivity	f = 1 kHz P_o = 6W R_L = 4Ω R_f = 56Ω R_f = 22Ω P_o = 7W R_L = 2Ω R_f = 56Ω R_f = 22Ω		 75 30 55 20		 mV mV mV mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3 dB)	R_L = 4Ω/2Ω C_3 = 820 pF C_3 = 1500 pF		40 to 20 000 40 to 10 000		Hz Hz
d	Distortion	P_o = 50 mW to 2.5W R_L = 4Ω/2Ω f = 1 kHz		0.3		%
G_v	Voltage gain (open loop)	R_L = 4Ω f = 1 kHz		80		dB
G_v	Voltage gain (closed loop)	R_L = 4Ω/2Ω f = 1 kHz	34	37	40	dB
e_N	Input noise voltage	V_s = 16V B (-3 dB) = 40 to 15 000 Hz		2		μV
i_N	Input noise current			80		pA
η	Efficiency	P_o = 6W R_L = 4Ω f = 1 kHz		75		%
SVR	Supply voltage rejection	R_L = 4Ω V_{ripple} = 1 V_{rms} f_{ripple} = 100 Hz	40	48		dB

TBA810P

NOT FOR NEW DESIGN

7W AUDIO AMPLIFIER

The TBS810P is an improvement of TBA810S.

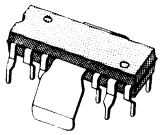
It offers:

- Higher output power (R_L = 4Ω and 2Ω)
- Low noise
- Polarity inversion protection
- Fortuitous open ground protection
- High supply voltage rejection (40dB min.)

The TBA810P is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.

The TBA810P provides 7W output power at 16V/4Ω; 7W at 14.4/2Ω.

It gives high output current (up to 3A), high efficiency (75% at 60W output) very low harmonic and crossover distortion. The circuit is provided with a thermal limiting circuit and can withstand a short-circuit on the load for supply voltages up to 15V.



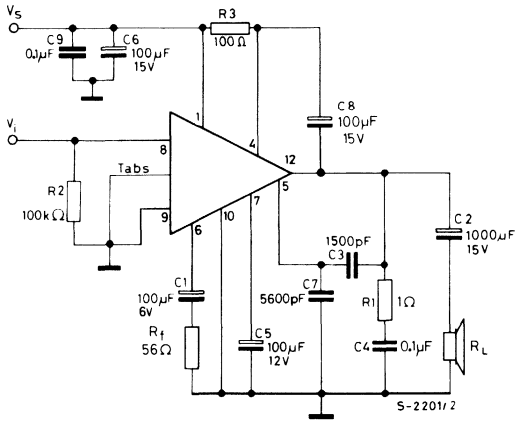
Findip

ORDER CODE: TBA810P

ABSOLUTE MAXIMUM RATINGS

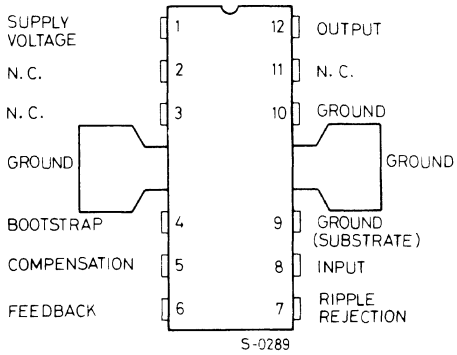
V_s	Supply voltage	20	V
I_o	Output peak current (non repetitive)	4	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation at $T_{amb} \leqslant 80°C$	1	W
	$T_{tab} \leqslant 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUIT

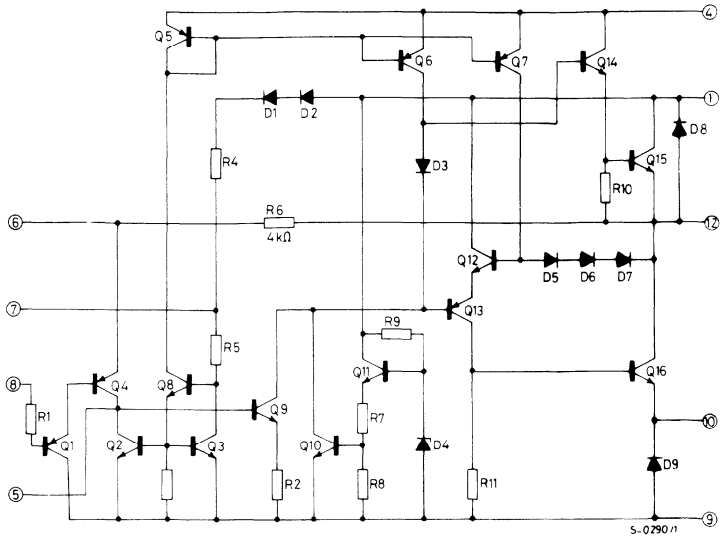


TBA810P

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 2)		6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Input bias current			0.4		μA
P_o	Output power	d = 10% f = 1KHz R_L = 4Ω R_L = 2Ω	 5.5 5.5	 6 7		 W W
$V_{i\,(rms)}$	Input saturation voltage		220			mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3dB)	R_L = 4Ω/2Ω C_3 = 820pF C_3 = 150pF		40 to 20,000 40 to 10,000		Hz Hz
d	Distortion	P_o = 50mW to 2.5W R_L = 4Ω/2Ω f = 1KHz		0.3		%
G_v	Voltage gain (open loop)	R_L = 4Ω f = 1KHz		80		dB
G_v	Voltage gain (closed loop)	R_L = 4Ω/2Ω f = 1KHz	34	37	40	dB
e_N	Input noise voltage	V_s = 16V B (-3dB) = 40 to 15,000Hz		2		μV
i_N	Input noise current			80		pA
η	Efficiency	P_o = 6W R_L = 4Ω f = 1KHz		75		%
SVR	Supply voltage rejection	R_L = 4Ω V_{ripple} = 1V_{rms} f_{ripple} = 10Hz	40	48		dB

Fig. 1 - Output power vs. supply voltage

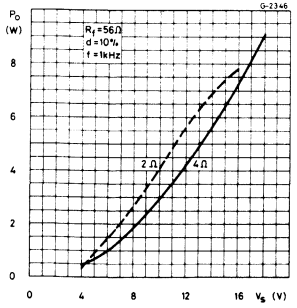


Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

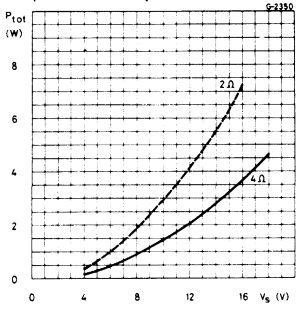
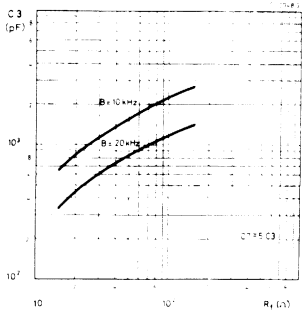


Fig. 3 - Value of C3 vs. feedback resistance for various values of B



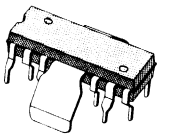
TBA810S

NOT FOR NEW DESIGN

7W AUDIO AMPLIFIER

The TBA810S is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.

The TBA810A provides 7W power output at 16V/4Ω, 6W at 14.4V/4Ω, 2.5W at 9V/4Ω, 1W at 6V/4Ω and works with a wide range of supply voltage (4 to 20V); it gives high output current (up to 2.5A), high efficiency (75%) at 6W output). very low harmonic and cross-over distortion. In addition, the circuit is provided with a thermal protection circuit.



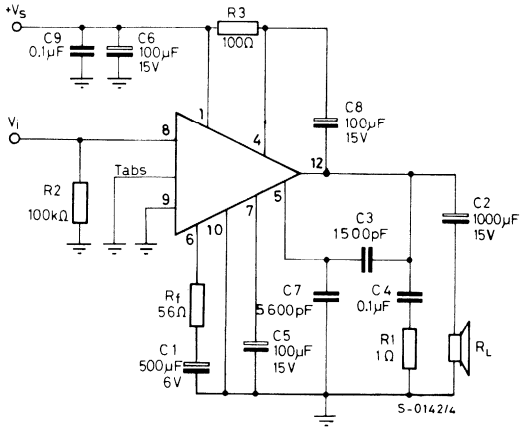
Findip

ORDERING NUMBER: TBA810S

ABSOLUTE MAXIMUM RATINGS

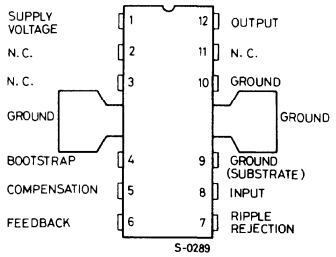
V_s	Supply voltage	20	V
I_o	Output peak current (non-repetitive)	3.5	A
I_o	Output current (repetitive)	2.5	A
P_{tot}	Power dissipation: at $T_{amb} \leqslant 70°C$	1	W
	at $T_{tab} \leqslant 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUIT

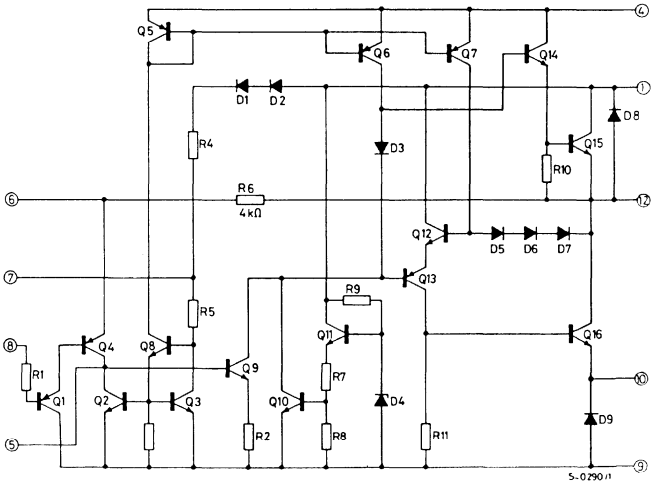


TBA810S

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70* °C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; T_{amb} = 25 °C)

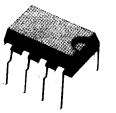
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)	V_s = 14.4V	6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Bias current (pin 8)			0.4		μA
P_o	Power output	d = 10% R_L = 4Ω f = 1 kHz V_s = 16V V_s = 14.4V V_s = 9V V_s = 6V	5.5	 7 6 2.5 1		 W W W W
$V_{i(rms)}$	Input voltage				220	mV
V_i	Input sensitivity	P_o = 6W V_s = 14.4V R_L = 4Ω f = 1kHz R_f = 56Ω R_f = 22Ω		 80 35		 mV mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3 dB)	V_s = 14.4V R_L = 4Ω C3 = 820 pF C3 = 1500 pF		40 to 20,000 40 to 10,000		 Hz Hz
d	Distorsion	P_o = 50mW to 3W V_s = 14.4V R_L = 4Ω f = 1kHz		 0.3		 %
G_v	Voltage gain (open loop)	V_s = 14.4V R_L = 4Ω f = 1kHz		 80		 dB
G_v	Voltage gain (closed loop)	V_s = 14.4V R_L = 4Ω f = 1kHz	34	 37	40	 dB
e_N	Input noise voltage	V_s = 14.4V R_g = 0 B (-3 dB) = 20Hz to 20,000 Hz		 2		 μV
i_N	Input noise current	V_s = 14.4V B (-3 dB) = 20 Hz to 20,000 Hz		 0.1		 nA
η	Efficiency	P_o = 5W V_s = 14.4V R_L = 4Ω f = 1kHz		 70		 %
SVR	Supply voltage rejection	V_s = 14.4V R_L = 4Ω f_{ripple} = 100 Hz		 38		 dB

TBA820M

MINIDIP 1.2W AUDIO AMPLIFIER

The TBA820M is a monolithic integrated audio amplifier in a 8 lead dual in-line plastic package. It is intended for use as low frequency class B power amplifier with wide range of supply voltage: 3 to 16V, in portable radios, cassette recorders and players etc. Main features are: minimum working supply voltage of 3V, low quiescent current, low number of external components, good ripple rejection, no cross-over distortion, low power dissipation.

Output power: P_o = 2W at 12V/8Ω, 1.6W at 9V/4Ω and 1.2W at 9V/8Ω.



Minidip Plastic

ORDERING NUMBER: TBA820M

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output peak current	1.5	A
P_{tot}	Power dissipation at T_{amb}= 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUITS

Fig. 1 - Circuit diagram with load connected to the supply voltage

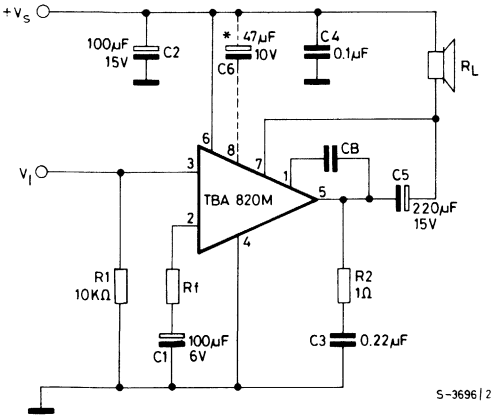
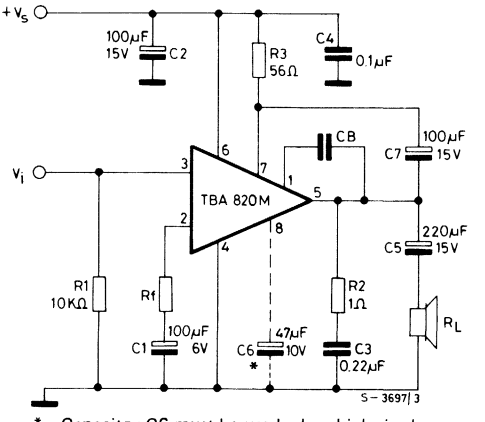


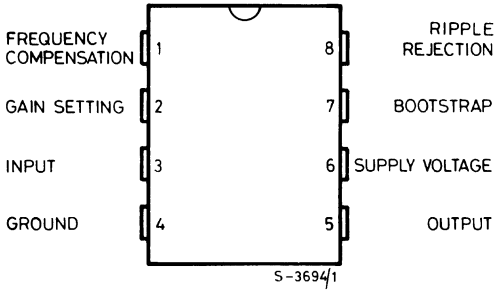
Fig. 2 - Circuit diagram with load connected to ground



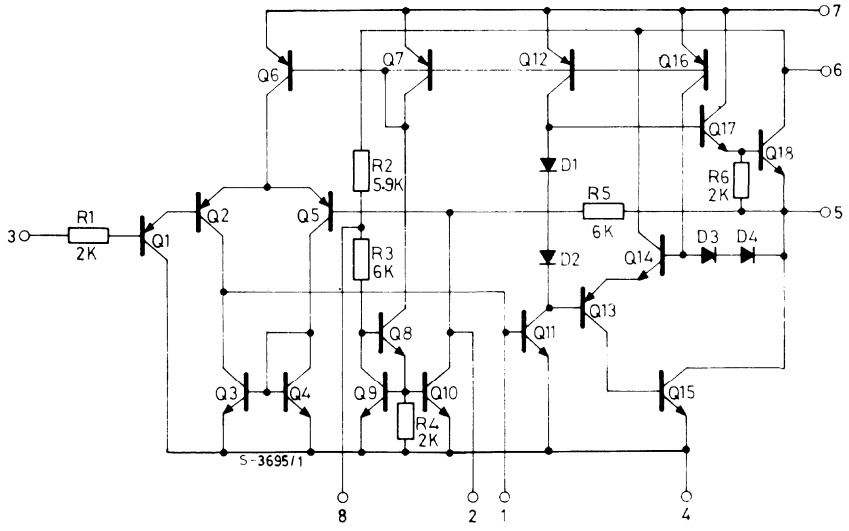
* Capacitor C6 must be used when high ripple rejection is requested.

CONNECTION DIAGRAM

(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits V_s= 9V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			3		16	V
V_o	Quiescent output voltage (pin 5)			4	4.5	5	V
I_d	Quiescent drain current				4	12	mA
I_b	Bias current (pin 3)				0.1		μA
P_o	Output power	d = 10% R_f= 120Ω V_s= 12V V_s= 9V V_s= 9V V_s= 6V V_s= 3.5V	f = 1 kHz R_L= 8Ω R_L= 4Ω R_L= 8Ω R_L= 4Ω R_L= 4Ω	0.9	 2 1.6 1.2 0.75 0.25		 W W W W W
R_i	Input resistance (pin 3)	f = 1 kHz			5		MΩ
B	Frequency response (-3 dB)	R_L= 8Ω C_5 = 1000 μF R_f= 120Ω	C_B= 680 pF C_B= 220 pF	25 to 7,000 25 to 20,000			Hz
d	Distortion	P_o= 500 mW R_L= 8Ω f = 1 kHz	R_f= 33Ω R_f= 120Ω		0.8 0.4		%
G_v	Voltage gain (open loop)	f = 1 kHz	R_L= 8Ω		75		dB
G_v	Voltage gain (closed loop)	R_L= 8Ω f = 1 kHz	R_f= 33Ω R_f= 120Ω		45 34		dB
e_N	Input noise voltage (*)				3		μV
i_N	Input noise current (*)				0.4		nA
$\frac{S+N}{N}$	Signal to noise ratio (*)	P_o= 1.2W R_L= 8Ω G_v= 34 dB	R1= 10KΩ R1= 50 kΩ		80 70		dB
SVR	Supply voltage rejection (test circuit of fig. 2)	R_L= 8Ω $f_{(ripple)}$ = 100 Hz C6= 47 μF R_f= 120Ω			42		dB

(*) B = 22 Hz to 22 KHz

Fig. 3 - Output power vs. supply voltage

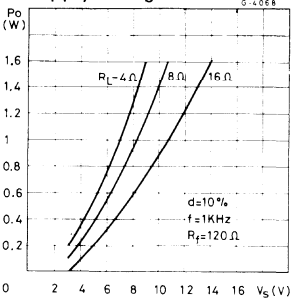


Fig. 4 - Harmonic distortion vs. output power

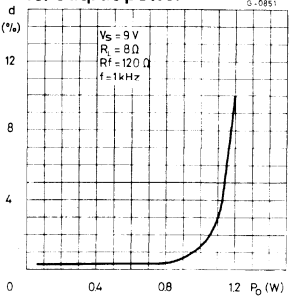


Fig. 5 - Power dissipation and efficiency vs. output power

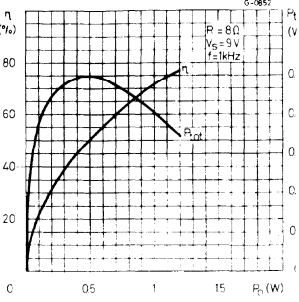


Fig. 6 - Maximum power dissipation (sine wave operation)

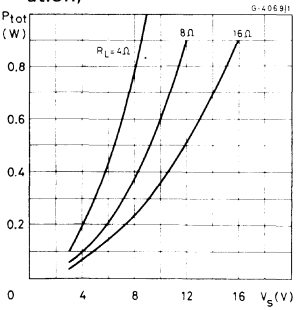


Fig. 7 - Suggested value of C_B vs. R_f

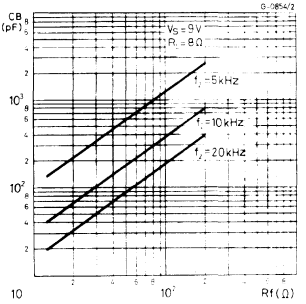


Fig. 8 - Frequency response

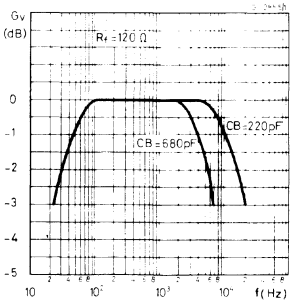


Fig. 9 - Harmonic distortion vs. frequency

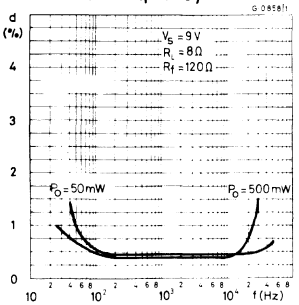


Fig. 10 - Supply voltage rejection (Fig. 2 circuit)

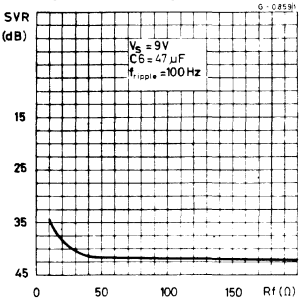
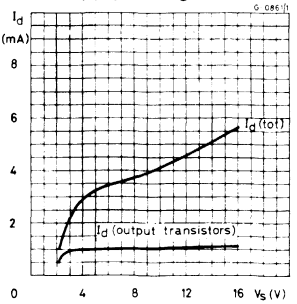


Fig. 11 - Quiescent current vs. supply voltage



TCA3089

NOT FOR NEW DESIGN

FM-IF RADIO SYSTEM

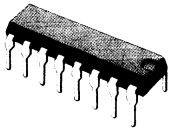
- HIGH LIMITING SENSITIVITY
- HIGH AMR
- HIGH RECOVERED AUDIO
- GOOD CAPTURE RATIO
- LOW DISTORTION
- MUTING CAPABILITY

The TCA3089 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It provides a complete subsystem for amplification of FM signals.

The functions incorporated are:

– FM amplification and detection
– Interchannel controlled muting
– AFC and delayed AGC for FM tuner
– Switching of stereo decoder
– Driver of a field strength meter

The TCA3089 can be used for FM-IF amplifier application in Hi-Fi, car-radios and communication receivers.



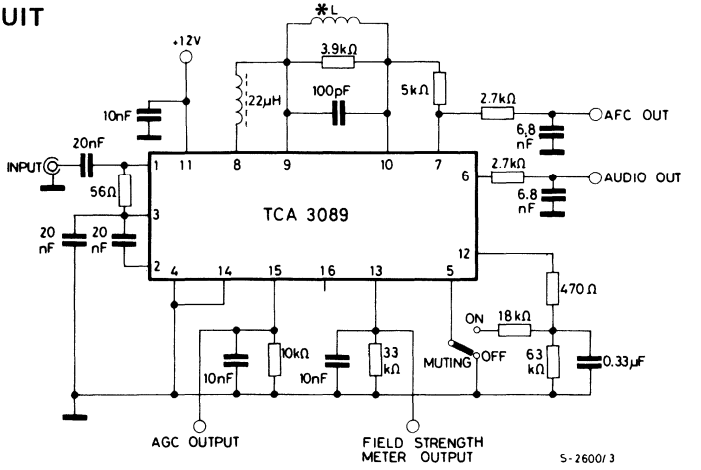
DIP-16 Plastic
(0.25)

ORDERING NUMBER: TCA3089

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output current (from pin 15)	2	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	-25 to 70	°C

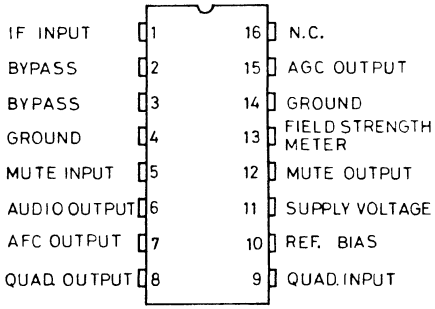
TEST CIRCUIT



*L tunes with 100pF at 10.7 MHz (Q_o=75)

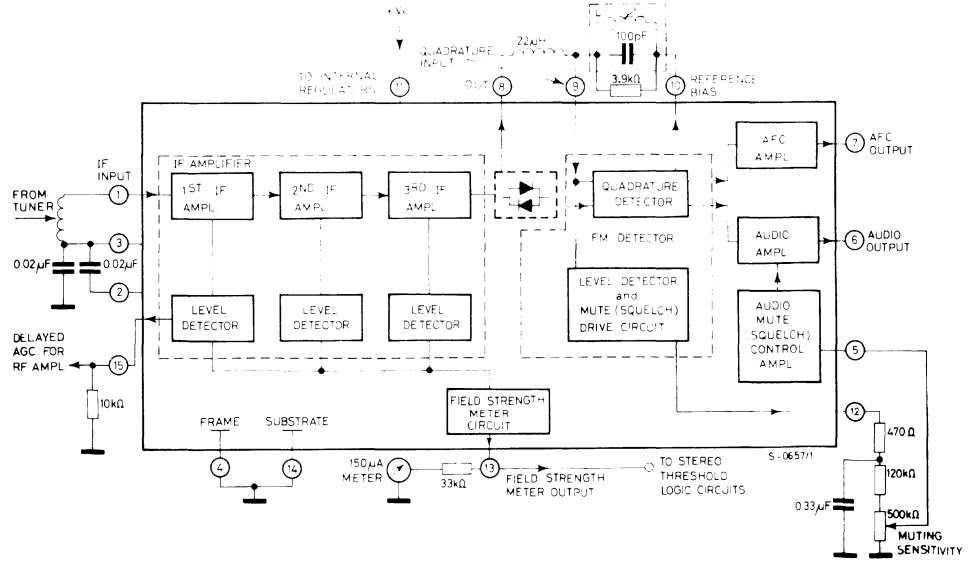
TCA3089

CONNECTION DIAGRAM
(top view)



S-0398/1

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit; V_s= 12V, f_o = 10.7 MHz, V_5= 0V, T_{amb}= 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
I_s	Supply current		16	23	30	mA
V_i	Voltage at the IF amplifier input		1.2	1.9	2.4	V
V_2, V_3	Voltage at the input bypassing		1.2	1.9	2.4	V
V_6	Voltage at the audio output		5	5.6	6	V
V_{10}	Reference bias voltage		5	5.6	6	V
AC CHARACTERISTICS						
$V_{i(threshold)}$	Input limiting voltage (-3 dB) at pin 1	f_m= 1 kHz Δf= ± 75 kHz		12	25	μV
V_o	Recovered audio voltage (pin 6)	$V_i \geq 100\ \mu V$ f_m= 1 kHz Δf= ± 75 kHz	300	400	500	mV
V_7	Recovered audio voltage (pin 7)		200	350	500	mV
d	Distortion	$V_i \geq 1$ mV f_m= 1 kHz Δf= ± 75 kHz		0.5	1	%
$\frac{S+N}{N}$	Signal to noise ratio		60	67		dB
AMR	Amplitude modulation rejection	V_i = 100 mV f_m= 1 kHz Δf = ± 75 kHz m = 0.3	45	55		dB
V_i	Input voltage for delayed AGC action (pin 1)			10		mV
V_{15}	AGC output	V_i = 100 mV			0.5	V
$\frac{\Delta I_7}{\delta f}$	AFC control slope (note 1)	V_i = 10 mV		1.2		$\frac{\mu A}{kHz}$
V_{13}	Field strength meter output sensitivity	V_i = 0.5 mV		1.5		V
	No signal mute (note 2)	muting: ON	55			dB

Note: 1) $\Delta I_7 = \frac{\Delta V_{7,10}}{R_{7,10}}$

2) No signal mute = $20 \log \frac{V_o @ V_i \geq 100\ \mu V}{V_o @ V_i = 0}$

Fig. 1 - Relative recovered audio and noise output vs. input voltage

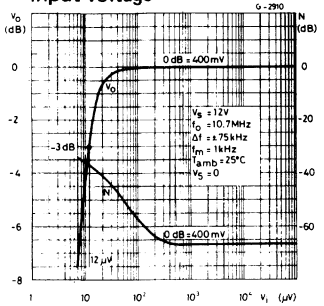


Fig. 2 - Capture ratio vs. input voltage

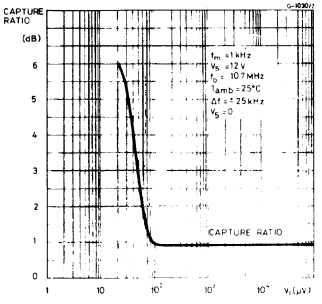


Fig. 3 - AGC (V_{15}) and field strength meter output (V_{13}) vs. input voltage

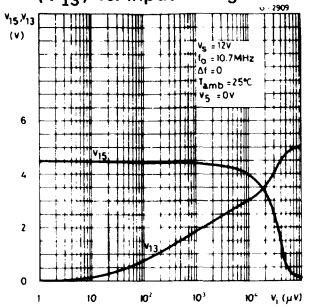


Fig. 4 - AFC output current vs. change in tuning frequency

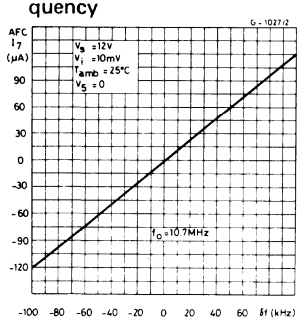


Fig. 5 - Amplitude modulation rejection vs. input voltage

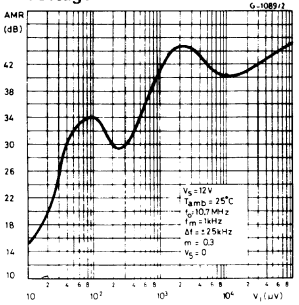
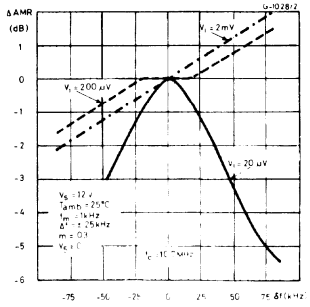


Fig. 6 - AMR vs. change in tuning frequency

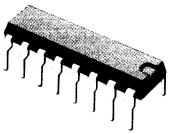


TCA3189

FM-IF HIGH QUALITY RADIO SYSTEM

- EXCEPTIONAL LIMITING SENSITIVITY
- VERY LOW DISTORTION (0.1% - DOUBLE TUNED DETECTOR COIL)
- IMPROVED S/N RATIO
- EXTERNALLY PROGRAMMABLE AUDIO LEVEL
- ON CHANNEL STEP FOR SEARCH CONTROL
- PROGRAMMABLE AGC VOLTAGE AND AFC FOR TUNER
- INTERCHANNEL MUTING (SQUELCH)
- DEVIATION MUTING
- DIRECT DRIVE OF TUNING METER
- DIRECT DRIVE OF FIELD STRENGTH METER

The TCA3189 is a monolithic integrated circuit in a 16-lead dual in-line plastic package, which provides a **complete subsystem** for amplification of 10.7MHz FM signal in Hi-Fi, car-radios and communications receivers.



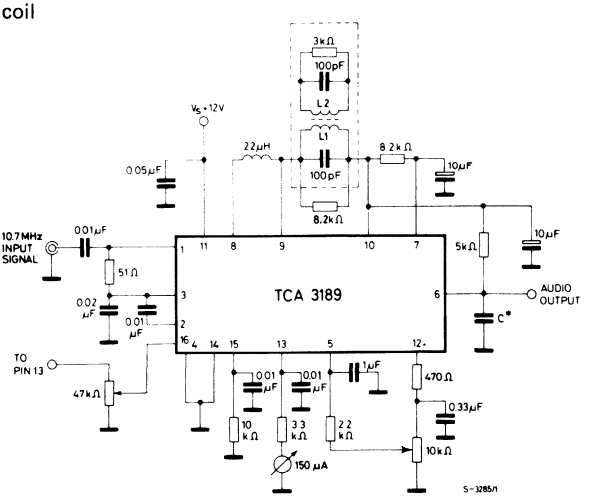
DIP-16 Plastic
(0.25)

ORDERING NUMBER: TCA3189

ABSOLUTE MAXIMUM RATINGS

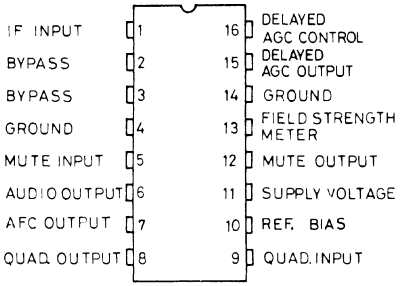
V_s	Supply voltage	16	V
I_o	Output current (from pin 15)	2	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	-25 to 85	°C

Double tuned detector coil



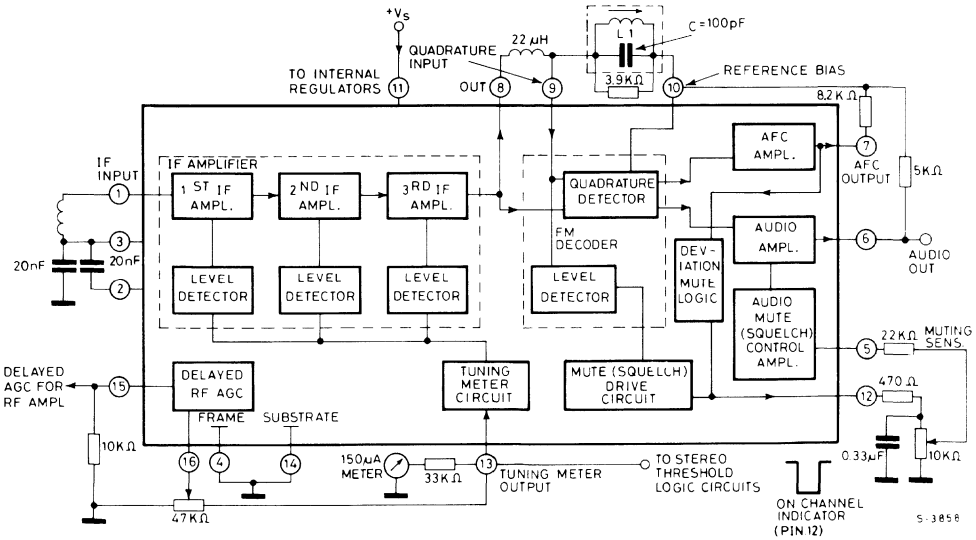
TCA3189

CONNECTION DIAGRAM
(top view)



S-3286

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s = 12V, T_{amb} = 25°C)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage range	No signal input, non muted		9		16	V
I_s	Supply current			20	31	44	mA
V_1	Voltage at the IF amplifier input			1.2	1.9	2.4	V
V_2, V_3	Voltage at the input bypass			1.2.	1.9	2.4	V
V_{15}	Voltage at the pin 15 (RF AGC)			7.5	9.5	11	V
V_{10}	Reference bias voltage			5	5.6	6	V
V_i	Input limiting voltage (-3 dB) at pin 1	f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz			12	25	μV
V_o	Recovered audio voltage (pin 6)	$V_i \geqslant 50\ \mu V$ f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz		325	500	650	mV
d	Distortion (single tuned)	$V_i \geqslant 1$ mV f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz			0.5	1	%
d	Distortion (double tuned)				0.1		%
$\frac{S+N}{N}$	Signal to noise ratio			65	72		dB
AMR	Amplitude modulation rejection	V_i = 100 mV f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz AM mod. 30%		45	55		dB
V_{16}	RF AGC threshold				1.25		V
$\frac{\Delta I_7}{\Delta f}$	AFC control slope				1.9		$\frac{\mu A}{KHz}$
V_{12}	On channel step (deviation mute)	V_i = 100 mV	$f_{DEV.} <$ ± 40 KHz		0		V
		f_o = 10.7 MHz	$f_{DEV.} >$ ± 40 KHz		5.6		V

TEST CIRCUIT

Fig. 1 - Single tuned detector coil

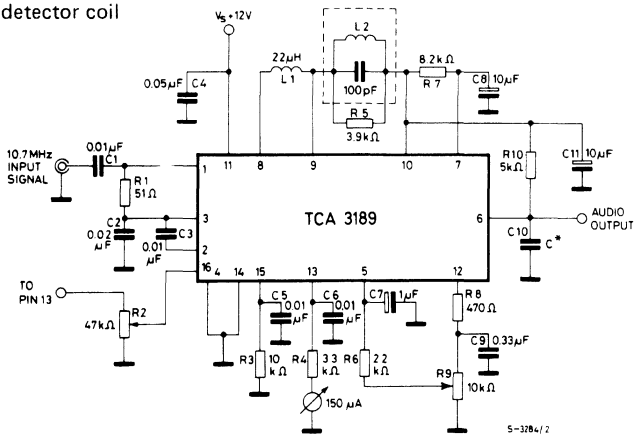


Fig. 2 - Limiting and noise characteristics

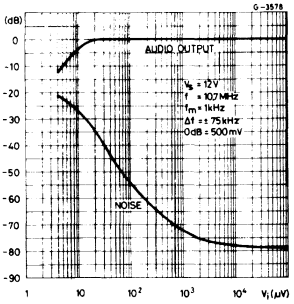


Fig. 3 - Deviation mute threshold vs. R_{7-10}

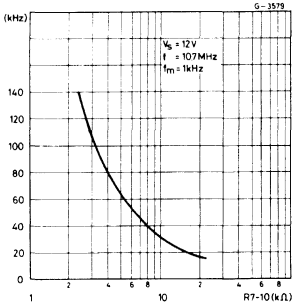


Fig. 4 - Recovered audio and muting action vs. input level

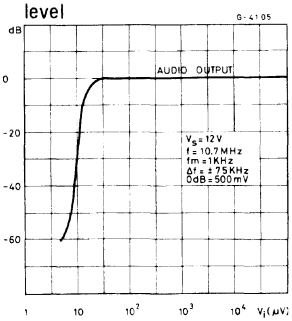


Fig. 5 - AFC characteristics

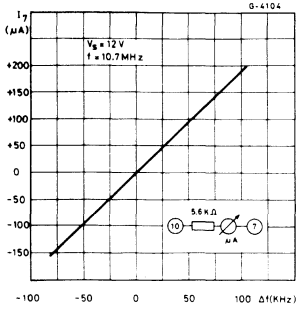


Fig. 6 - AGC voltage for FM tuner vs. input level

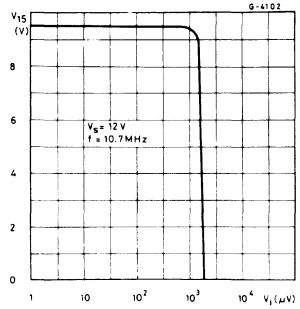
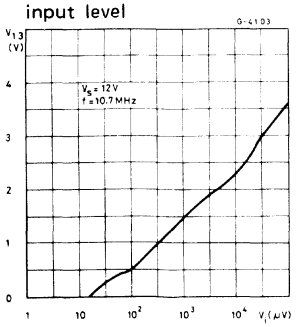


Fig. 7 - Field strength and tuning meter output vs. input level

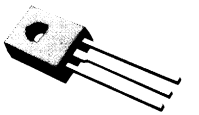


TDA1151

MOTOR SPEED REGULATOR

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (UP TO 800mA)
- LOW QUIESCENT CURRENT (1.7mA)
- LOW REFERENCE VOLTAGE (1.2V)
- EXCELLENT PARAMETERS STABILITY VERSUS TEMPERATURE

The TDA1151 is a monolithic integrated circuit in SOT-32 plastic package. It is intended for use as speed regulator for DC motors of record players, tape and cassette recorders, movie cameras, toys etc.



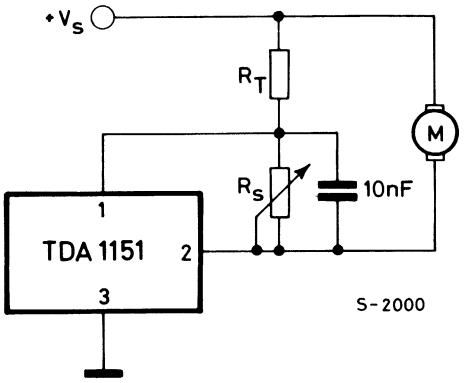
SOT-32

ORDERING NUMBER: TDA1151

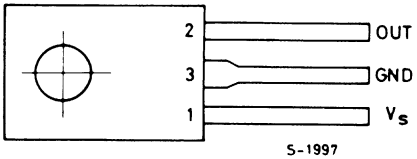
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 70°C	0.8	W
	at T_{case} = 100°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT

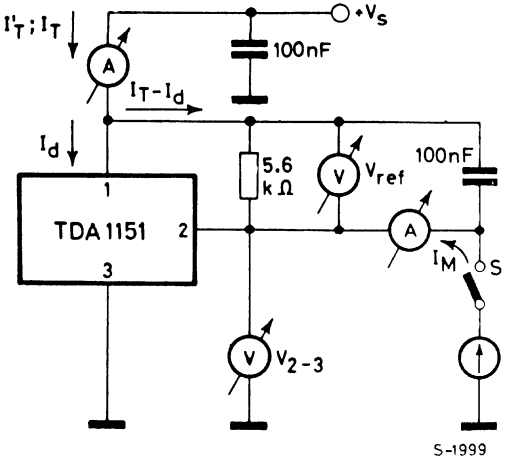


CONNECTION DIAGRAM



tab connected to pin 3

TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage (between pins 1 and 2)	V_s = 6V I_M= 0.1A	1.1	1.2	1.3	V
I_d	Quiescent drain current	V_s = 6V I_M= 100 μA		1.7		mA
I_{MS}	Starting current	V_s = 5V $\Delta V_{ref}/V_{ref}$= -50%	0.8			A
V_{1-3}	Minimum supply voltage	I_M= 0.1A $\Delta V_{ref}/V_{ref}$= -5%			2.5	V
$K=I_M/I'_T$	Reflection coefficient	V_s = 6V I_M= 0.1A	18	20	22	–
$\frac{\Delta K}{K}/\Delta V_s$		V_s = 6V to 18V I_M= 0.1A		0.45		%/V
$\frac{\Delta K}{K}/\Delta I_M$		V_s = 6V I_M= 25 to 400 mA		0.005		%/mA
$\frac{\Delta K}{K}/\Delta T$		V_s = 6V I_M= 0.1A T_{amb}= -20 to 70°C		0.02		%/°C
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$	Line regulation	V_s = 6V to 18V I_M= 0.1A		0.02		%/V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$	Load regulation	V_s = 6V I_M= 25 to 400 mA		0.009		%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$	Temperature coefficient	V_s = 6V I_M= 0.1A T_{amb}= -20 to 70°C		0.02		%/°C

Fig. 1 - Quiescent drain current vs. power supply

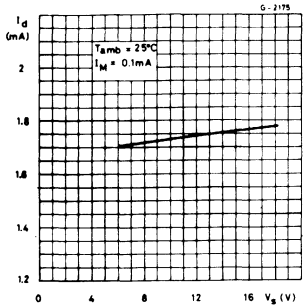


Fig. 2 - Quiescent drain current vs. ambient temperature

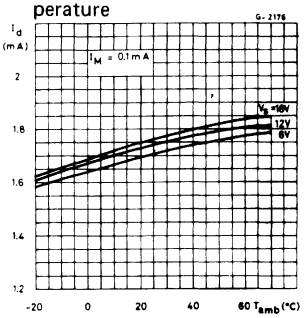


Fig. 3 - Reference voltage vs. supply voltage

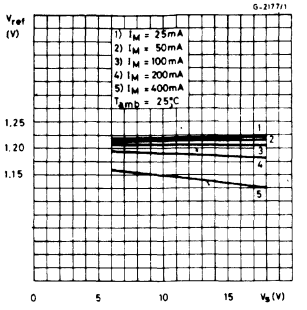


Fig. 4 - Reference voltage vs. motor current

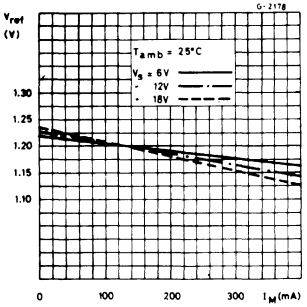


Fig. 5 - Reference voltage vs. ambient temperature

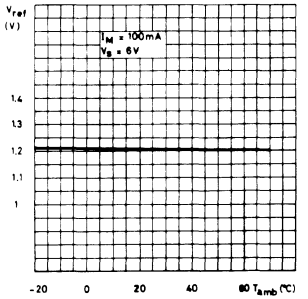


Fig. 6 - Reflection coefficient vs. supply voltage

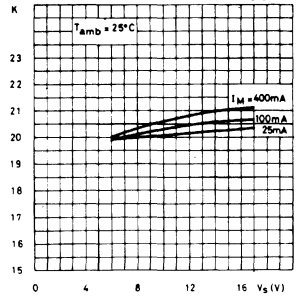


Fig. 7 - Reflection coefficient vs. motor current

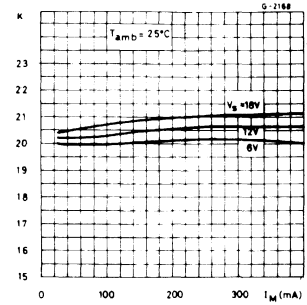


Fig. 8 - Reflection coefficient vs. ambient temperature

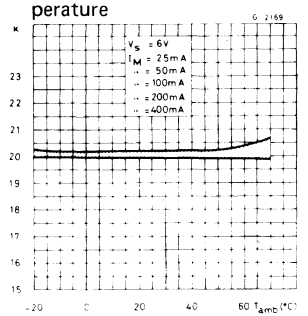


Fig. 9 - Typical minimum supply voltage vs. motor current

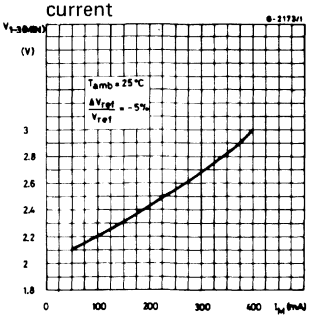
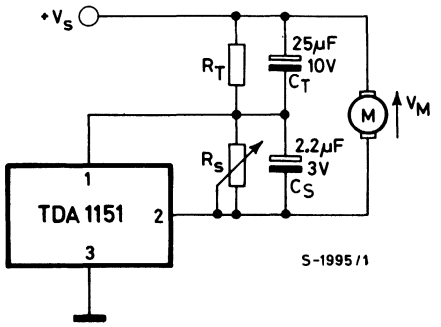


Fig. 10 - Application circuit



V_s = +9V
R_M = 14.2Ω
R_T = 280Ω
R_S = 1 kΩ
E_g = 2.9V
I_M = 150 mA
$V_M = R_M \cdot I_M + E_g = 5.03V$

Note: A ceramic capacitor of 10 nF between pins, 1 and 2 improves stability in some applications.

Fig. 11 - P.C. board and component layout of the circuit of Fig. 10 (1 : 1 scale)

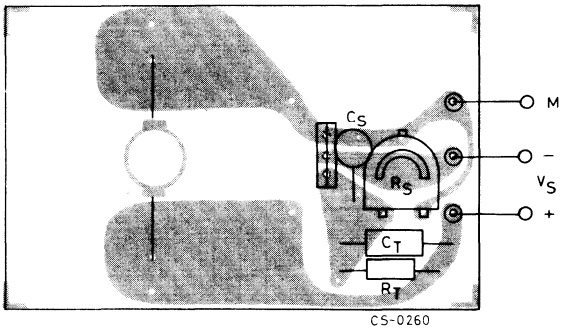


Fig. 12 - Speed variation vs. supply voltage

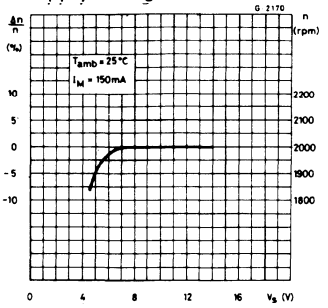


Fig. 13 - Speed variation vs. motor current

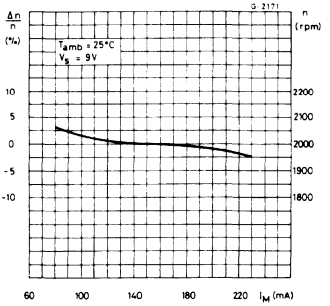


Fig. 14 - Speed variation vs. ambient temperature

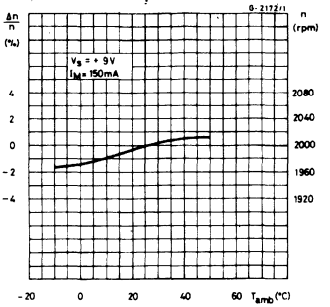
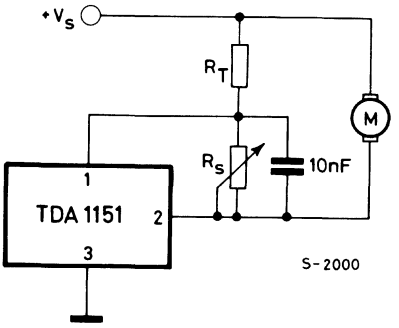


Fig. 15 - Low cost application circuit



V_S = +12V
R_M = 14.7Ω
R_T = 290Ω
R_S = 1 kΩ
E_g = 2.65V
I_M = 110 mA

Fig. 16 - Speed variation vs. supply voltage

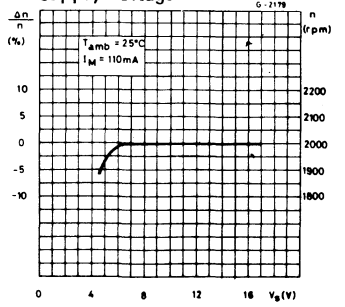


Fig. 17 - Speed variation vs. motor current

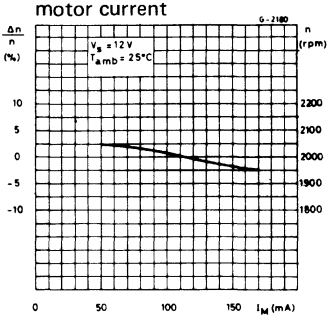
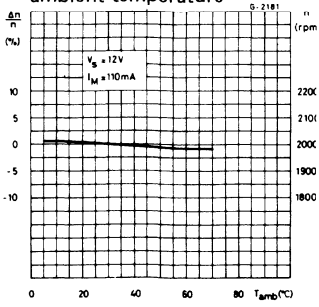


Fig. 18 - Speed variation vs. ambient temperature



TDA1220B

AM-FM QUALITY RADIO

The TDA1220B is a monolithic integrated circuit in a 16-lead dual in-line package designed as an improved version of the TDA1220A.

It is intended for quality receivers produced in large quantities.

The functions incorporated are:

AM SECTION

- Preamplifier and double balanced mixer
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

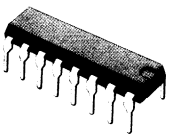
FM SECTION

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA1220B is suitable up to 30MHz AM and for FM bands (including 450KHz narrow band) and features:

- Very constant characteristics (3V to 16V)
- High sensitivity and low noise
- Very low tweet
- Very high signal handling (1V)
- Sensitivity regulation facility (*)
- High recovered audio signal suited for stereo decoders and radio recorders
- Very simple DC switching of AM-FM
- Low current drain
- AFC facility

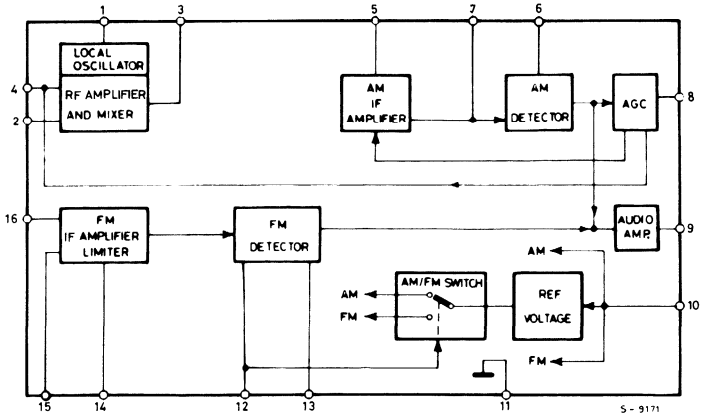
(*) Maximum AM sensitivity can be reduced by means of a resistor (5 to 12KΩ) between pin 4 and ground.



DIP-16 Plastic
(0.25)

ORDERING NUMBER: TDA1220BK

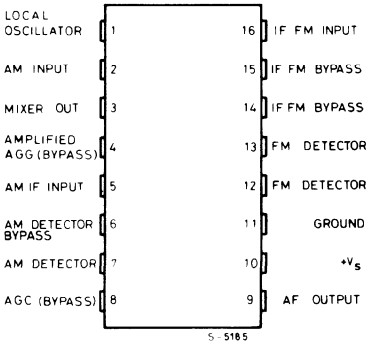
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 9V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ	Max	Unit
V_s	Supply voltage			3		16	V
I_d	Drain current	FM			10	15	mA
		AM			14	20	mA
AM SECTION (f_o = 1 MHz; f_m = KHz)							
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		12	25	μV
S/N		V_i = 10 mV	m = 0.3	45	52		dB
V_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	94	100		dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	80	130	190	mV
d	Distortion	V_i = 1 mV	m = 0.3		0.4	1	%
			m = 0.8		1.2		%
V_H	Max input signal handling capability	m = 0.8	d < 10%	1			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)			4.5	7	9.5	KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB
FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)							
V_i	Input limiting voltage	-3 dB limiting point			22	36	μV
AMR	Amplitude modulation rejection	$\Delta f = \pm 22.5$ KHz V_i = 3 mV	m = 0.3	40	50		dB
S/N	Ultimate quieting	$\Delta f = \pm 22.5$ KHz	V_i = 1 mV	55	65		dB
d	Distortion	$\Delta f = \pm 75$ KHz	V_i = 1 mV		0.7	1.5	%
d	Distortion	$\Delta f = \pm 22.5$ KHz	V_i = 1 mV		0.25	0.5	%
d	Distortion (double tuned)				0.1		%
V_o	Recovered audio signal (pin 9)	$\Delta f = \pm 22.5$ KHz	V_i = 1 mV	80	110	140	mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)			4.5	7	9.5	KΩ

Fig. 1 - Test circuit

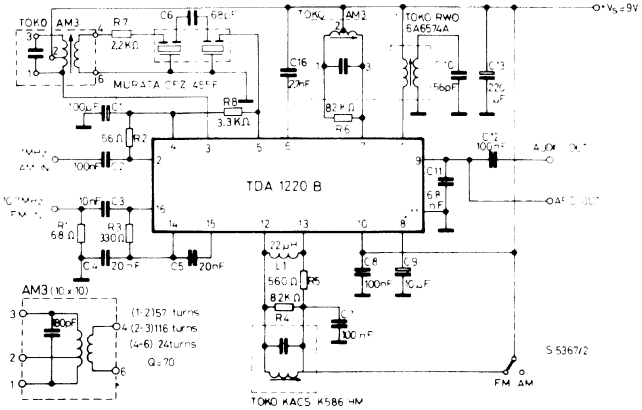


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.

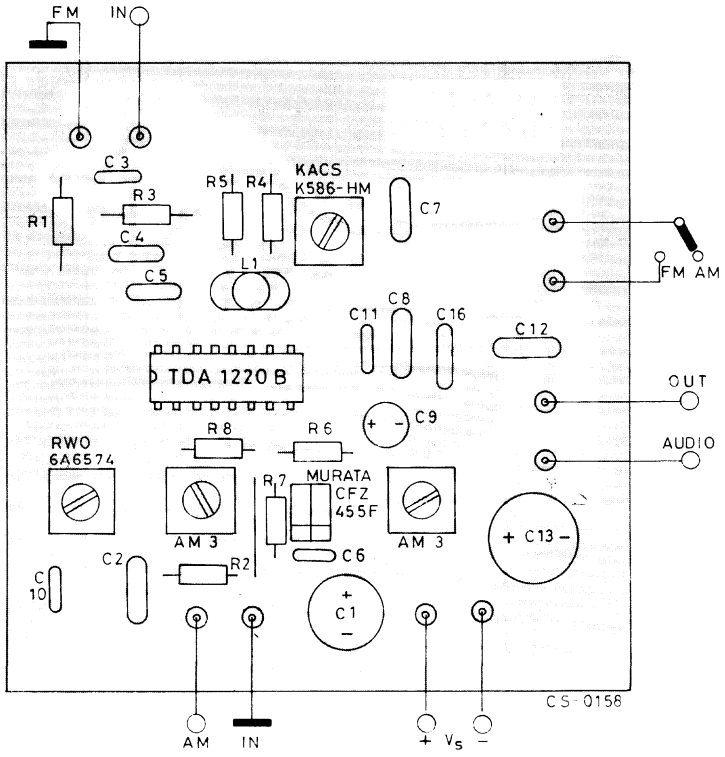


Fig. 3 - Audio output, noise and tweet levels vs. input signal (AM section)

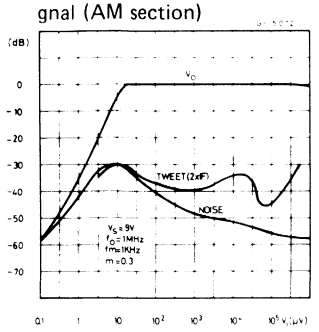


Fig. 4 - Distortion vs input signal and modulation index (AM section)

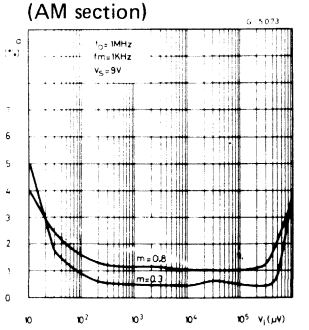


Fig. 5 - Audio output vs. supply voltage (AM section)

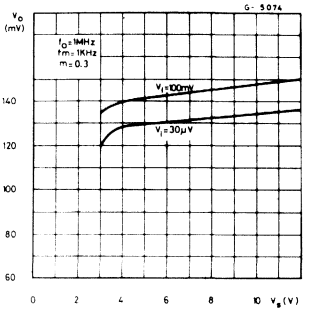


Fig. 6 - Audio output and noise level vs. input signal (FM section)

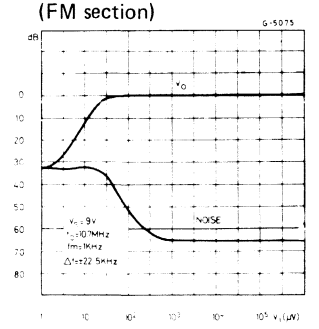


Fig. 7 - Distortion vs. input signal (FM section)

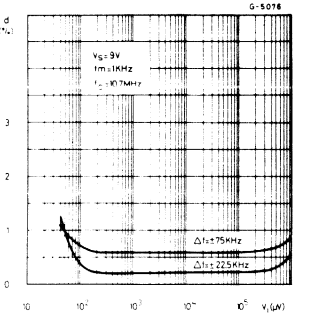


Fig. 8 - Audio output vs. supply voltage (FM section)

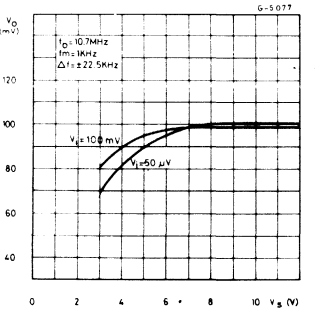


Fig. 9 - Amplitude modulation rejection vs. input signal (FM section)

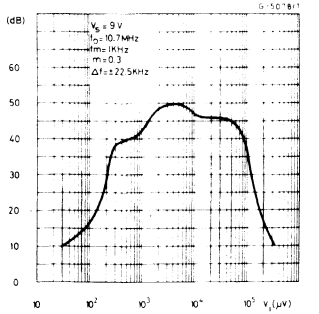


Fig. 10 - ΔDC output voltage (pin. 9) vs. frequency shift (FM section)

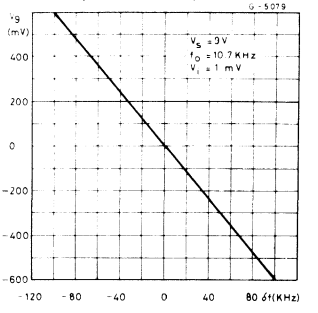
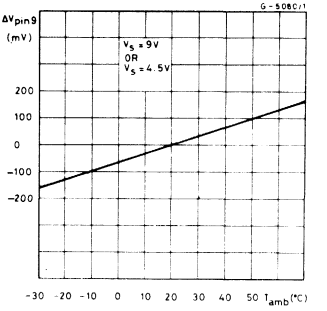


Fig. 11 - ΔDC output voltage (pin 9) vs. ambient tempetature (FM section)



APPLICATION INFORMATION

AM Section

RF Amplifier and mixer stages

The RF amplifier stage (pin 2) is connected directly to the secondary winding of the ferrite rod antenna or input tuned circuit. Bias is provided at pin 4 which must be adequately decoupled. The RF amplifier provides stable performance extending beyond 30 MHz.
The Mixer employed is a double - balanced multiplier and the IF output at pin 3 is connected directly to the IF filter coil.

Local oscillator

The local oscillator is a cross coupled differential stage which oscillates at the frequency determined by the load on pin 1.
The oscillator resonant circuit is transformer coupled to pin 1 to improve the **Q** factor and frequency stability.
The oscillator level at pin 1 is about 100 mV rms and the performance extends beyond 30 MHz, however to enhance the stability and reduce to a minimum pulling effects of the AGC operation or supply voltage variations, a high C/L ratio should be used above 10 MHz.
An external oscillator can be injected at pin 1. The level should be 50 mV rms and pin 1 should be connected to the supply via a 100Ω resistor.

IF Amplifier Detector

The IF amplifier is a wide band amplifier with a tuned output stage.
The IF filters can be either LC or mixed LC/ceramic.
AM detection occurs at pin 7. A detection capacitor is connected to pin 6 to reduce the radiation of spurious detector products.
The Audio output is at pin 9 (for either AM or FM); the IF frequency is filtered by an external capacitor which is also used as the FM mono de-enphasis network. The audio output impedance is about 7KΩ and a high impedance load (~ 50KΩ) must be used.

AGC

Automatic gain control operates in two ways.
With weak signals it acts on the IF gain, maintaining the maximum S/N. For strong signals a second circuit intervenes which controls the entire chain and allows signal handling in excess of one volt (m = 0.8).
At pin 8 there is a carrier envelope signal which is filtered by an external capacitor to remove the Audio and RF content and obtain a mean DC signal to drive the AGC circuit.

APPLICATION INFORMATION (continued)

FM Section

IF Amplifier and limiter

The 10.7 MHz IF signal from the ceramic filter is amplified and limited by a chain of four differential stages.
Pin 16 is the amplifier input and has a typical input impedance of 6.5 KΩ in parallel with 14 pF at 10.7 MHz.
Bias for the first stage is available at pin 14 and provides 100% DC feedback for stable operating conditions. Pin 15 is the second input to the amplifier and is decoupled to pin 14, which is grounded by a 20 nF capacitor.
An RLC network is connected to the amplifier output and gives a 90° phase shift (at the IF centre frequency) between pins 13 and 12. The signal level at pin 13 is about 150 mV rms.

FM Detector

The circuit uses a quadrature detector and the choise of component values is determined by the acceptable level of distortion at a given recovered audio level.
With a double tuned network the linearity improves (distortion is reduced) and the phase shift can be optimized; however this leads to a reduction in the level of the recovered audio. A satisfactory compromise for most FM receiver applications is shown in the test circuit.

Care should be taken with the physical layout.
The main recommandations are:

- Locate the phase shift coil as near as possible to pin 13.
- Shunt pins 14 and 16 with a low value resistor (between 56Ω and 330Ω).
- Ground the decoupling capacitor of pin 14 and the 10.7 MHz input filter at the same point.

AM-FM Switching

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

Typical DC voltages (refer to the test circuit)

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Unit
AM	9	1.4	9	1.4	1.4	8.4	9	0.7	1.9	9	0	0.1	0.1	8.5	8.5	8.5	V
FM	9	0.02	9	0.02	0.02	8.5	9	0	1.7	9	0	9	9	8	8	8	V

APPLICATION SUGGESTION

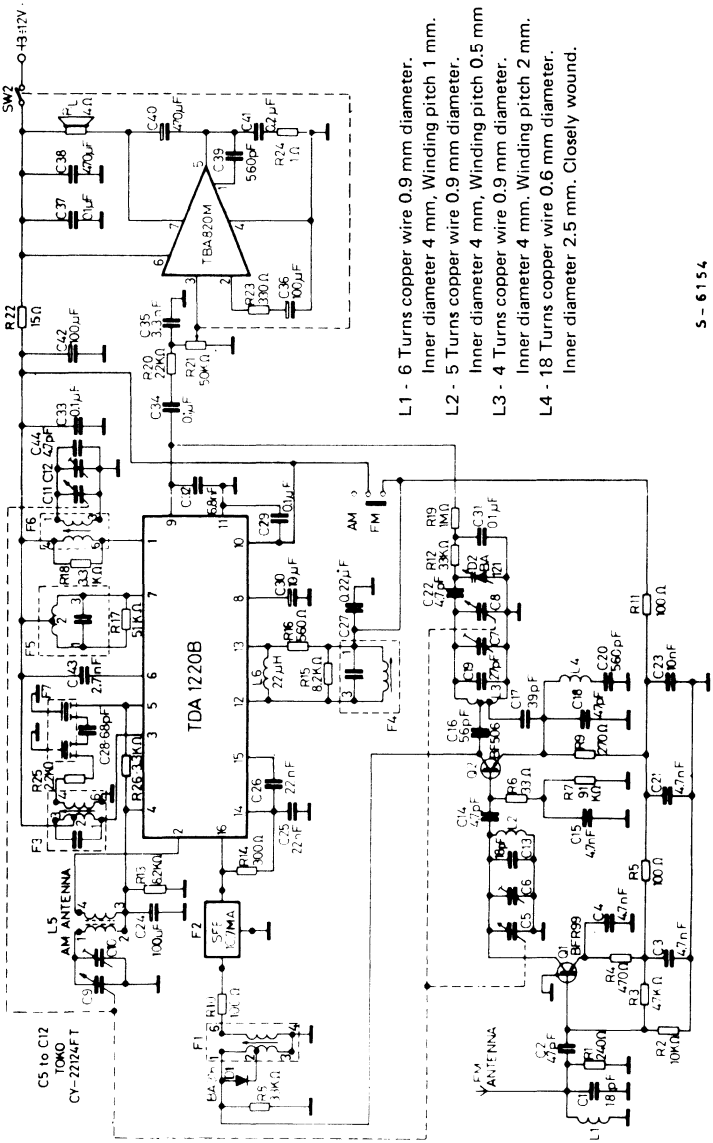
Reccomended values are referred to the test circuit of Fig. 2

Part number	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C1	100 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C2 (*)	100 nF	AM input DC cut		
C3 (*)	10 nF	FM input DC cut		
C4 C5	20 nF 20 nF	FM amplifier bypass	Reduction of sensitivity	– Bandwidth increase – Higher noise
C6	68 pF	Ceramic filter coupling	IF bandwidth reduction	IF bandwidth increase
C7	100 nF	FM detector decoupling	Danger of RF irradiation	
C8	100 nF	Power supply bypass	Noise increase of the audio output	
C9	10 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C10 (*)	56 pF	Tuning of the AM oscillator at 1455 KHz		
C11	6.8 nF	50 μs FM de-enphasis		
C12	100 nF	Output DC decoupling	Low audio frequency cut	
C13	220 μF	Power supply decoupling	Increase of the distortion at low frequency	
C16	2.7 nF	AM detector capacitor	Low suppression of the IF frequency and harmonics	Increase of the audio distortion
R1 (*)	68 ohm	FM input matching		
R2 (*)	56 ohm	AM input matching		
R3	330 ohm	Ceramic filter matching		
R4	8.2 Kohm	FM detector coil Q setting	Audio output decrease and lower distortion	Audio output increase and higher distortion
R5	560 ohm	FM detector load resistor	Audio output decrease and higher AMR	
R6	82 Kohm	AM detector coil Q setting	Lower IF gain and Lower AGC range	Higher IF gain and lower AGC range
R7	2.2 Kohm	455 KHz IF filter matching		
R8	3.3 Kohm	455 KHz IF filter matching		

(*) Only for test circuit

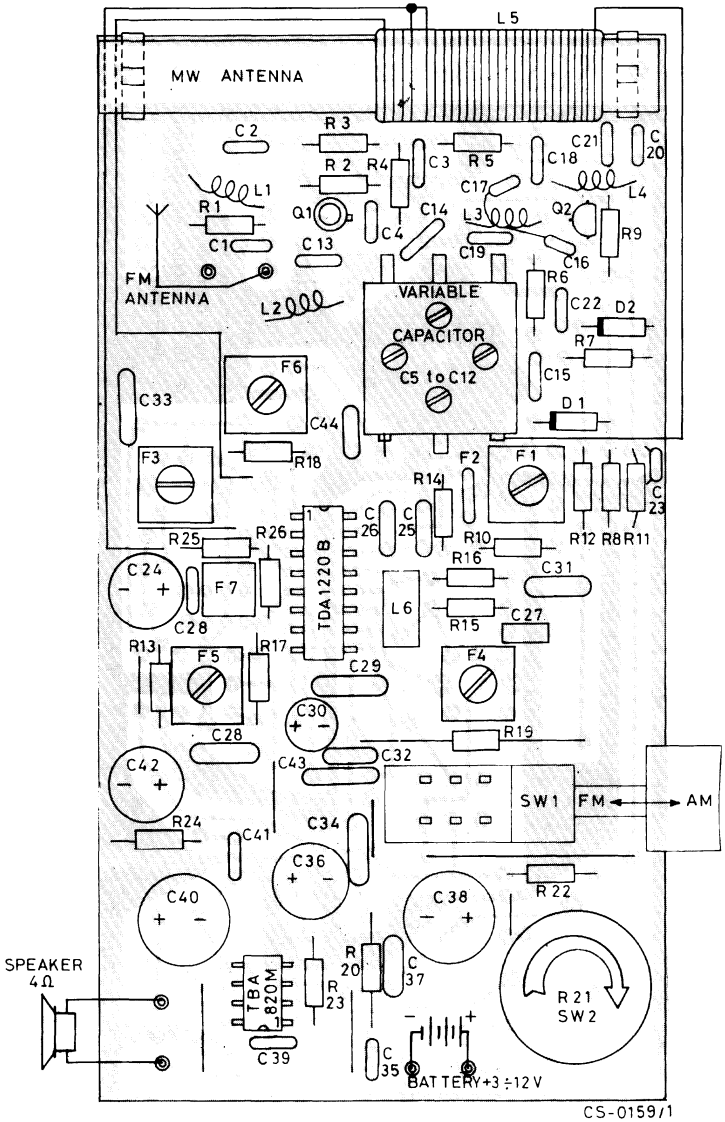
APPLICATION INFORMATION (continued)

Fig. 12 - Portable AM/FM radio



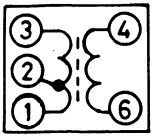
APPLICATION INFORMATION (continued)

Fig. 13 - PC board and component layout of the fig. 12 1:1 scale



APPLICATION INFORMATION (continued)

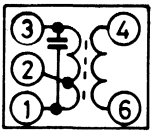
F1 – 10.7 MHz IF Coil



C_o (pF)	f (MHz)	Q_o	TURNS		
–		1-3	1-2	2-3	4-6
–	10.7	110	6	8	2

TOKO - FM1 - 10x10 mm.
154 AN - 7A5965R

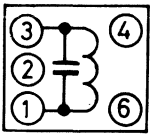
F3 and F5 - 455 KHz IF Coil



C_o (pF)	f (kHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	57	116	24

TOKO - AM3 - 10x10 mm.
RLC - 4A7525N

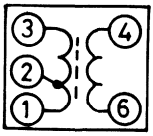
F4 – FM Detector Coil



C_o (pF)	f (MHz)	Q_o	TURNS		
1-3		1-3	1-3	–	–
82	10.7	100	12	–	–

TOKO - 10x10 mm.
KACS - K586 HM

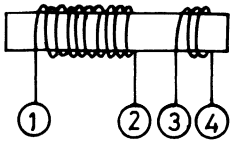
F6 – AM Oscillator Coil



f (kHz)	L (μH)	Q_o	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	220	80	2	75	8

TOKO -10x10 mm
RWO + 6A6574N

L5 – Antenna Coil



S-6161

f (KHz)	L (μH)	Q_o	TURNS	
	1-2	1-2	1-2	3-4
796			105	7

WIRE: LITZ - 15x0.05 mm.
CORE: 10x80 mm.

APPLICATION INFORMATION (continued)

Typical performance of the radio receiver of fig.12 (V_s = 9V)

Parameter		Test Conditions		Value
WAVEBANDS	FM			87.5 to 108 MHz
	AM			510 to 1620 KHz
SENSITIVITY	FM	S/N = 26dB	Δf = 22.5KHz	1 μV
	AM	S/N = 6dB	m = 0.3	1 μV
	AM	S/N = 26dB	m = 0.3	10 μV
DISTORTION (fm = 1KHz)	FM	P_o = 0.5W	Δf = 22.5KHz	0.25%
			Δf = 75KHz	0,7%
	AM	V_i = 100 μV	m = 0.3	0.4%
			m = 0,8	0,8%
SIGNAL TO NOISE (fm = 1KHz)	FM	P_o = 0.5W V_i = 100 μV	Δf = 22.5KHz	64 dB
	AM	P_o = 0.5W V_i = 1 mV	m = 0.3	50dB
AMPLITUDE MODULATION REJECTION	FM	V_i = 100 μV	Δf = 22.5KHz m = 0.3	50dB
TWEET	2nd H.	f = 911 KHz		0.3%
	3rd H.	f = 1370 KHz		0.07%
QUIESCENT CURRENT				20mA
SUPPLY VOLTAGE RANGE				3 to 12V

APPLICATION INFORMATION (continued)

Fig. 14 - Low cost 27 MHz receiver

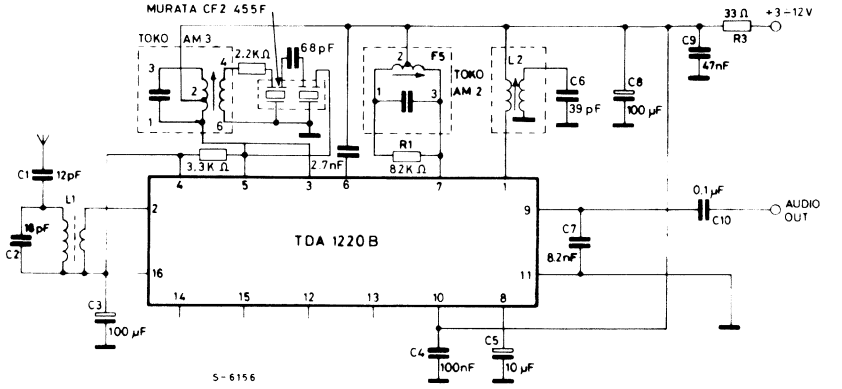
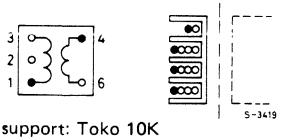
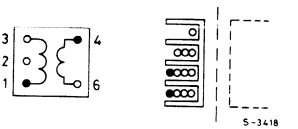


Fig. 15 - L2 Oscillator coil



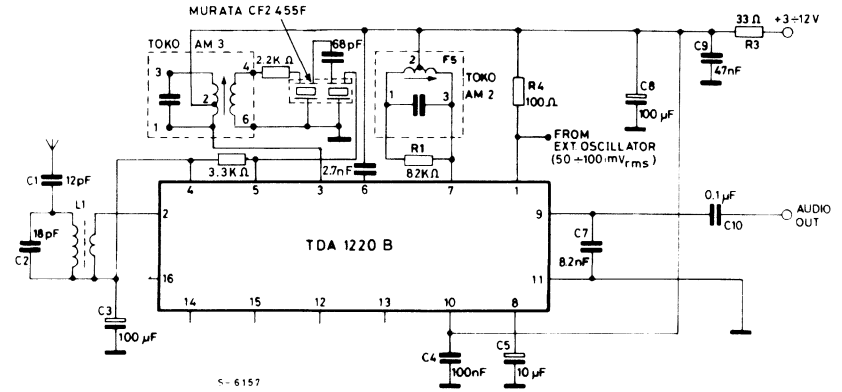
Coil support: Toko 10K
Primary winding: 10 Turns of enamelled copper wire 0.16 mm diameter (pins 3-1).
Secondary winding: 4 Turns copper wire 0.16 mm diameter (pins 6-4)

Fig. 16 - L1 Antenna Coil



Coil support: Toko 10K.
Primary winding: as L2 (pins 3-1)
Secondary winding: 2 Turns copper wire 0.16 mm diameter (pins 6-4)

Fig. 17 - Low cost 27 MHz receiver with external xtal oscillator



APPLICATION INFORMATION (continued)

Fig. 18 - 455 KHz FM narrow band IF

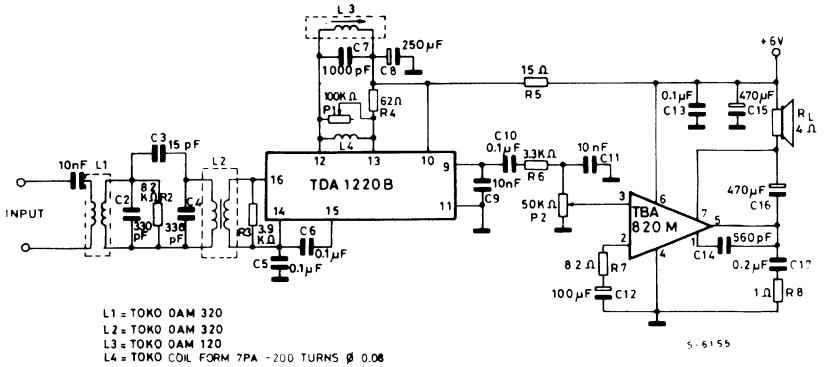
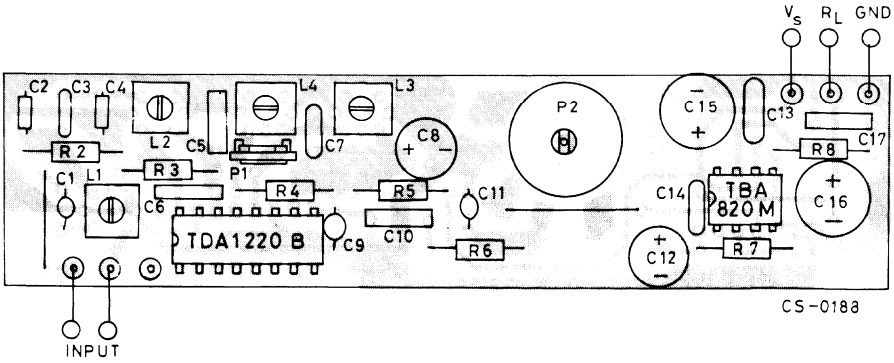


Fig. 19 - P.C. board and component layout of the circuit of fig. 18



APPLICATION INFORMATION (continued)

Fig. 20 - Discriminator "S" curve response (circuit of fig. 18)

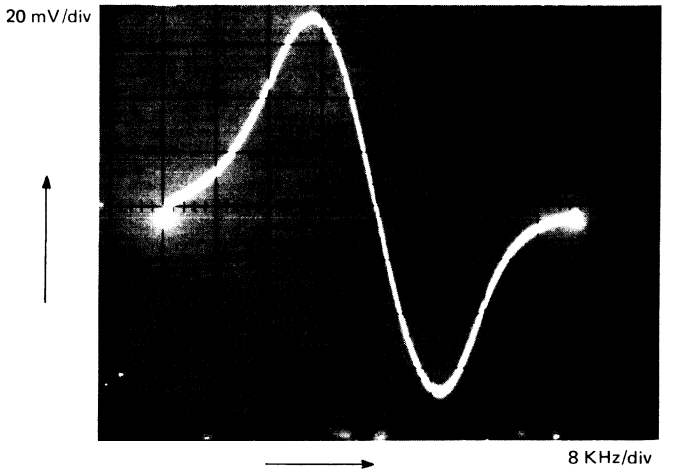
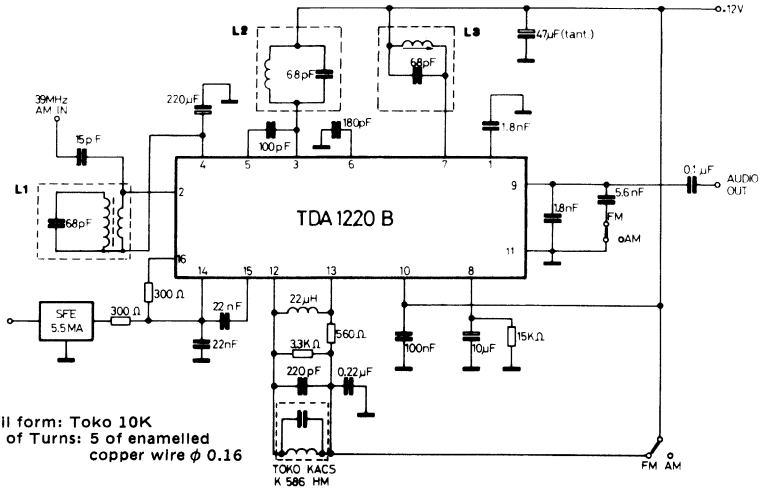


Fig. 21 - Application in sound channel of multistandard TV or in parallel AM modulated sound channel (AM section only).



L2, L3 Coil form: Toko 10K
N° of Turns: 5 of enamelled copper wire ϕ 0.16

L1 Coil form: Toko 10K
N° of Turns: 5+2 of enamelled copper wire ϕ 0.16

ELECTRICAL CHARACTERISTICS (V_s = 12V)

AM Section (f_o = 39MHz; f_m = 15KHz)

Parameter	Typ	Unit
Audio out (m = 0.3)	60	mV
S/N (V_i = 100 μV; m = 0.3)	37	dB
S/N (V_i = 1mV; m = 0.3)	55	dB
S/N (V_i = 10mV; m = 0.3)	56	dB
AGC range (m = 0.8, ΔVout = 3dB)	65	dB
Max input signal handling (m = 0.8; d = 5%)	150	mV
−3dB bandwidth	600	KHz
Distortion (V_i = 100 μV; m = 0.3)	2	%
(V_i = 1mV; m = 0.3)	1	%
(V_i = 10mV; m = 0.3)	0.8	%
(V_i = 100 μV; m = 0.8)	7	%
(V_i = 1mV; m = 0.8)	5	%
(V_i = 10mV; m = 0.8)	3	%

FM Section (f_o = 5.5MHz; f_m = 1KHz)

Parameter	Typ	Unit
−3dB input limiting voltage (Δf = 25KHz)	3	μV
AMR (Δf = +25KHz; m = 0.3; V_i = 100 μV)	40	dB
(Δf = +25KHz; m = 0.3; V_i = 1mV)	58	dB
(Δf = +25KHz; m = 0.3; V_i = 10mV)	54	dB
S/N (Δf = ±25KHz; V_i = 100 μV)	51	dB
S/N (Δf = ±25KHz; V_i = 1mV)	70	dB
S/N (Δf = ±25KHz; V_i = 10mV)	70	dB
Distortion (Δf = ±25KHz; V_i = 100 μV)	0.5	%
(Δf = ±25KHz; V_i = 1mV)	0.6	%
(Δf = ±25KHz; V_i = 10mV)	0.6	%
(Δf = ±50KHz; V_i = 100 μV)	1	%
(Δf = ±50KHz V_i = 1mV)	1	%
(Δf = ±50KHz; V_i = 10mV)	1	%
Recovered audio (Δf = ±15KHz; V_i = 1mV) (Recovered audio can be varied by variation of 3.3K ohm resistor in parallel with the discriminator coil)	70	mV
Max input signal handling	1	V

Note: AM performance at 39MHz can be improved by mean of a selective preamplifier stage.

TDA1220L

LOW VOLTAGE AM-FM RADIO

The TDA1220L is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in 4.5V-6V portable AM-FM radio receivers.

The functions incorporated are:

AM SECTION

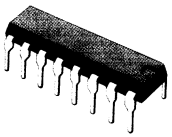
- Preamplifier and double balanced mixer
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

FM SECTION

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA1220L is suitable for AM applications up to 30MHz and for FM-IF and features:

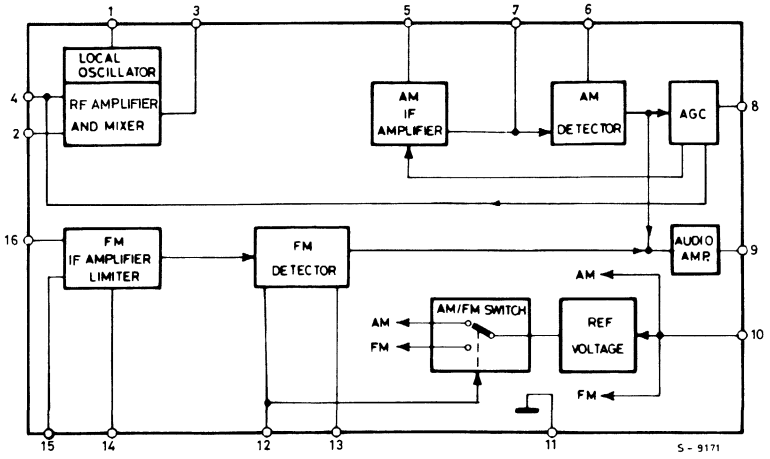
- High sensitivity and low noise
- Very low tweet
- High signal handling
- Low battery drain
- AM sensitivity regulation facility
- Operating supply voltage: 2.5V to 9V
- Very simple DC switching of AM-FM



DIP-16 Plastic
(0.25)

ORDERING NUMBER: TDA1220LK

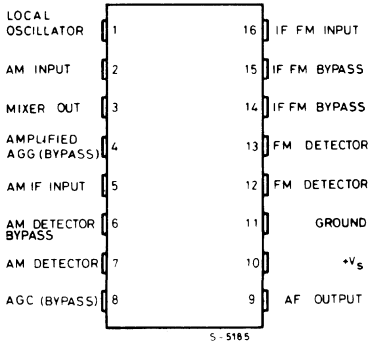
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	12	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s= 4.5V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_d	Drain current	AM section			10	15	mA
		FM section			7	11	mA

AM SECTION (f_o = 1 MHz; f_m= 1 KHz)

V_i	Input sensitivity	S/N = 26 dB	m = 0.3		15	25	μV
S/N		V_i = 10 mV	m = 0.3	45	50		dB
V_i	AGC range	ΔV_{out}= 10 dB	m = 0.8	94	100		dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	70	90	120	mV
d	Distortion				0.4	1	%
V_H	Max input signal handling capability	m = 0.8	d < 10%	1			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)			3.5	5	6.5	KΩ
	Tweet 2 IF	m = 0,3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB

FM SECTION (f_o = 10.7 MHz; f_m= 1 KHz)

V_i	Input limiting voltage	-3 dB limiting point			26	36	μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3	35	46		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz	V_i = 1 mV	55	64		dB
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.3	0.6	%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV	55	80	100	mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)			3.5	5	6.5	KΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 3V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_d	Drain current	AM section			9	14	mA
		FM section			6	10	mA
AM SECTION (f_o = 1 MHz; f_m = 1 KHz)							
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		15	25	μV
S/N		V_i = 10 mV	m = 0.3	45	50		dB
V_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	94	100		dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	70	95	120	mV
d	Distortion				0.4	1	%
V_H	Max input signal handling capability	m = 0.8	d < 10%	1			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)			3.5	5	6.5	KΩ
	Tweet 2 IF	m = 0,3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB
FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)							
V_i	Input limiting voltage	-3 dB limiting point			40	75	μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3	35	42		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz	V_i = 1 mV	55	64		dB
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.3	0.7	%
		Δf = 75 KHz			0.9		%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV	55	80	100	mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)			3.5	5	6.5	KΩ

Fig. 1 - Test circuit

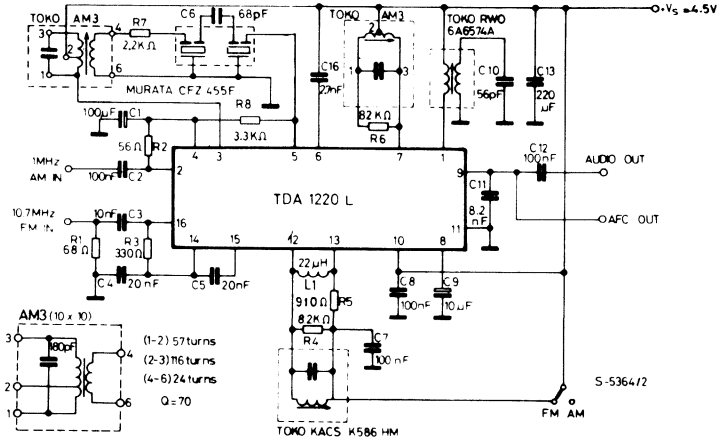
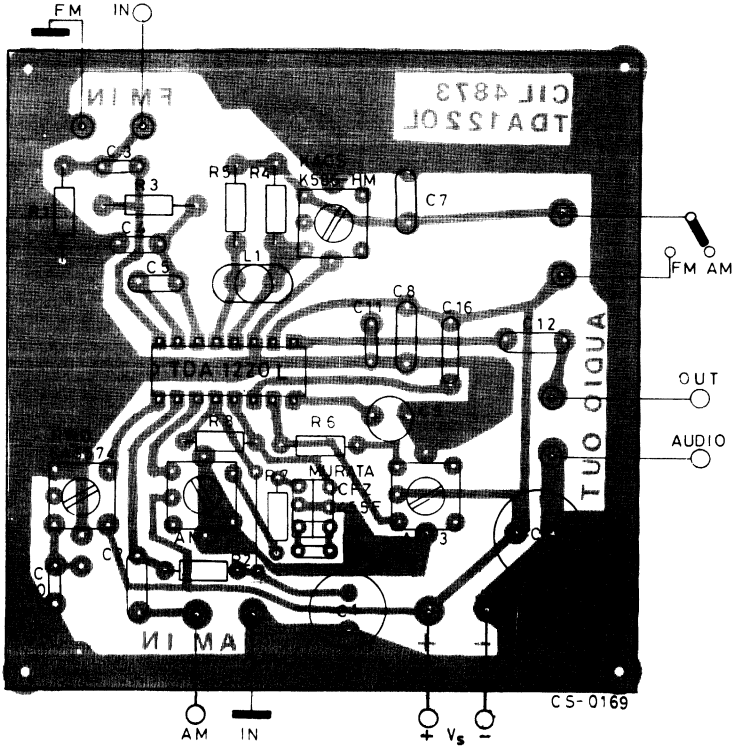


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.



APPLICATION INFORMATION

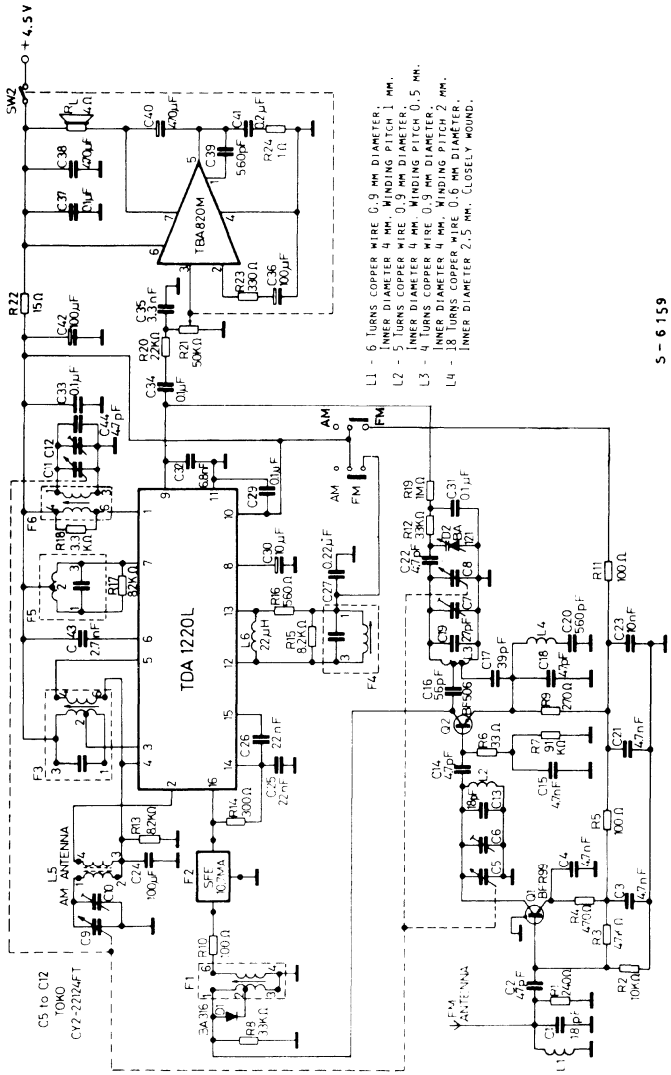
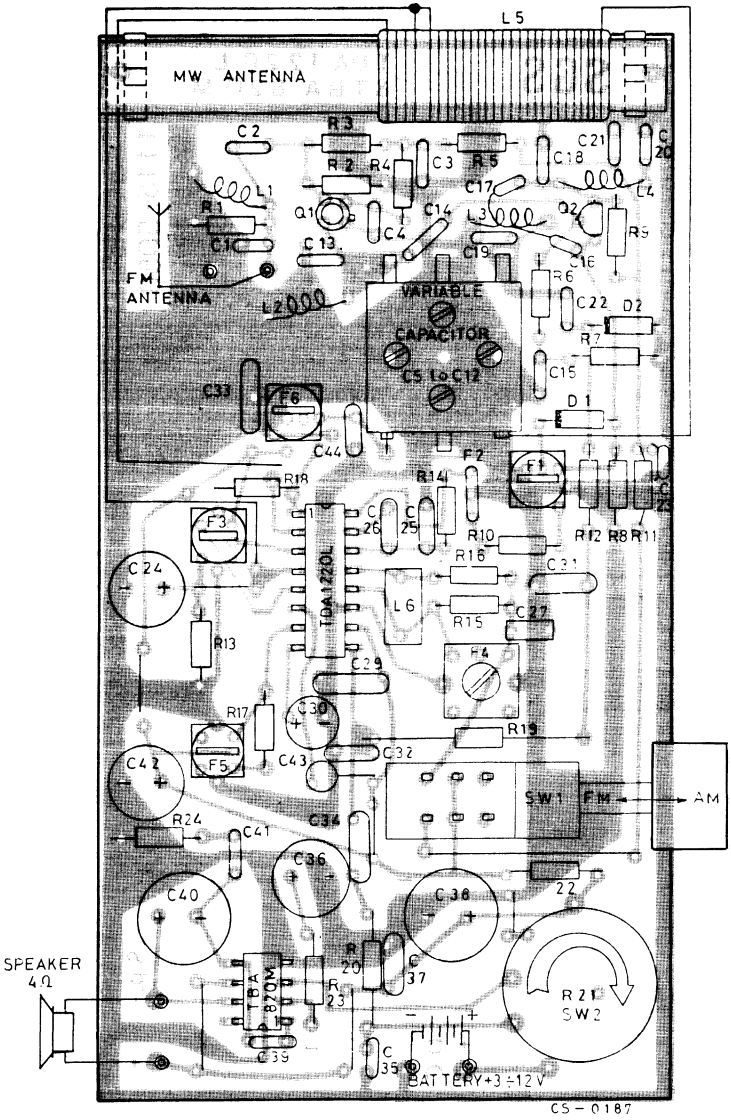


Fig. 3 - Portable AM/FM radio

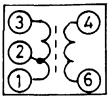
APPLICATION INFORMATION

Fig. 4 - PC board and component layout of the circuit of fig. 3. (1:1 scale)



APPLICATION INFORMATION (continued)

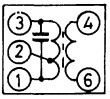
F1 - 10.7 MHz IF Coil



C_o (pF)	f (MHz)	Q_o	TURNS			
		1-3	1-2	2-3	4-6
–	10.7	1.05	6	8	2

TOKO - FM1 - 7x7 mm.
119 AN - A5066R

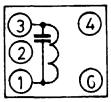
F3 - 455 KHz IF Coil



C_o (pF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	63	81	7

TOKO - AM1 - 7x7 mm.
7LC - A5070EK

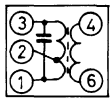
F4 - FM Detector Coil



C_o (pF)	f (MHz)	Q_o	TURNS		
1-3		1-3	1-3	–	–
82	10.7	100	12	–	–

TOKO - 10x10 mm.
KACS - K586 HM

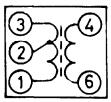
F5 - 455 KHz IF Coil



C_o (pF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	41	103	20

TOKO - AM3 - 7x7 mm.
7LC - A5073 EK

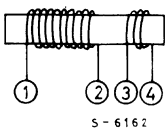
F6 - AM Oscillator Coil



f (KHz)	L (μH)	Q_o	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	320	80	90	3	9

TOKO - OAM320 - 7x7 mm.
7BO - A5071 DC

L5 - Antenna Coil



f (KHz)	L (μH)	Q_o	TURNS	
	1-2	1-2	1-2	3-4
796			105	7

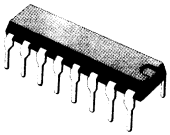
WIRE: LITZ - 10x0.05 mm.
CORE: 10x80 mm.

TDA1904

4W AUDIO AMPLIFIER

- HIGH OUTPUT CURRENT CAPABILITY (UP TO 2A)
- PROTECTION AGAINST CHIP OVERTEMPERATURE
- LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- SUPPLY VOLTAGE RANGE: 4V TO 20V

The TDA 1904 is a monolithic integrated circuit in POWERDIP package intended for use as low-frequency power amplifier in wide range of applications in portable radio and TV sets.



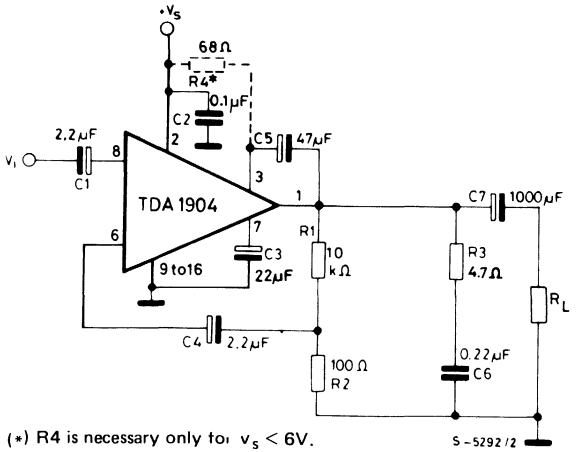
Powerdip
(8 + 8)

ORDERING NUMBER: TDA 1904

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	20	V
I_O	Peak output current (non repetitive)	2.5	A
I_O	Peak output current (repetitive	2	A
P_{tot}	Total power dissipation at $T_{amb} = 80°C$	1	W
	at $T_{pins} = 60°C$	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

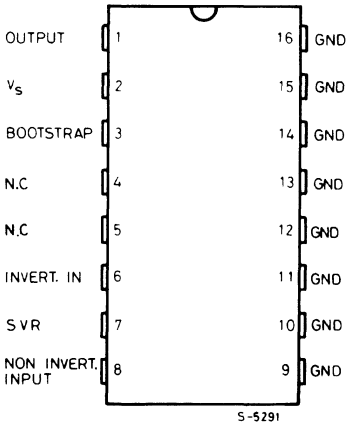
TEST AND APPLICATION CIRCUIT



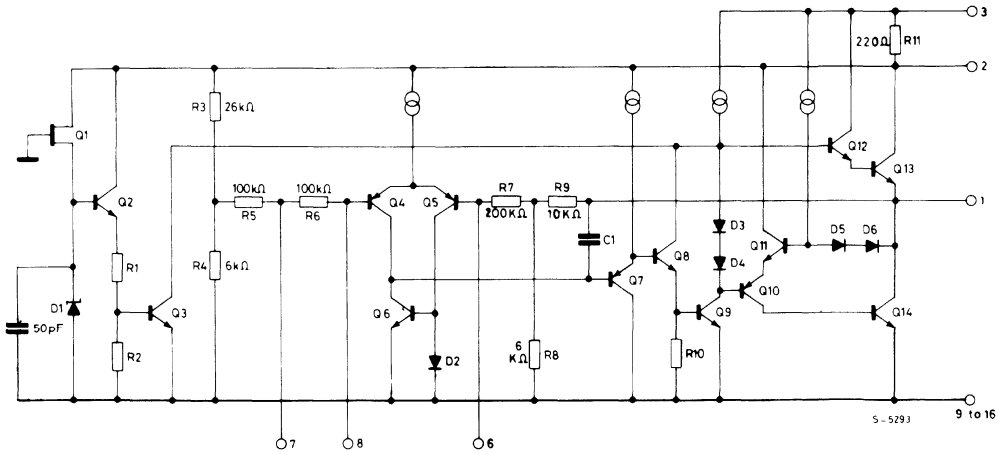
(*) R4 is necessary only for $v_s < 6V$.

TDA1904

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, R_{th} (heatsink) = 20°C/W, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
V_o	Quiescent output voltage	V_s = 4V V_s = 14V		2.1 7.2		V
I_d	Quiescent drain current	V_s = 9V V_s = 14V		8 10	15 18	mA
P_o	Output power	d = 10% f = 1 KHz V_s = 9V R_L = 4Ω V_s = 14V V_s = 12V V_s = 6V	1.8 4 3.1 0.7	2 4.5		W
d	Harmonic distortion	f = 1 KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.2W		0.1	0.3	%
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V	0.8 1.3			V
R_i	Input resistance (pin 8)	f = 1 KHz	55	150		KΩ
η	Efficiency	f = 1 KHz V_s = 9V R_L = 4Ω P_o = 2W V_s = 14V R_L = 4Ω P_o = 4.5W		70 65		%
BW	Small signal bandwidth (-3 dB)	V_s = 14V R_L = 4Ω	40 to 40,000			Hz
G_v	Voltage gain (open loop)	V_s = 14V f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 14V R_L = 4Ω f = 1 KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	R_g = 50Ω (°) R_g = 10 KΩ		1.2 2	4	μV
		R_g = 50Ω (°°) R_g = 10 KΩ		2 3		μV
SVR	Supply voltage rejection	V_s = 12V f_{ripple}= 100 Hz R_g = 10 KΩ V_{ripple}= 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down case temperature	P_{tot}= 2W		120		°C

Note: (°) Weighting filter = curve A.
(°°) Filter with noise bendwidth: 22 Hz to 22 KHz.

Fig. 1 - Test and application circuit

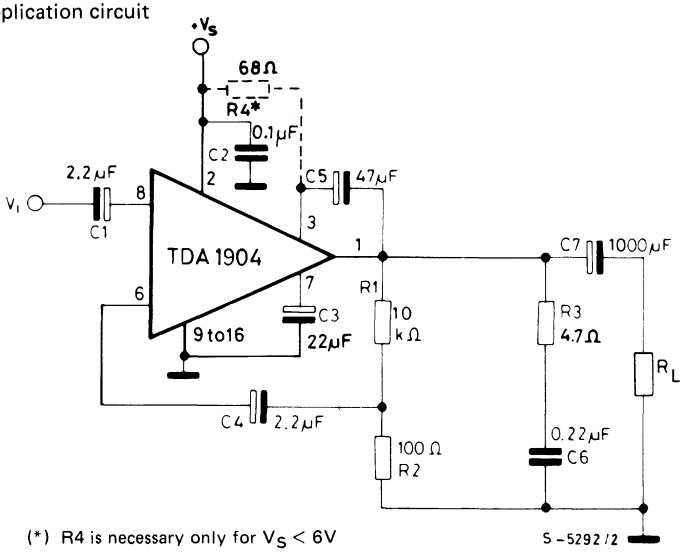
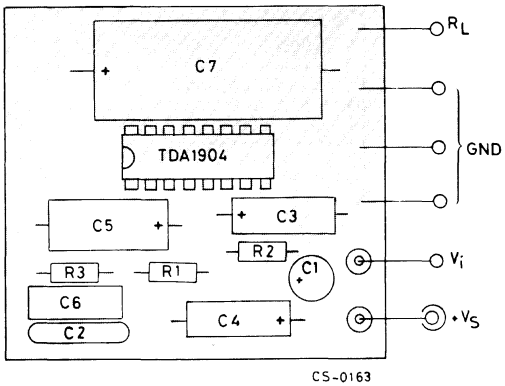


Fig. 2 - P.C. board and components layout of fig. 1 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 1.
When the supply voltage V_S is less than 6V, a 68Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Components	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range	
					Min.	Max.
R1	10 KΩ	Feedback resistors	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R3	
R2	100 Ω		Decrease of gain.	Increase of gain.		1 KΩ
R3	4.7 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R4	68 Ω	Increase of the output swing with low supply voltage.			39 Ω	220 Ω
C1	2.2 μF	Input DC decoupling.	Higher cost lower noise.	Higher low frequency cutoff. Higher noise.		
C2	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C3	22 μF	Ripple rejection	Increase of SVR increase of the switch-on time.	Degradation of SVR.	2.2 μF	100μF
C4	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise	Higher low frequency cutoff.	0.1 μF	
C5	47 μF	Bootstrap.		Increase of the distortion at low frequency.	10 μF	100μF
C6	0.22 μF	Frequency stability.		Danger of oscillation.		
C7	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

Fig. 3 - Quiescent output voltage vs. supply voltage

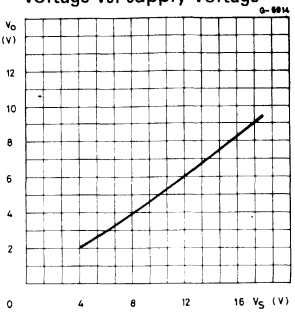


Fig. 4 - Quiescent drain current vs. supply voltage

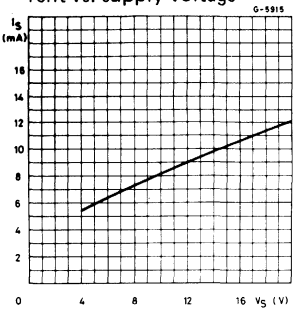


Fig. 5 - Output power vs. supply voltage

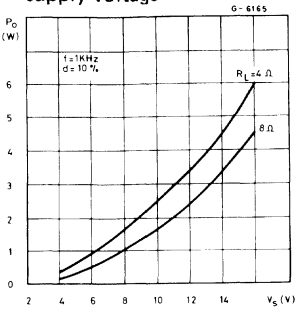


Fig. 6 - Distortion vs. output power

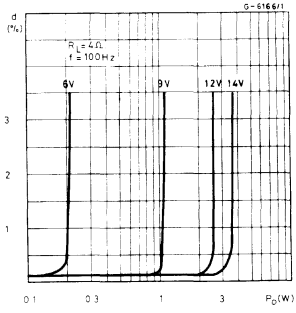


Fig. 7 - Distortion vs. output power

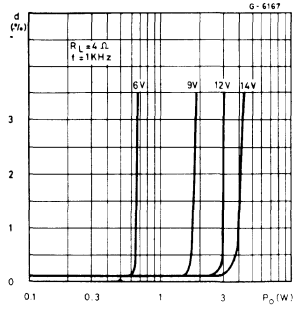


Fig. 8 - Distortion vs. output power

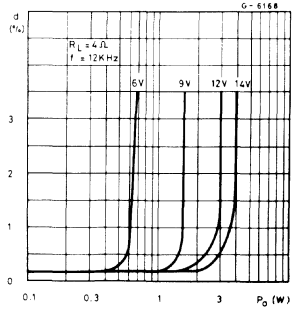


Fig. 9 - Distortion vs. output power

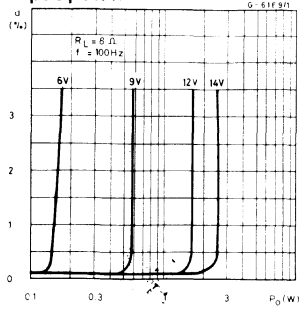


Fig. 10 - Distortion vs. output power

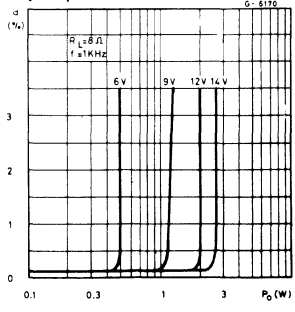


Fig. 11 - Distortion vs. output power

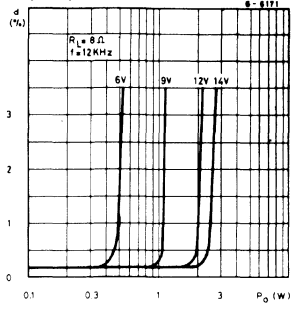


Fig. 12 - Distortion vs. frequency

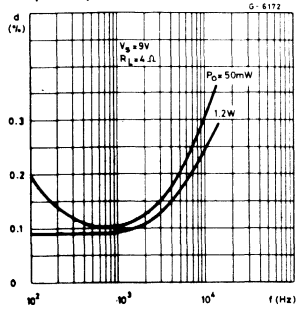


Fig. 13 - Distortion vs. frequency

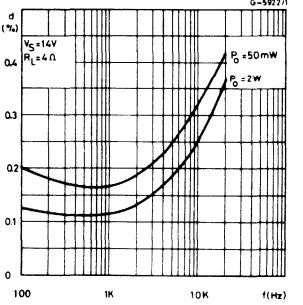


Fig. 14 - Distortion vs. frequency

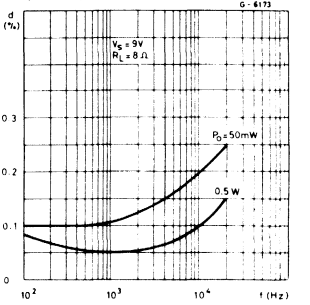


Fig. 15 - Distortion vs. frequency

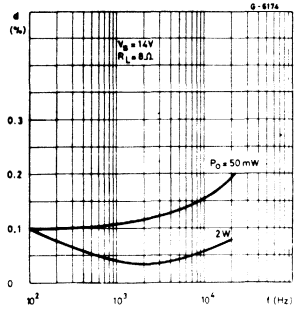


Fig. 16 - Supply voltage rejection vs. frequency

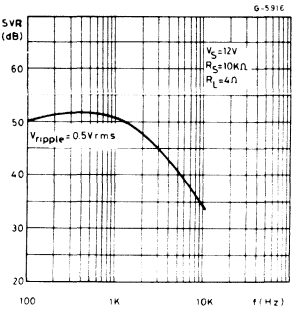


Fig. 17 - Total power dissipation and efficiency vs. output power

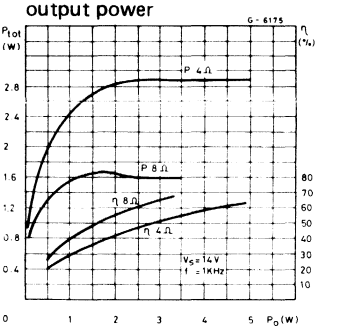


Fig. 18 - Total power dissipation vs. output power

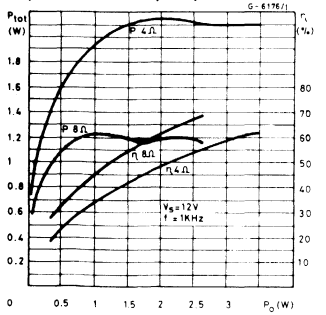


Fig. 19 - Total power dissipation vs. output power

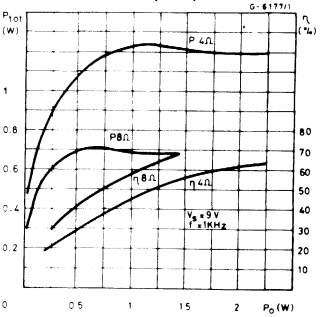
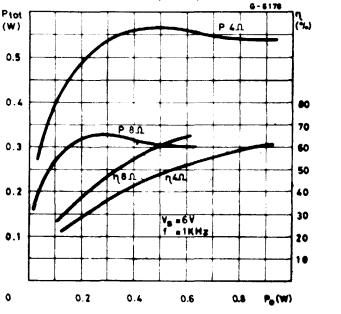


Fig. 20 - Total power dissipation vs. output power



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150°C.

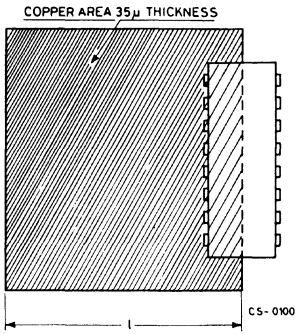
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

MOUNTING INSCTRUCTION

The TDA 1904 is assembled in the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat produced by the chip.

Figure 21 shows a PC board copper area used as a heatsink (l = 65 mm).
The thermal resistance junction-ambient is 35°C.

Fig. 21- Example of heatsink using PC board copper (l = 65 mm)



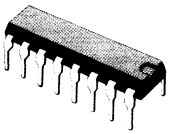
TDA1905

5W AUDIO AMPLIFIER WITH MUTING

The TDA1905 is a monolithic integrated circuit in POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise
- voltage range 4V to 30V

The TDA 1905 is assembled in a new plastic package, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6W and a thermal resistance of 15°C/W (junction to pins).



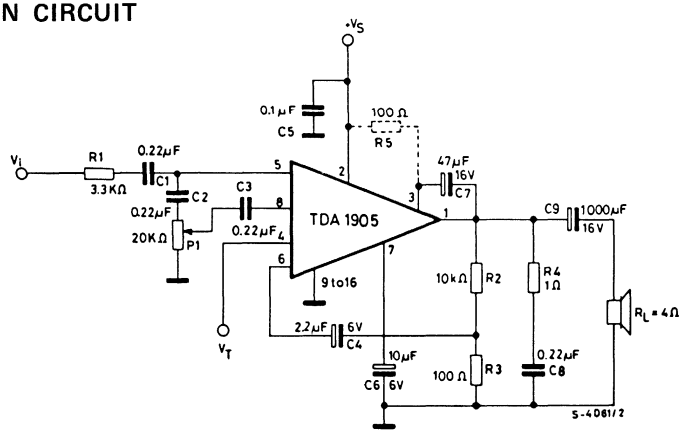
Powerdip
(8 + 8)

ORDERING NUMBER: TDA1905

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3	A
I_o	Output peak current (repetitive)	2.5	A
V_i	Input voltage	0 to + V_s	V
V_i	Differential input voltage	± 7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at T_{amb} = 80°C	1	W
	T_{case} = 60°C	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

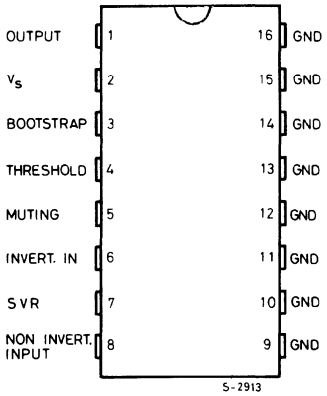
APPLICATION CIRCUIT



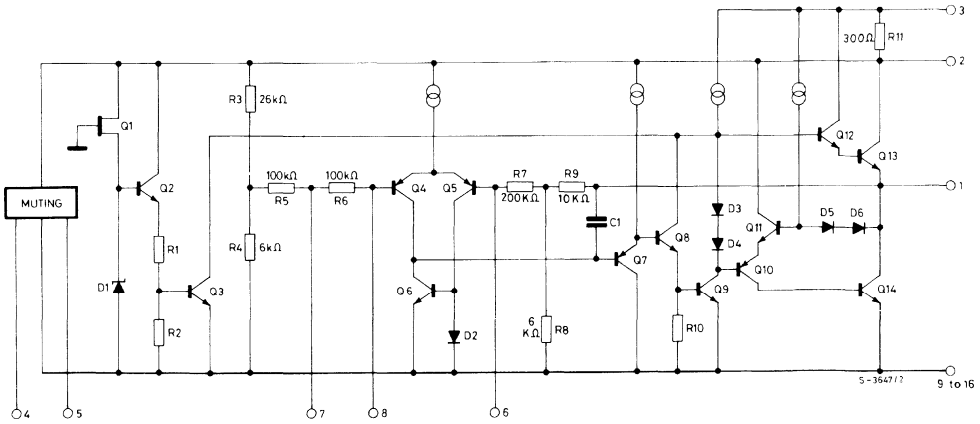
TDA1905

CONNECTION DIAGRAM

(Top view)



SCHEMATIC DIAGRAM

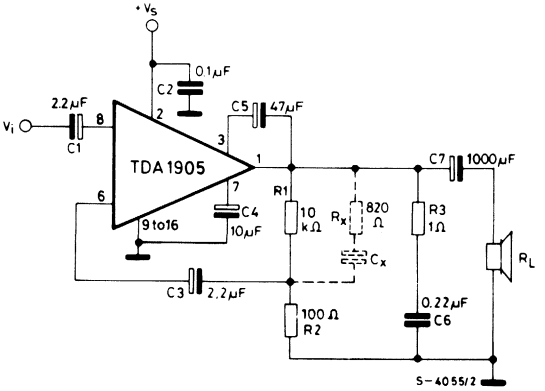


THERMAL DATA

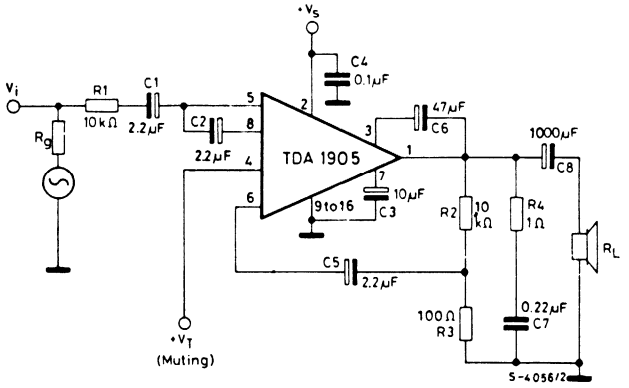
$R_{thj\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	max	70	°C/W

TEST CIRCUITS:

WITHOUT MUTING



WITH MUTING FUNCTION



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, R_{th} (heatsink) = 20°C/W, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		30	V
V_o	Quiescent output voltage	V_s = 4V V_s = 14V V_s = 30V	1.6 6.7 14.4	2.1 7.2 15.5	2.5 7.8 16.8	V
I_d	Quiescent drain current	V_s = 4V V_s = 14V V_s = 30V		15 17 21	 35	mA
$V_{CE\ sat}$	Output stage saturation voltage	I_C = 1A I_C = 2A		0.5 1		V
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 4Ω (*) V_s = 14V R_L = 4Ω V_s = 18V R_L = 8Ω V_s = 24V R_L = 16Ω	 2.2 5 5 4.5	 2.5 5.5 5.5 5.3		W
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 14V R_L = 4Ω P_o = 50 mW to 3W V_s = 18V R_L = 8Ω P_o = 50 mW to 3W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		 0.1 0.1 0.1 0.1		%
V_i	Input sensitivity	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 37 49 73 100		mV
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4			V
R_i	Input resistance (pin 8)	f = 1KHz	60	100		KΩ
I_d	Drain current	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 380 550 410 295		mA
η	Efficiency	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 73 71 74 75		%

(*) With an external resistor of 100Ω between pin 3 and $+V_s$.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
BW	Small signal bandwidth (-3dB)	V_s = 14V R_L = 4Ω P_o = 1W		40 to 40,000			Hz
G_v	Voltage gain (open loop)	V_s = 14V f = 1KHz			75		dB
G_v	Voltage gain (closed loop)	V_s = 14V R_L = 4Ω f = 1KHz P_o = 1W		39.5	40	40.5	dB
e_N	Total input noise		R_g = 50Ω R_g = 1KΩ (°) R_g = 10KΩ		1.2 1.3 1.5	4.0	μV
			R_g = 50Ω R_g = 1KΩ (°°) R_g = 10KΩ		2.0 2.0 2.2	6.0	μV
S/N	Signal to noise ratio	V_s = 14V P_o = 5.5W R_L = 4Ω	R_g = 10KΩ R_g = 0 (°)		90 92		dB
			R_g = 10KΩ R_g = 0 (°°)		87 87		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 8Ω f_{ripple} = 100 Hz R_g = 10KΩ V_{ripple} = 0.5Vrms		40	50		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot} = 2.5W			115		°C

MUTING FUNCTION

$V_{T_{OFF}}$	Muting-off threshold voltage (pin 4)		1.9		4.7	V
$V_{T_{ON}}$	Muting-on threshold voltage (pin 4)		0		1.3	V
			6.2		V_s	
R_5	Input resistance (pin 5)	Muting off	80	200		KΩ
		Muting on		10	30	Ω
R_4	Input resistance (pin 4)		150			KΩ
A_T	Muting attenuation	$R_g + R_1$ = 10KΩ	50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 30 and fig. 31

Fig. 1 - Quiescent output voltage vs. supply voltage

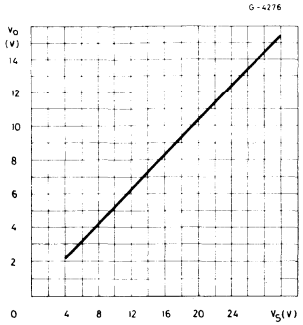


Fig. 2 - Quiescent drain current vs. supply voltage

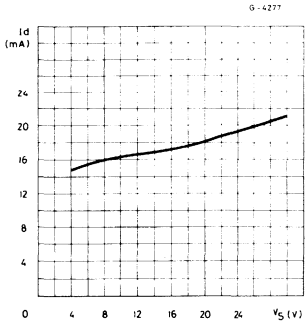


Fig. 3 - Output power vs. supply voltage

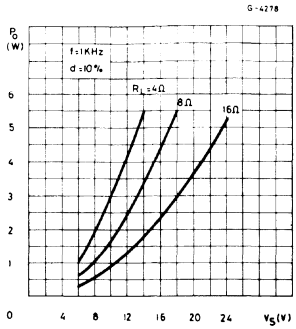


Fig. 4 - Distortion vs. output power (R_L = 16Ω)

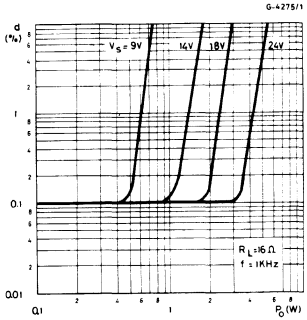


Fig. 5 - Distortion vs. output power (R_L = 8Ω)

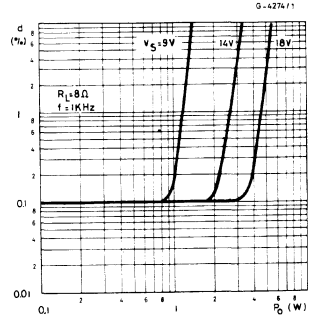


Fig. 6 - Distortion vs. output power (R_L = 4Ω)

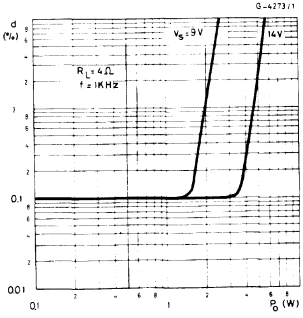


Fig. 7 - Distortion vs. frequency (R_L = 16Ω)

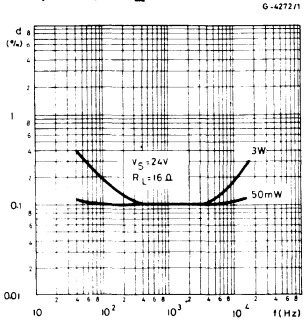


Fig. 8 - Distortion vs. frequency (R_L = 8Ω)

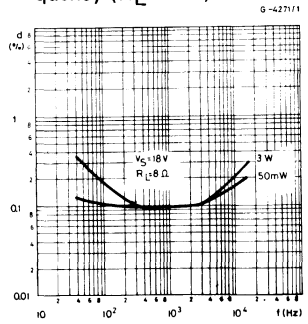


Fig. 9 - Distortion vs. frequency (R_L = 4Ω)

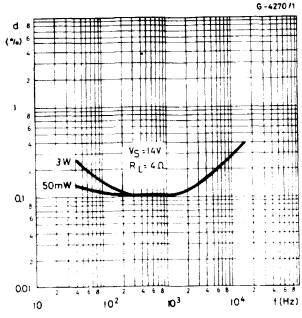


Fig. 10 - Open loop frequency response

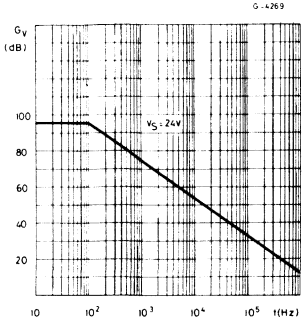


Fig. 11 - Output power vs. input voltage

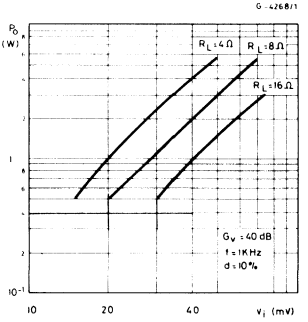


Fig. 12 - Value of capacitor Cx vs. bandwidth (BW) and gain (Gv)

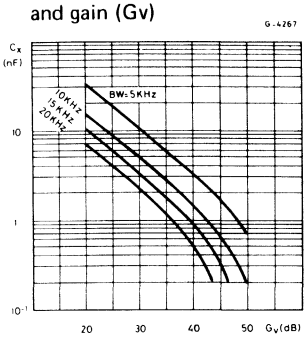


Fig. 13 - Supply voltage rejection vs. voltage gain (ref. to the Muting circuit)

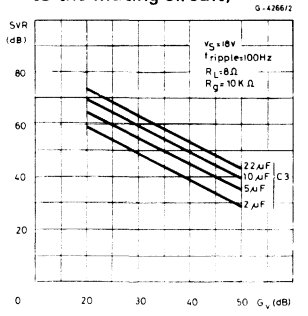


Fig. 14 - Supply voltage rejection vs. source resistance

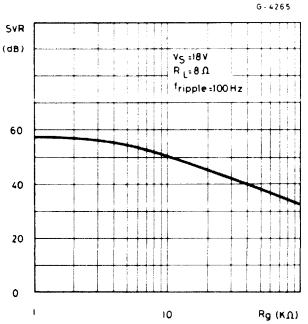


Fig. 15 - Max power dissipation vs. supply voltage (sine wave operation)

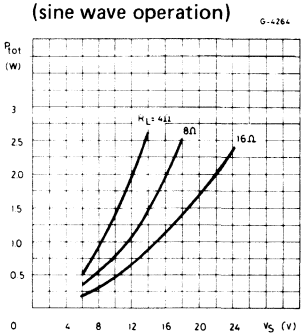


Fig. 16 - Power dissipation and efficiency vs. output power

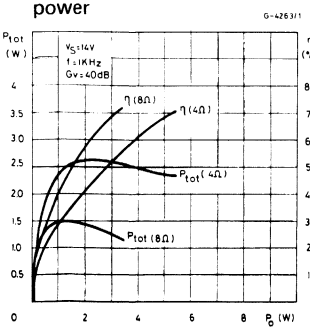


Fig. 17 - Power dissipation and efficiency vs. output power

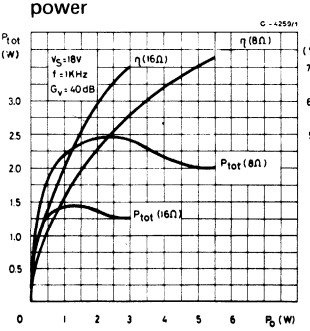
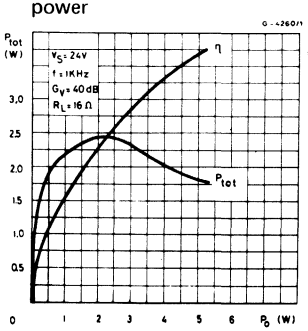
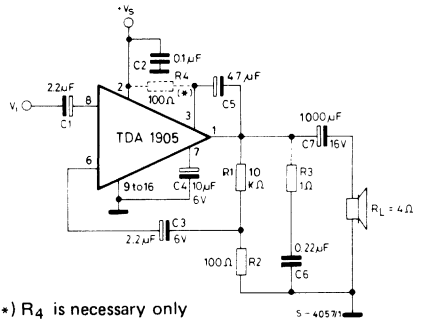


Fig. 18 - Power dissipation and efficiency vs. output power



APPLICATION INFORMATION

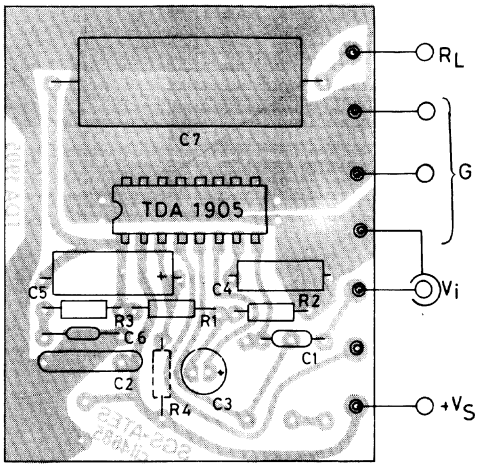
Fig. 19 - Application circuit without muting



(*) R_4 is necessary only for $V_s < 10V$.

$P_o = 5.5W$ (d = 10%)
$V_s = 14V$
$I_d = 0.55A$
$G_v = 40$ dB

Fig. 20 - PC board and components lay-out of the circuit of fig. 19 (1:1 scale)



CS-0129/1

Fig. 21 - Application circuit with muting

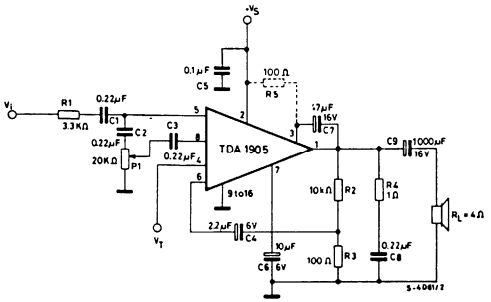
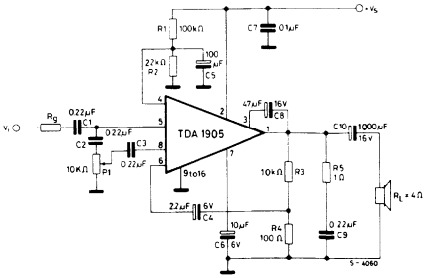


Fig. 22 - Delayed muting circuit



APPLICATION INFORMATION (continued)

Fig. 23 - Low-cost application circuit without bootstrap.

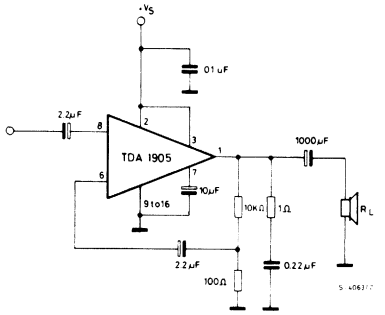


Fig. 24 - Output power vs. supply voltage (circuit of fig. 23)

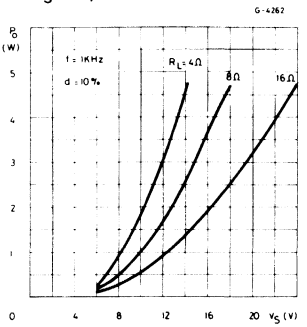


Fig. 25 - Two position DC tone control using change of pin 5 resistance (muting function)

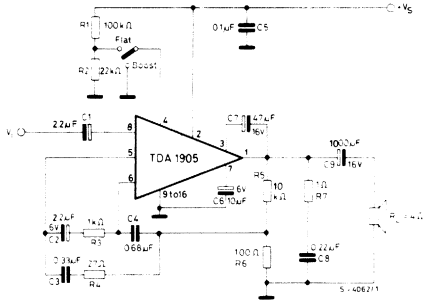


Fig. 26 - Frequency response of the circuit of fig. 25

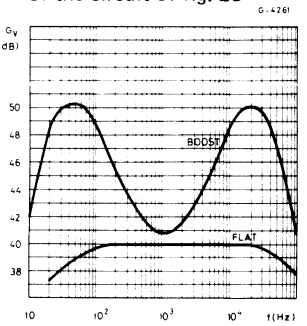


Fig. 27 - Bass Bomb tone control using change of pin 5 resistance (muting function)

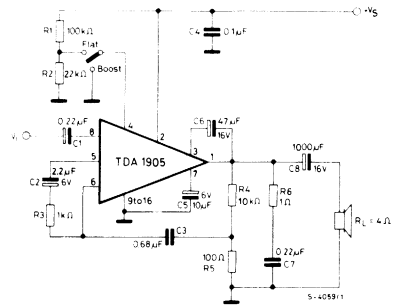
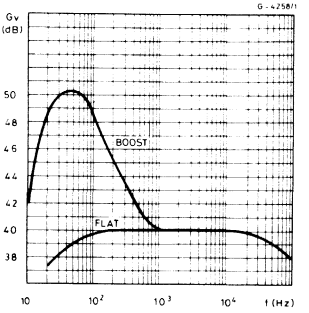


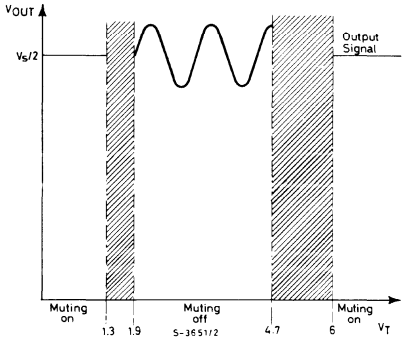
Fig. 28 - Frequency response of the circuit of fig. 27



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 4, as shown in fig. 29

Fig. 29

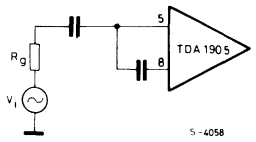


The input resistance at pin 5 depends on the threshold voltage V_T at pin 4 and is typically:

$R_5 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_5 = 10\Omega$ @ $0V \leqslant V_T \leqslant 1.3V$ or $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression:



$$A_T = \frac{V_i}{V_8} = \frac{R_g + \left(\frac{R_8 \cdot R_5}{R_8 + 5}\right)}{\left(\frac{R_8 \cdot R_5}{R_8 + R_5}\right)}$$

where $R_8 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, tipically 1.2 dB.
A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 4 is greater than 150 $K\Omega$. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 22)
- during switching at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 5 can be useful in many application and two examples are shown in fig. 25 and 27, where it has been used to change the feedback network, obtaining 2 different frequency response.

APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 21. When the supply voltage V_s is less than 10V, a 100Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Component	Raccom. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range Min.	Max.
$R_g + R_1$	10KΩ	Input signal imped. for muting operation	Increase of the attenuation in muting-on condition. Decrease of the input sensitivity.	Decrease of the attenuation in muting on condition.		
R_2	10KΩ	Feedback resistors	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R_3	
R_3	100Ω		Decrease of gain.	Increase of gain.		1KΩ
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R_5	100Ω	Increase of the output swing with low supply voltage.			47	330
P_1	20KΩ	Volume potentiometer	Increase of the switch-on noise.	Decrease of the input impedance and of the input level.	10KΩ	100KΩ
C_1 C_2 C_3	0.22 μF	Input DC decoupling.	Higher cost lower noise.	Higher low frequency cutoff. Higher noise		
C_4	2.2μF	Inverting input DC decoupling.	Increase of the switch-on noise.	Higher low frequency cutoff.	0.1μF	
C_5	0.1μF	Supply voltage bypass.		Danger of oscillations.		
C_6	10 μF	Ripple rejection	Increase of SVR increase of the switch-on time	Degradation of SVR	2.2 μF	100 μF
C_7	47μF	Bootstrap.		Increase of the distortion at low frequency.	10μF	100μF
C_8	0.22μF	Frequency stability.		Danger of oscillation.		
C_9	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 32 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 30 - Output power and drain current vs. case temperature.

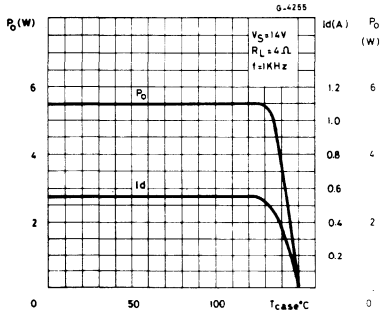


Fig. 31 - Output power and drain current vs. case temperature

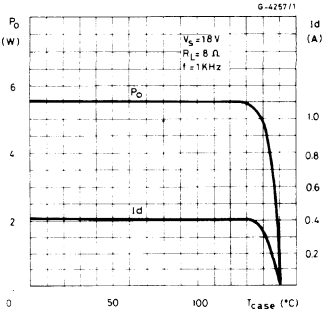
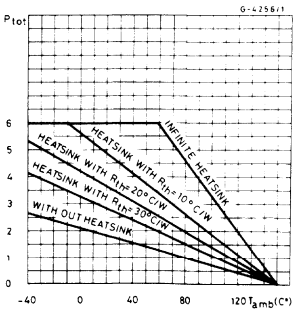


Fig. 32 - Maximum allowable power dissipation vs. ambient temperature.



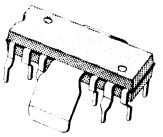
MOUNTING INSTRUCTION: See TDA1904

TDA1908

8W AUDIO AMPLIFIER

The TDA1908 is a monolithic integrated circuit in 12 lead quad in-line plastic package intended for low frequency power applications. The mounting is compatible with the old types TBA800, TBA810S, TCA830S and TCA940N. Its main features are:

- flexibility in use with a max output curent of 3A and an operating supply voltage range of 4V to 30V;
- protection against chip overtemperature;
- soft limiting in saturation conditions;
- low "switch-on" noise;
- low number of external components;
- high supply voltage rejection;
- very low noise.



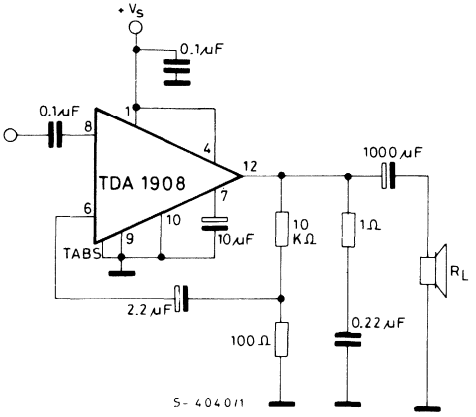
Findip

ORDER CODE: TDA1908

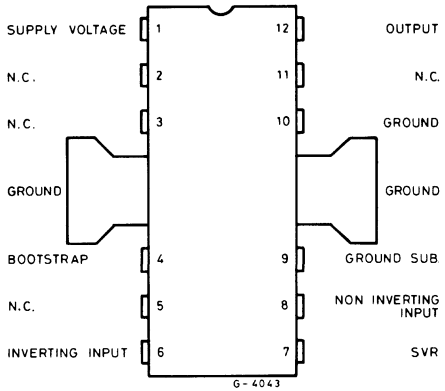
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3.5	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation: at $T_{amb} = 80°C$	1	W
	at $T_{amb} = 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

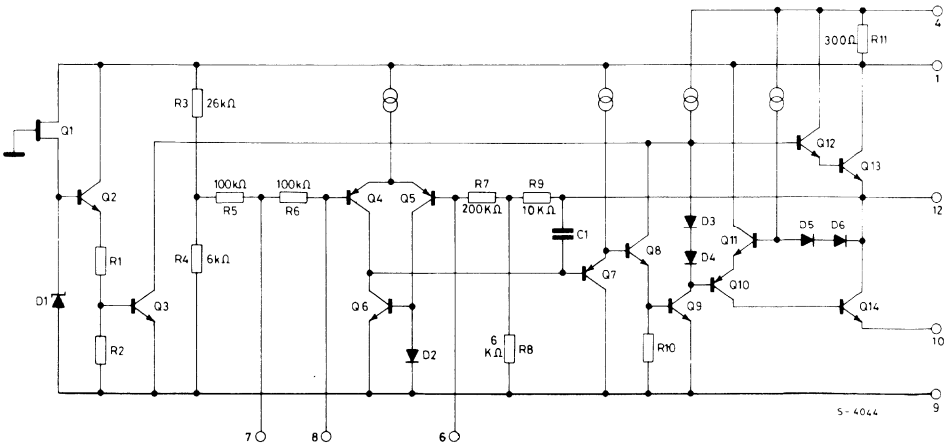
APPLICATION CIRCUIT



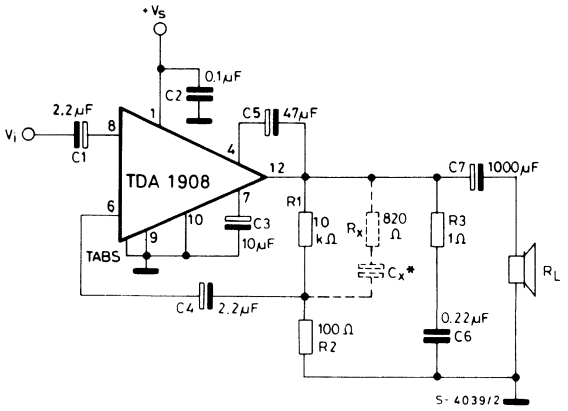
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



TEST CIRCUIT



* See fig. 12.

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	(°) 70	°C/W

(°) Obtained with tabs soldered to printed circuit board with min copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, R_{th} (heatsink)= 8 °C/W, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		30	V
V_o	Quiescent output voltage	V_s = 4V V_s = 18V V_s = 30V	1.6 8.2 14.4	2.1 9.2 15.5	2.5 10.2 16.8	V
I_d	Quiescent drain current	V_s = 4V V_s = 18V V_s = 30V		15 17.5 21	 35	mA
V_{CEsat}	Output stage saturation voltage (each output transistor)	I_C= 1A I_C= 2.5A		0.5 1.3		V
P_o	Output power	d = 10% f = 1 KHz V_s = 9V R_L= 4Ω V_s = 14V R_L= 4Ω V_s = 18V R_L= 4Ω V_s = 22V R_L= 8Ω V_s = 24V R_L= 16Ω	 7 6.5 4.5	 2.5 5.5 9 8 5.3		W

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test condition	Min.	Typ.	Max	Unit
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 18V R_L = 4Ω P_o = 50 mW to 4W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		0.1 0.1 0.1		%
V_i	Input sensitivity	V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 4Ω P_o = 9W V_s = 22V R_L = 8Ω P_o = 8W V_s = 24V R_L = 16Ω P_o = 5.3W		37 52 64 90 110		mV
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4			V
R_i	Input resistance (pin 8)	f = 1 KHz	60	100		KΩ
I_s	Drain current	f = 1 KHz V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 4Ω P_o = 9W V_s = 22V R_L = 8Ω P_o = 8W V_s = 24V R_L = 16Ω P_o = 5.3W		570 730 500 310		mA
η	Efficiency	V_s = 18V f = 1 KHz R_L = 4Ω P_o = 9W		72		%
BW	Small signal bandwidth (-3 dB)	V_s = 18V R_L = 4Ω P_o = 1W	40 to 40 000			Hz
G_v	Voltage gain (open loop)	f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 18V R_L = 4Ω f = 1 KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	(°) R_g = 50Ω R_g = 1KΩ R_g = 10 KΩ		1.2 1.3 1.5	4.0	μV
		(°°) R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		2.0 2.0 2.2	6.0	μV
S/N	Signal to noise ratio	V_s = 18V P_o = 9W R_L = 4Ω; R_g = 10KΩ R_g = 0 (°)		92 94		dB
		V_s = 18V P_o = 9W R_L = 4Ω; R_g = 10KΩ R_g = 0 (°°)		88 90		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 4Ω f_{ripple} = 100 Hz R_g = 10KΩ	40	50		dB
T_{sd}	Thermal shut-down junction temperature (*)			145		°C

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.

Fig. 1 - Quiescent output voltage vs. supply voltage

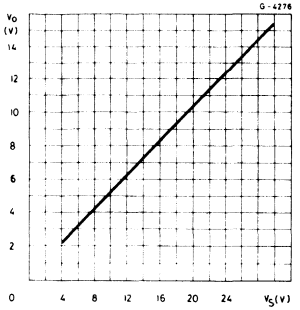


Fig. 2 - Quiescent drain current vs. supply voltage

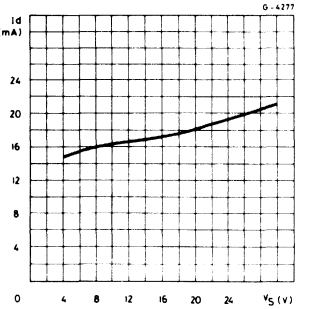


Fig. 3 - Output power vs. supply voltage

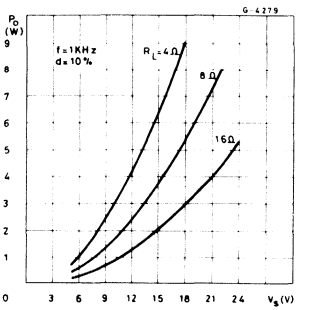


Fig. 4 - Distortion vs. output power ($R_L = 16\Omega$)

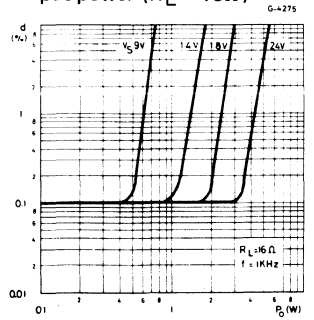


Fig. 5 - Distortion vs. output power ($R_L = 8\Omega$)

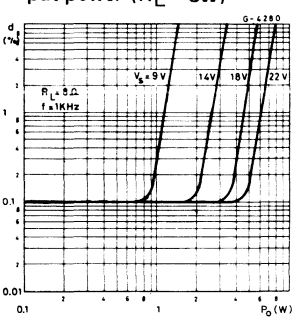


Fig. 6 - Distortion vs. output power ($R_L = 4\Omega$)

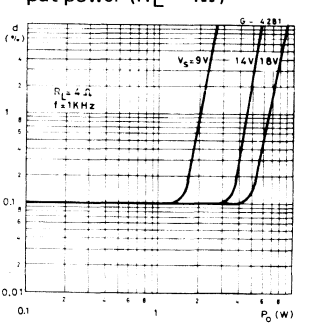


Fig. 7 - Distortion vs. frequency ($R_L = 16\Omega$)

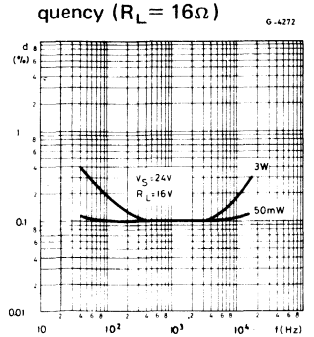


Fig. 8 - Distortion vs. frequency ($R_L = 8\Omega$)

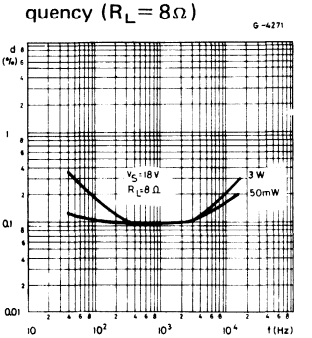


Fig. 9 - Distortion vs. frequency ($R_L = 4\Omega$)

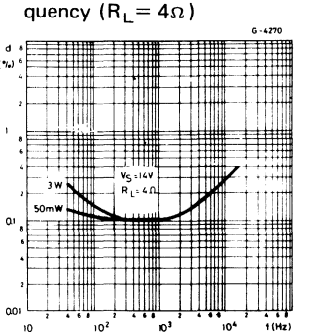


Fig. 10 - Open loop frequency response

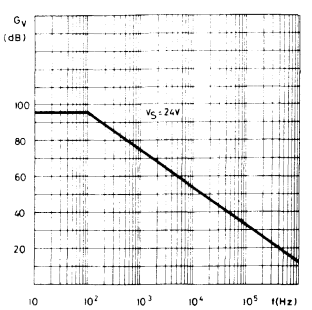


Fig. 11 - Output power vs. input voltage

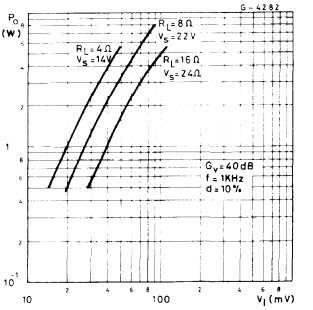


Fig. 12 - Values of capacitor C_X versus gain and B_W

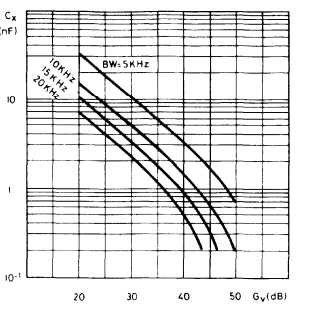


Fig. 13 - Supply voltage rejection vs. voltage gain

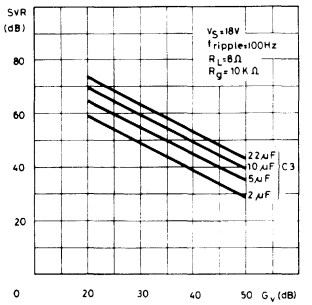


Fig. 14 - Supply voltage rejection vs. source resistance

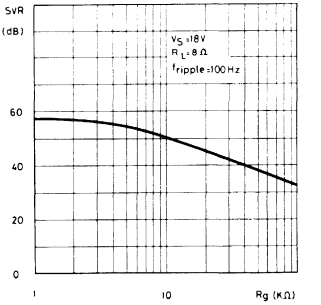


Fig. 15 - Max power dissipation vs. supply voltage

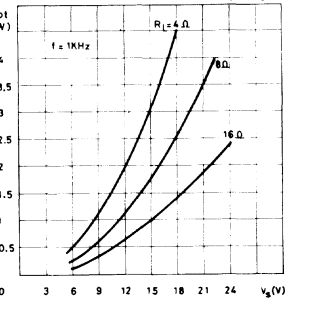


Fig. 16 - Power dissipation and efficiency vs. output power (V_S = 14V)

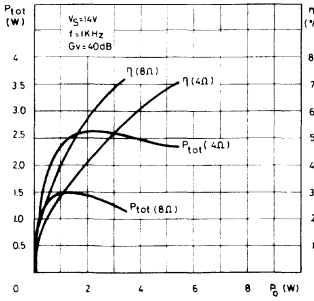


Fig. 17 - Power dissipation and efficiency vs. output power (V_S = 18V)

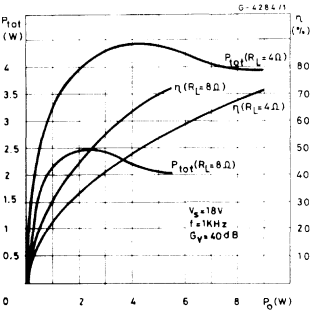
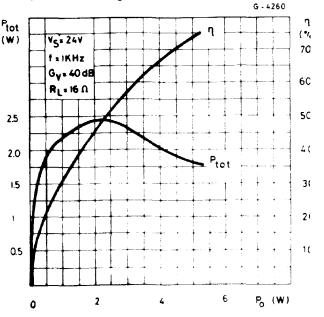
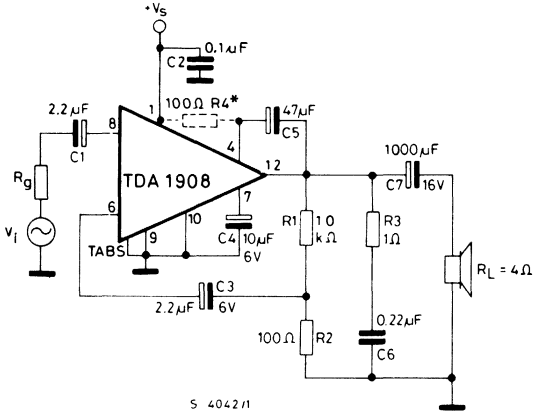


Fig. 18 - Power dissipation and efficiency vs. output power (V_S = 24V)



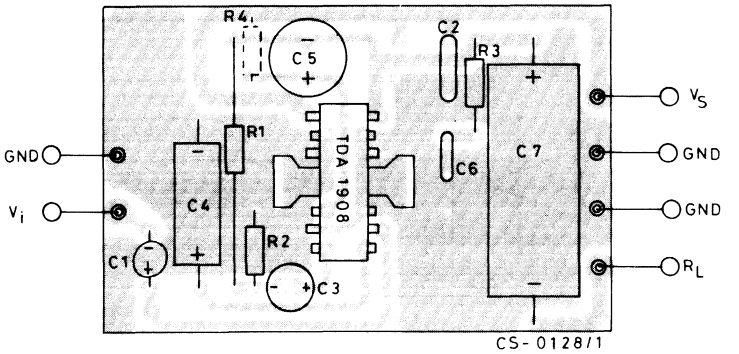
APPLICATION INFORMATION

Fig. 19 - Application circuit with bootstrap



* R4 is necessary when V_s is less than 10V.

Fig. 20 - P.C. board and component lay-out of the circuit of fig. 19 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 21 - Application circuit without bootstrap

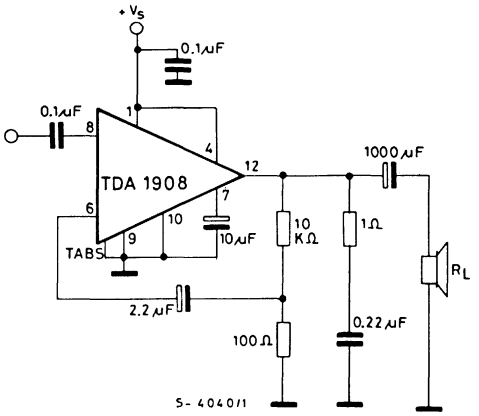


Fig. 22 - Output power vs. supply voltage (circuit of fig. 21)

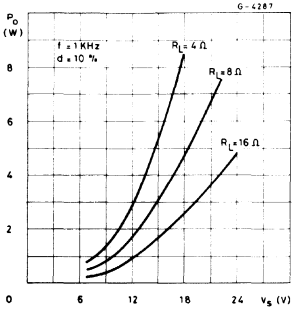
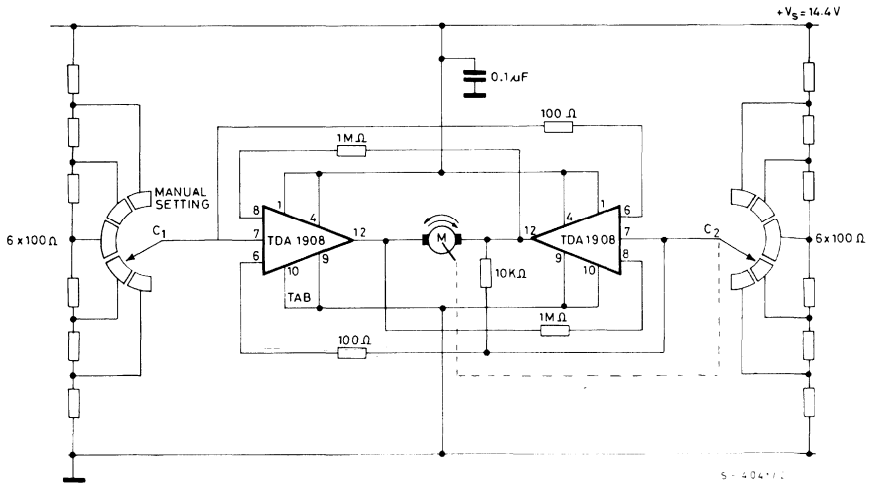


Fig. 23 - Position control for car headlights



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 19.
When the supply voltage V_s is less than 10V, a 100Ω resistor must be connected between pin 1 and pin 4 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Component	Raccom. value	Purpose	Larger than raccomanded value	Smaller than raccomanded value	Allowed range	
					Min.	Max.
R_1	10 KΩ	Close loop gain setting.	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R_2	
R_2	100 Ω	Close loop gain setting.	Decrease of gain.	Increase of gain.		$R_1/9$
R_3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R_4	100 Ω	Increasing of output swing with low V_s.			47Ω	330Ω
C_1	2.2 μF	Input DC decoupling.	Lower noise	Higher low frequency cutoff. Higher noise.	0.1 μF	
C_2	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C_3	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise	Higher low frequency cutoff.	0.1 μF	
C_4	10 μF	Ripple Rejection.	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.	2.2 μF	100 μF
C_5	47 μF	Bootstrap		Increase of the distortion at low frequency	10 μF	100 μF
C_6	0.22 μF	Frequency stability.		Danger of oscillation.		
C_7	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If, for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 26 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 24 - Output power and drain current vs. case temperature

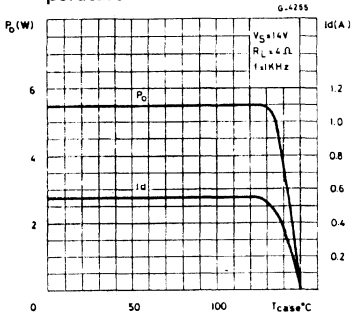


Fig. 25 - Output power and drain current vs. case temperature

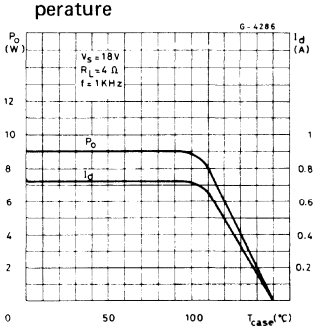
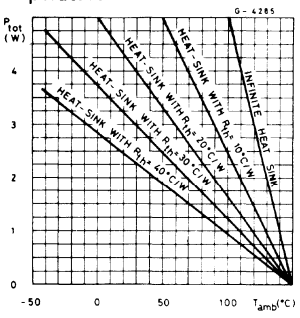


Fig. 26 - Maximum power dissipation vs. ambient temperature



MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by soldering the tabs to a copper area on the PC board (see Fig. 27).

During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 27 - Mounding example

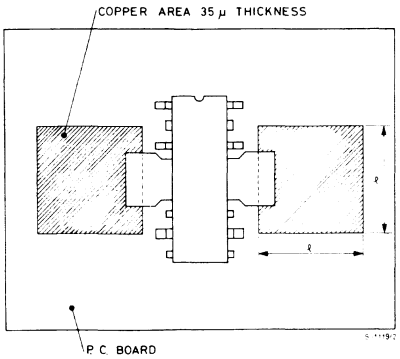
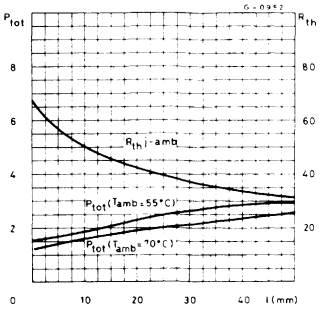


Fig. 28 - Maximum power dissipation and thermal resistance vs. side "ℓ"



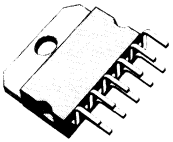
TDA1910

10W AUDIO AMPLIFIER WITH MUTING

The TDA 1910 is a monolithic integrated circuit in MULTIWATT® package, intended for use in Hi-Fi audio power applications, **as high quality TV sets.**

The TDA 1910 meets the DIN 45500 (d = 0.5%) guaranteed output power of 10W when used at 24V/4Ω. At 24V/8Ω the output power is 7W min. Features:
- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise.

The TDA 1910 is assembled in MULTIWATT® package that offers:
- easy assembly
- simple heatsink
- space and cost saving
- high reliability.



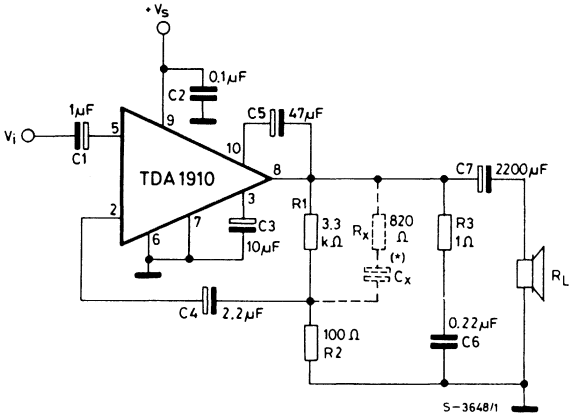
Multiwatt 11

ORDERING NUMBER: TDA 1910

ABSOLUTE MAXIMUM RATINGS

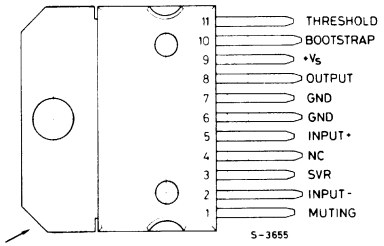
V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3.5	A
I_o	Output peak current (repetitive)	3.0	A
V_i	Input voltage	0 to + V_s	V
V_i	Differential input voltage	± 7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST CIRCUIT



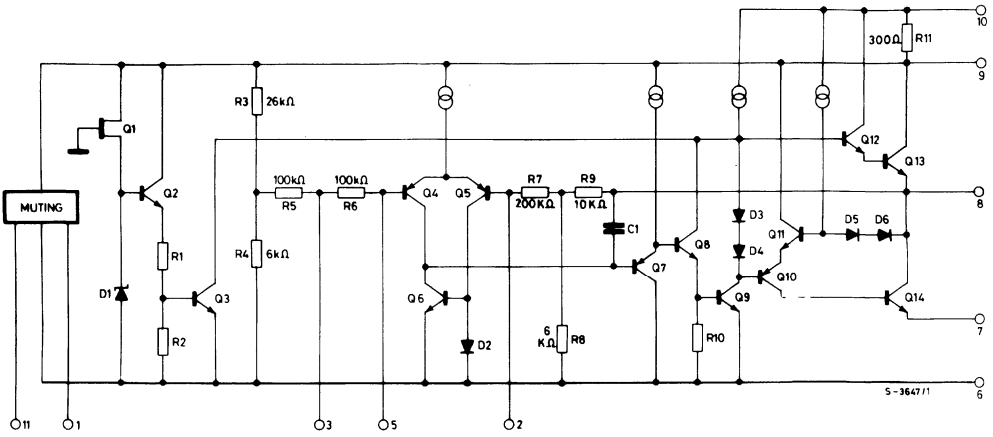
(*) See fig. 13.

CONNECTION DIAGRAM (Top view)

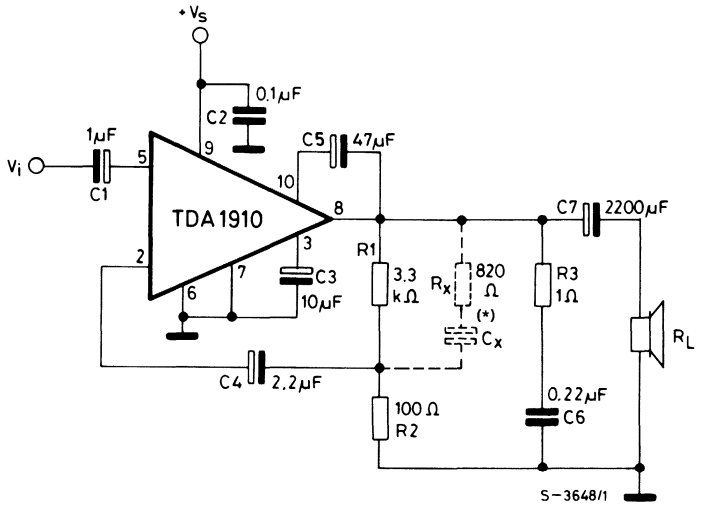


tab connected to pin 6

SCHEMATIC DIAGRAM

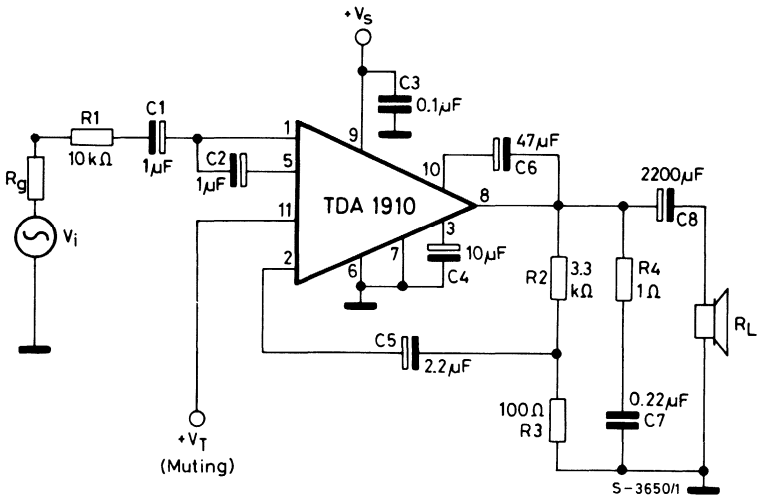


TEST CIRCUIT



(*) See fig. 13.

MUTING CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, R_{th} (heatsink) = 4°C/W, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		30	V
V_o	Quiescent output voltage	V_s = 18V V_s = 24V	8.3 11.5	9.2 12.4	10 13.4	V
I_d	Quiescent drain current	V_s = 18V V_s = 24V		19 21	32 35	mA
$V_{CE\ sat}$	Output stage saturation voltage	I_C= 2A		1		V
		I_C= 3A		1.6		
P_o	Output power	d = 0.5% f = 40 to 15,000Hz V_s = 18V R_L= 4Ω V_s = 24V R_L= 4Ω V_s = 24V R_L= 8Ω	 6.5 10 7	 7 12 7.5		W
		d = 10% f = 1 KHz V_s = 18V R_L= 4Ω V_s = 24V R_L= 4Ω V_s = 24V R_L= 8Ω	 8.5 15 9	 9.5 17 10		W
d	Harmonic distortion	f = 40 to 15,000 Hz V_s = 18V R_L= 4Ω P_o= 50 mW to 6.5W V_s= 24V R_L= 4Ω P_o= 50 mW to 10W V_s = 24V R_L= 8Ω P_o= 50 mW to 7W		 0.2 0.2 0.2	 0.5 0.5 0.5	%
d	Intermodulation distortion	V_s = 24V R_L= 4Ω P_o= 10W f_1= 250 Hz f_2= 8 KHz (DIN 45500)		0.2		%
V_i	Input sensitivity	f = 1 KHz V_s = 18V R_L= 4Ω P_o= 7W V_s = 24V R_L= 4Ω P_o= 12W V_s = 24V R_L= 8Ω P_o= 7.5W		 170 220 245		mV
V_i	Input saturation voltage (rms)	V_s = 18V V_s = 24V	1.8 2.4			V
R_i	Input resistance (pin 5)	f = 1 KHz	60	100		KΩ
I_d	Drain current	V_s = 24V f = 1 KHz R_L= 4Ω P_o= 12W R_L= 8Ω P_o= 7.5W		 820 475		mA

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test condition		Min.	Typ.	Max.	Unit
η	Efficiency	V_s = 24V f = 1 KHz R_L= 4Ω P_o= 12W R_L= 8Ω P_o= 7.5W			62 65		%
BW	Small signal bandwidth	V_s = 24V R_L= 4Ω P_o= 1W		10 to 120,000			Hz
BW	Power bandwidth	V_s = 24V R_L= 4Ω P_o = 12W d ≤ 0.5%		40 to 15,000			Hz
G_v	Voltage gain (open loop)	f = 1 KHz			75		dB
G_v	Voltage gain (closed loop)	V_s = 24V R_L= 4Ω f = 1 KHz P_o = 1W		29.5	30	30.5	dB
e_N	Total input noise		R_g = 50Ω R_g = 1KΩ (°) R_g = 10KΩ		1.2 1.3 1.5	3.0 3.2 4.0	μV
			R_g = 50Ω R_g = 1KΩ (°°) R_g = 10KΩ		2.0 2.0 2.2	5.0 5.2 6.0	μV
S/N	Signal to noise ratio	V_s = 24V P_o = 12W R_L= 4Ω	R_g = 10KΩ R_g = 0 (°)	97	103 105		dB
			R_g = 10KΩ R_g = 0 (°°)	93	100 100		dB
SVR	Supply voltage rejection	V_s = 24V R_L= 4Ω f_{ripple}= 100 Hz R_g= 10 KΩ		50	60		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot}= 8W		110	125		°C

MUTING FUNCTION (Refer to Muting circuit)

V_T	Muting-off threshold voltage (pin 11)			1.9		4.7	V
V_T	Muting-on threshold voltage (pin 11)			0		1.3	V
				6		V_s	
R_1	Input resistance (pin 1)	Muting off		80	200		KΩ
		Muting on			10	30	Ω
R_{11}	Input resistance (pin 11)			150			KΩ
A_T	Muting attenuation	$R_g + R_1$= 10 KΩ		50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 29 and fig. 30.

Fig. 1 - Quiescent output voltage vs. supply voltage

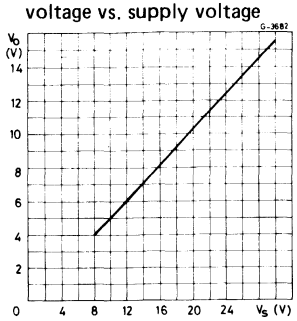


Fig. 2 - Quiescent drain current vs. supply voltage

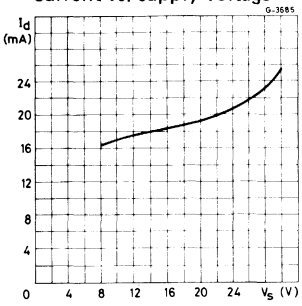


Fig. 3 - Open loop frequency response

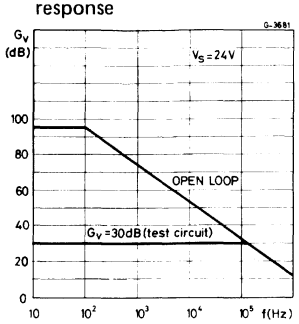


Fig. 4 - Output power vs. supply voltage

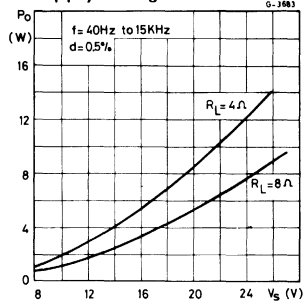


Fig. 5 - Output power vs. supply voltage

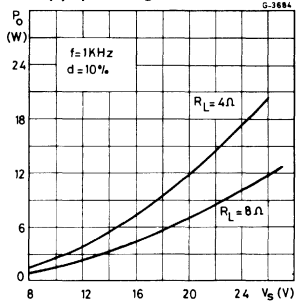


Fig. 6 - Distortion vs. output power

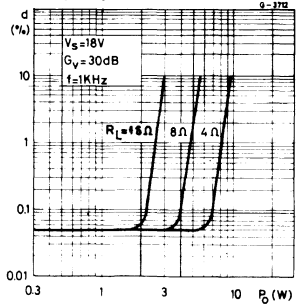


Fig. 7 - Distortion vs. output power

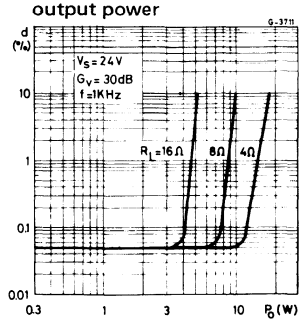


Fig. 8 - Output power vs. frequency

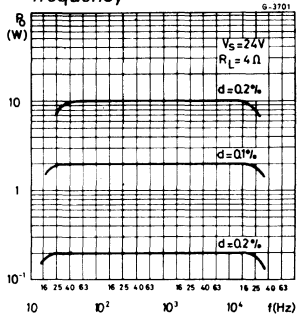


Fig. 9 - Output power vs. frequency

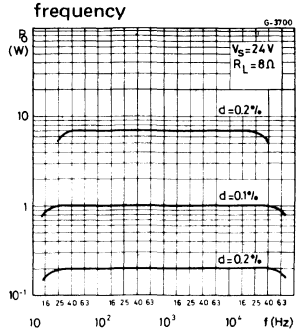


Fig. 10 - Output power vs. input voltage

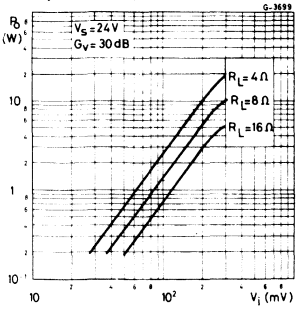


Fig. 11 - Output power vs. input voltage

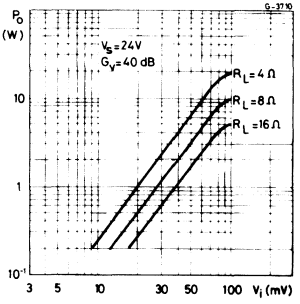


Fig. 12 - Total input noise vs. source resistance

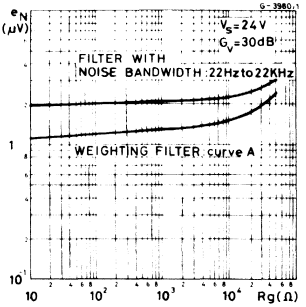


Fig. 13 - Values of capacitor C_X vs. bandwidth (BW) and gain (G_v)

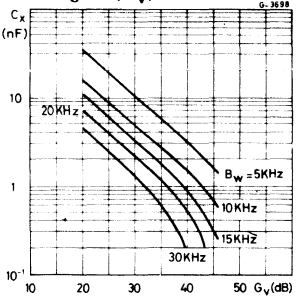


Fig. 14 - Supply voltage rejection vs. voltage gain

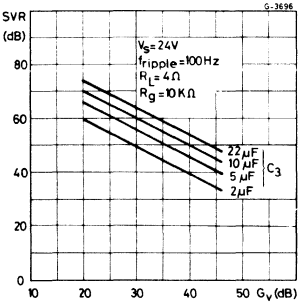


Fig. 15 - Supply voltage rejection vs. source resitance

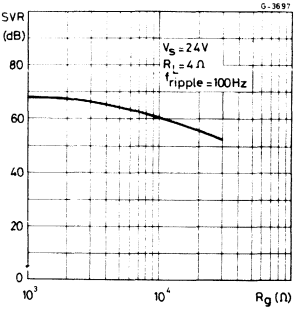


Fig. 16 - Power dissipation and efficiency vs. output power

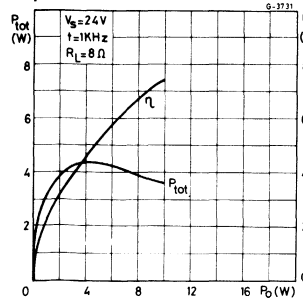


Fig. 17 - Power dissipation and efficiency vs. output power

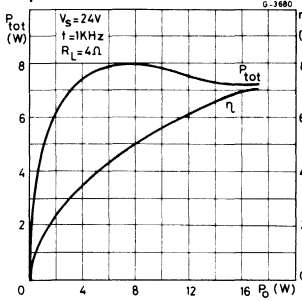
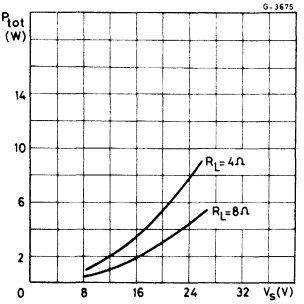


Fig. 18 - Max power dissipation vs. supply voltage



APPLICATION INFORMATION

Fig. 19 - Application circuit without muting

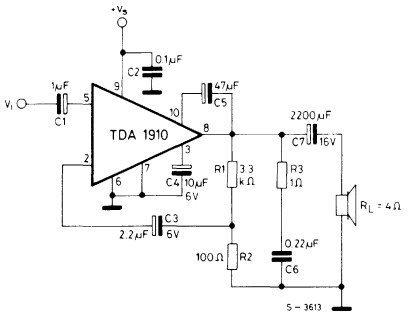


Fig. 20 - PC board and component lay-out of the circuit of fig. 19 (1:1 scale)

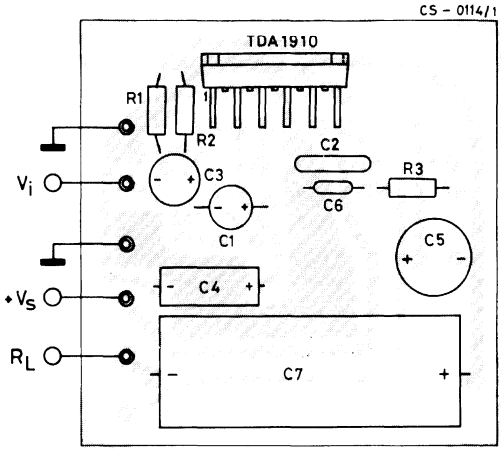
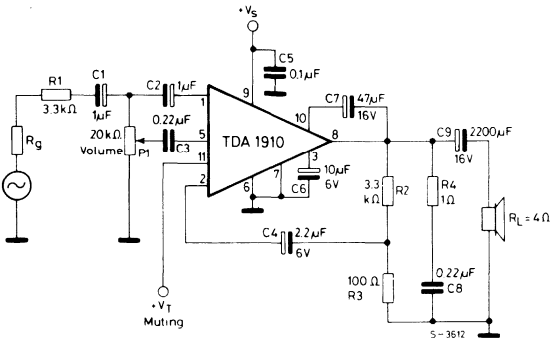


Fig. 21 - Application circuit with muting



Performance (circuits of fig. 19 and 21)

P_o = 12W (40 to 15000 Hz, d ⩽0.5%)
V_s = 24V
I_d = 0.82A
G_v = 30 dB

APPLICATION INFORMATION (continued)

Fig. 22 - Two position DC tone control (10 dB boost 50 Hz and 20 KHz) using change of pin 1 resistance (muting function)

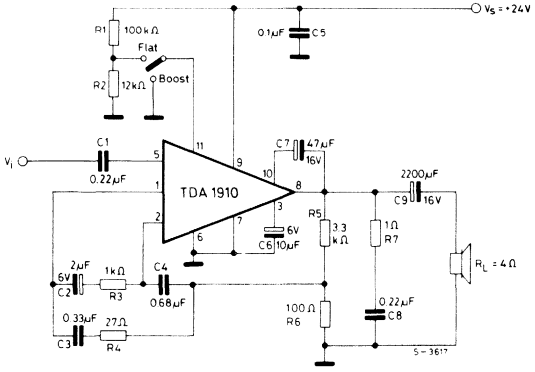


Fig. 23 - Frequency response of the circuit of fig. 22

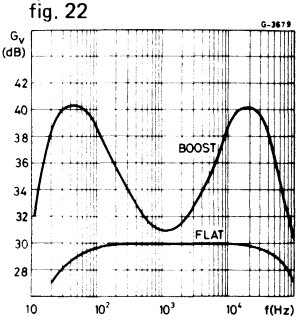


Fig. 24 - 10 dB 50 Hz boost tone control using change of pin 1 resistance (muting function)

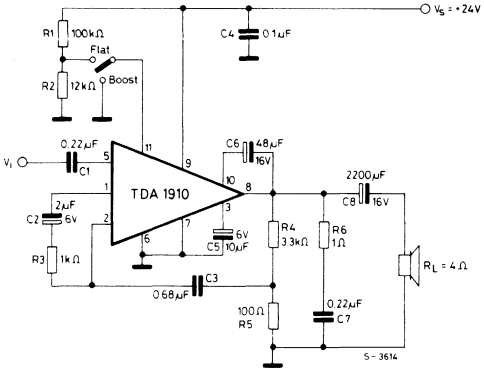


Fig. 25 - Frequency response of the circuit of fig. 24

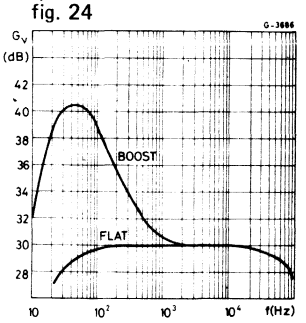


Fig. 26 - Squelch function in TV applications

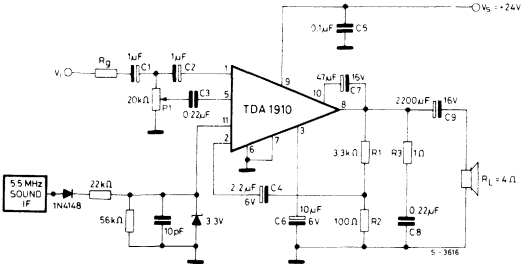
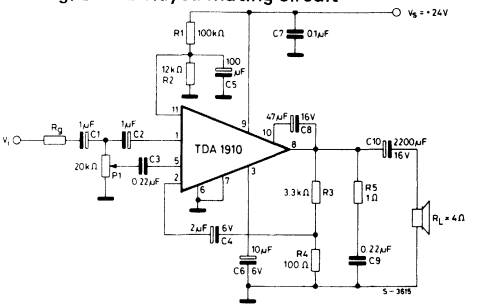


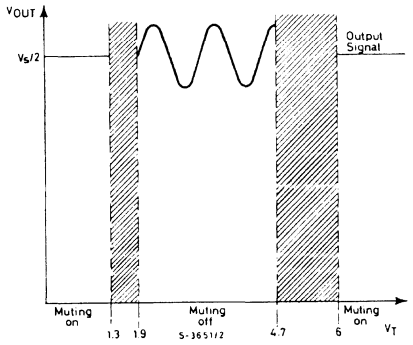
Fig. 27 - Delayed muting circuit



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 11, as shown in fig. 28

Fig. 28

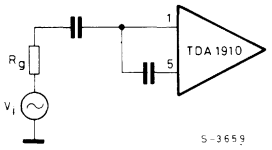


The input resistance at pin 1 depends on the threshold voltage V_T at pin 11 and is typically.

$R_1 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_1 = 10\ \Omega$ @ $0V \leqslant V_T \leqslant 1.3V$, $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression.



$$A_T = \frac{V_i}{V_5} = \frac{R_g + R_5//R_1}{R_5//R_1}$$

where $R_5 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, typically 1.2 dB.
A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 11 is greater than 150 KΩ. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 27)
- during commutations at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 1 can be useful in many applications and we have shown 2 examples in fig. 22 and 24, where it has been used to change the feedback network, obtaining 2 different frequency responses.

APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 21. Different values can be used.
The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range	
					Min.	Max.
$R_g + R_1$	10KΩ	Input signal imped. for muting operation	Increase of the attenuation in muting-on condition.Decrease of the input sensitivity.	Decrease of the attenuation in muting on condition.		
R_2	3.3KΩ	Close loop gain setting.	Increase of gain.	Decrease of gain. Increase quiescent current.	$9\,R_3$	
R_3	100Ω	Close loop gain setting.	Decrease of gain.	Increase of gain.		$R_2/9$
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
P_1	20KΩ	Volume potentiometer.	Increase of the switch-on noise.	Decrease of the input impedance and the input level.	10KΩ	100KΩ
C_1 C_2 C_3	1 μF 1 μF 0.22 μF	Input DC decoupling.		Higher low frequency cutoff.		
C_4	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise.	Higher low frequency cutoff.	0.1 μF	
C_5	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C_6	10 μF	Ripple Rejection.	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.	2.2 μF	100 μF
C_7	47 μF	Bootstrap.		Increase of the distortion at low frequency.	10 μF	100 μF
C_8	0,22 μF	Frequency stability.		Danger of oscillation.		
C_9	2200 μF (R_L= 4Ω) 1000 μF (R_L= 8Ω)	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 31 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 29 - Output power and drain current vs. case temperature

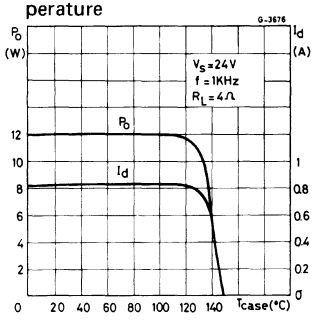


Fig. 30 - Output power and drain current vs. case temperature

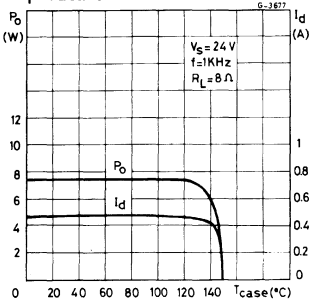
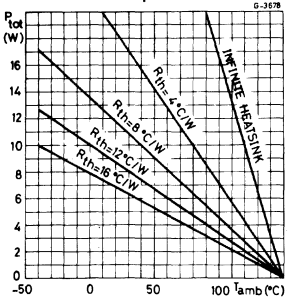


Fig. 31 - Maximum allowable power dissipation vs. ambient temperature



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

TDA2002

NOT FOR NEW DESIGN

8W CAR RADIO AUDIO AMPLIFIER

The TDA2002 is a class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 1.6Ω).

The device provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion.

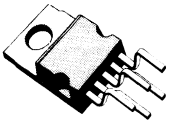
In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use

Protection against:

a) short circuit;
b) thermal over range;
c) fortuitous open ground;
d) load dump voltage surge.

See TDA2003 for more complete information.



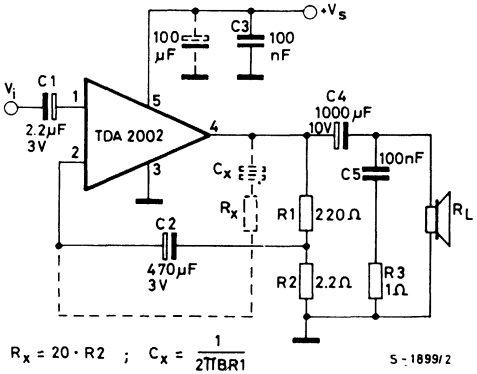
Pentawatt

ORDER CODE: TDA2002H (Hor. Pentawatt)
TDA2002V (Ver. Pentawatt)

ABSOLUTE MAXIMUM RATINGS

V_s	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	18	V
I_o	Output peak current (repetitive)	3.5	A
I_o	Output peak current (non repetitive)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	15	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Fig. 1 - Application circuit



ELECTRICAL CHARACTERISTICS (V_s= 14.4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS (Refer to DC test circuit)						
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage (pin 4)		6.4	7.2	8	V
I_d	Quiescent drain current (pin 5)			45	80	mA
AC CHARACTERISTICS (Refer to AC test circuit, G_v= 40 dB)						
P_o	Output power	d = 10% f = 1 kHz R_L= 4Ω R_L= 2Ω V_s = 16V R_L= 4Ω R_L= 2Ω	4.8 7	5.2 8 6.5 10		W W W W
$V_{i(rms)}$	Input saturation voltage		600			mV
V_i	Input sensitivity	f = 1 kHz P_o = 0.5W R_L= 4Ω P_o = 0.5W R_L= 2Ω P_o = 5.2W R_L= 4Ω P_o= 8W R_L= 2Ω		15 11 55 50		mV mV mV mV
B	Frequency response (-3 dB)	R_L= 4Ω P_o= 1W	40 to 15 000			Hz
d	Distortion	f = 1 kHz P_o = 0.05 to 3.5W R_L= 4Ω P_o = 0.05 to 5W R_L= 2Ω		0.2 0.2		% %
R_i	Input resistance (pin 1)	f = 1 kHz	70	150		kΩ
G_V	Voltage gain (open loop)	R_L= 4Ω f = 1 kHz		80		dB
G_V	Voltage gain (closed loop)	R_L= 4Ω f = 1 kHz	39.5	40	40.5	dB
e_N	Input noise voltage (*)			4		μV
i_N	Input noise current (*)			60		pA
η	Efficiency	f = 1 kHz P_o = 5.2W R_L= 4Ω P_o = 8W R_L= 2Ω		68 58		% %
SVR	Supply voltage rejection	R_L= 4Ω R_g= 10 kΩ f_{ripple}= 100 Hz	30	35		dB

(*) Filter with noise bandwidth: 22 Hz to 22 KHz.

TDA2003

10W CAR RADIO AUDIO AMPLIFIER

The TDA 2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002, very low number of external components, ease of assembly, space and cost saving, are maintained.
The device provides a high output current capability (up to 3.5A) very low harmonic and cross-over distortion.
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range, load dump voltage surge up to 40V and fortuitous open ground.

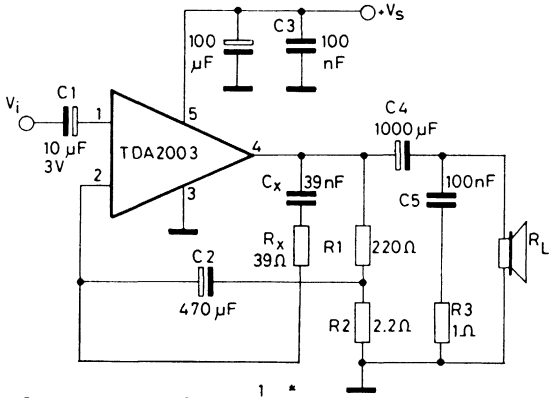
Pentawatt

ORDERING NUMBERS: TDA 2003H
TDA 2003V

ABSOLUTE MAXIMUM RATINGS

V_s	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	18	V
I_o	Output peak current (repetitive)	3.5	A
I_o	Output peak current (non repetitive)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

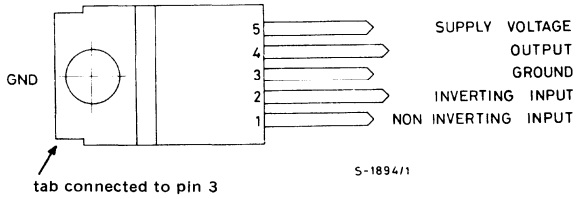
TEST CIRCUIT



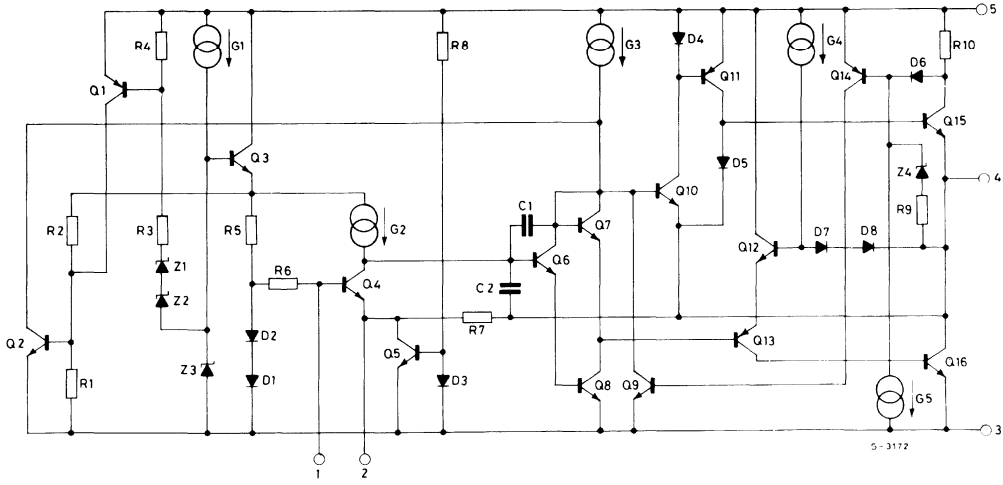
$R_x = 20 \cdot R2$; $C_x = \frac{1}{2\pi BR1}$ *

S - 3205

CONNECTION DIAGRAM
(top view)



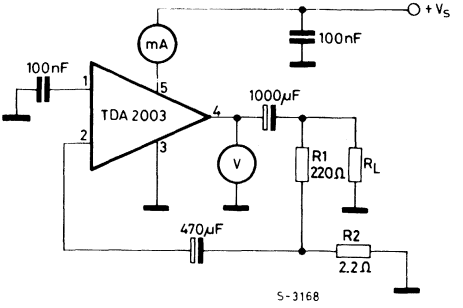
SCHEMATIC DIAGRAM



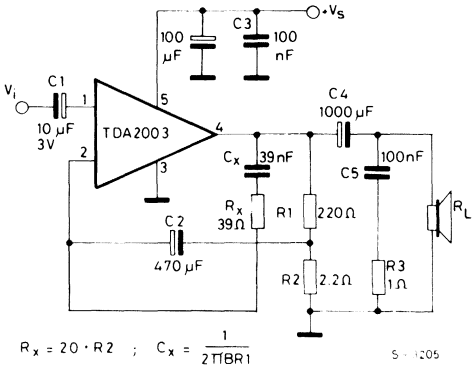
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

DC TEST CIRCUIT



AC TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_s= 14.4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS (Refer to DC test circuit)							
V_s	Supply voltage			8		18	V
V_o	Quiescent output voltage (pin 4)			6.1	6.9	7.7	V
I_d	Quiescent drain current (pin 5)				44	50	mA
AC CHARACTERISTICS (Refer to AC test circuit, G_v= 40 dB)							
P_o	Output power	d = 10% f = 1 kHz	R_L= 4Ω R_L= 2Ω R_L= 3.2Ω R_L= 1.6Ω	5.5 9	6 10 7.5 12		W W W W
$V_{i(rms)}$	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 kHz P_o = 0.5W P_o = 6W P_o = 0.5W P_o = 10W	 R_L= 4Ω R_L= 4Ω R_L= 2Ω R_L= 2Ω		 14 55 10 50		 mV mV mV mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
B	Frequency response (-3 dB)	P_o = 1W R_L = 4Ω		40 to 15,000		Hz
d	Distortion	f = 1 kHz P_o = 0.05 to 4.5W R_L = 4Ω P_o = 0.05 to 7.5W R_L = 2Ω		0.15 0.15		% %
R_i	Input resistance (pin 1)	f = 1 kHz	70	150		kΩ
G_v	Voltage gain (open loop)	f = 1 kHz f = 10 kHz		80 60		dB dB
G_v	Voltage gain (closed loop)	f = 1 kHz R_L = 4Ω	39.3	40	40.3	dB
e_N	Input noise voltage (0)			1	5	μV
i_N	Input noise current (0)			60	200	pA
η	Efficiency	f = 1 kHz P_o = 6W R_L = 4Ω P_o = 10W R_L = 2Ω		69 65		% %
SVR	Supply voltage rejection	f = 100 Hz V_{ripple} = 0.5V R_g = 10 kΩ R_L = 4Ω	30	36		dB

(0) Filter with noise bandwidth: 22 Hz to 22 kHz

Fig. 1 - Quiescent output voltage vs. supply voltage

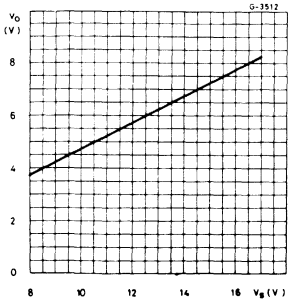


Fig. 2 - Quiescent drain current vs. supply voltage

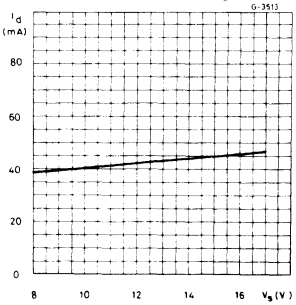


Fig. 3 - Output power vs. supply voltage

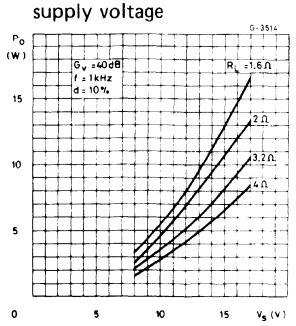


Fig. 4 - Output power vs. load resistance R_L

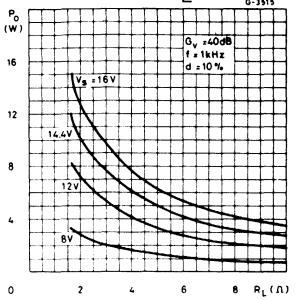


Fig. 5 - Gain vs. input sensitivity

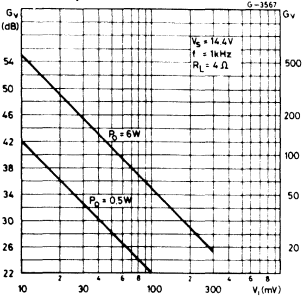


Fig. 6 - Gain vs. input sensitivity

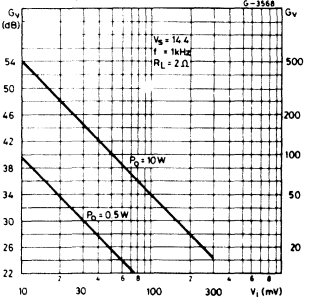


Fig. 7 - Distortion vs. output power

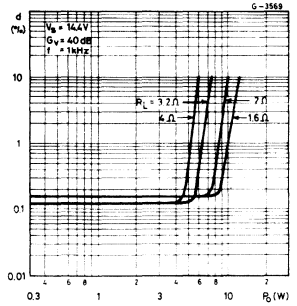


Fig. 8 - Distortion vs. frequency

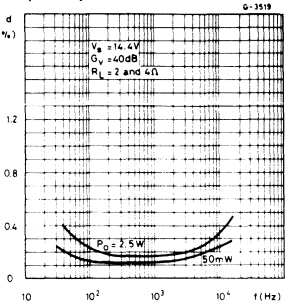


Fig. 9 - Supply voltage rejection vs. voltage gain

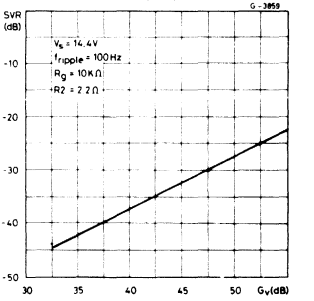


Fig. 10 - Supply voltage rejection vs. frequency

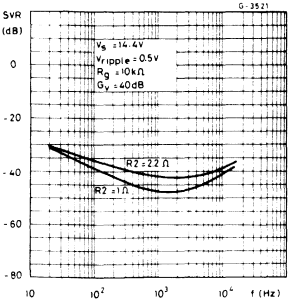


Fig. 11 - Power dissipation and efficiency vs. output power ($R_L = 4\Omega$)

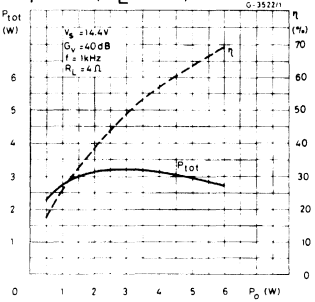


Fig. 12 - Power dissipation and efficiency vs. output power ($R_L = 2\Omega$)

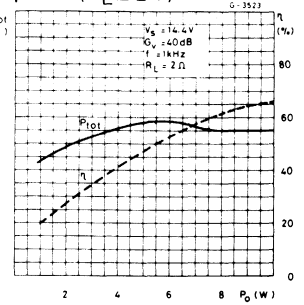


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

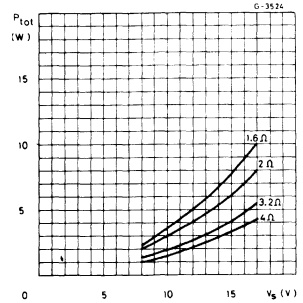


Fig. 14 - Maximum allowable power dissipation vs. ambient temperature

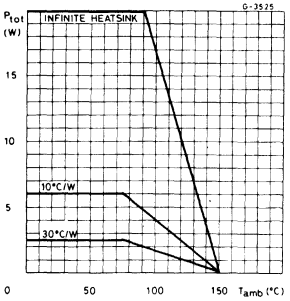
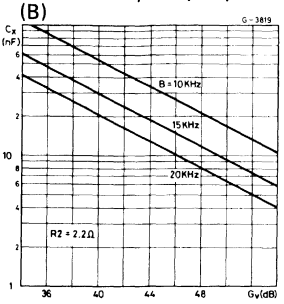


Fig. 15 - Typical values of capacitor (C_X) for different values of frequency response (B)



APPLICATION INFORMATION

Fig. 16 - Typical application circuit

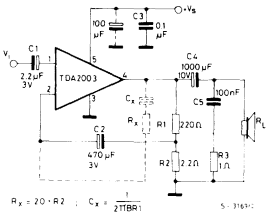


Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)

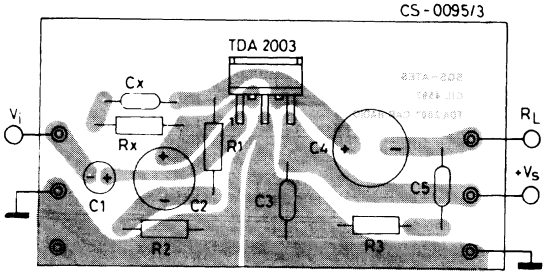
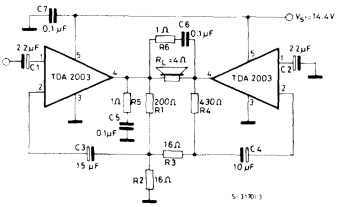
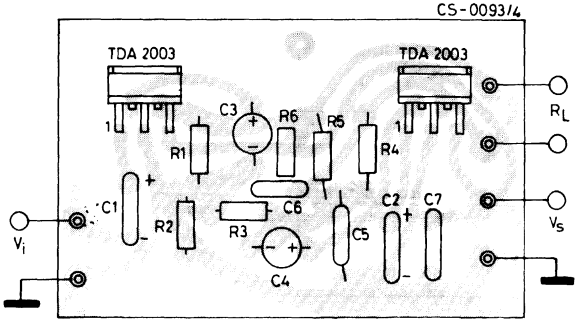


Fig. 18 - 20W bridge configuration application circuit (*)



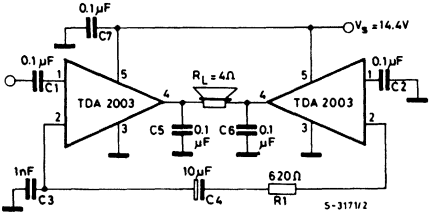
(*) The values of the capacitors C3 and C4 are different to optimize the SVR (Typ.= 40 dB)

Fig. 19 - P.C. board and component layout for the circuit of fig. 18 (1:1 scale)



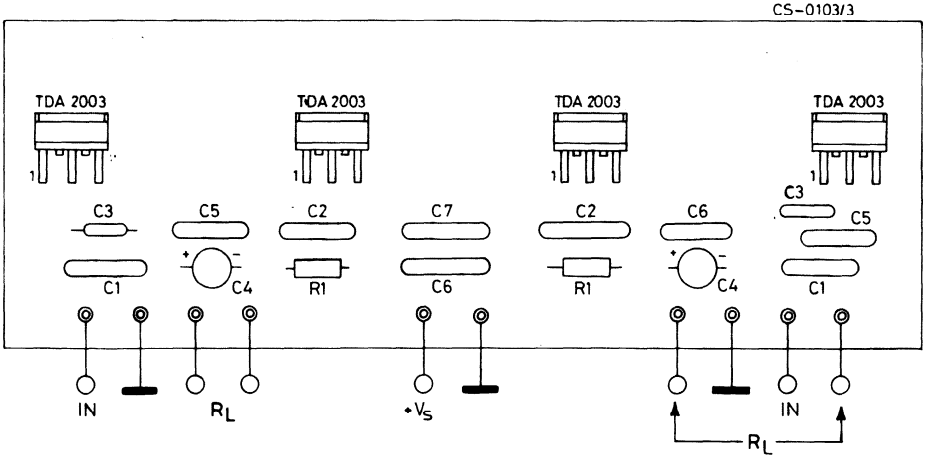
APPLICATION INFORMATION (continued)

Fig. 20 - Low cost bridge configuration application circuit (*) (P_o = 18W)



(*) In this application the device can support a short circuit between every side of the loudspeaker and ground.

Fig. 21 - P.C. board and component layout for the low-cost bridge amplifier of fig. 20, in stereo version (1:1 scale)



BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA 2003 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 23.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 22.

A suggested LC network is shown in fig. 23. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 22

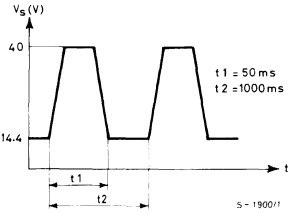
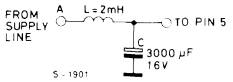


Fig. 23



Short-circuit (AC and DC conditions)

The TDA 2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1A fuse (normally connected in series with the supply).
This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2003 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA 2003 with inductive loads. In particular, the TDA 2003 can drive a coupling transformer for audio modulation.

DC voltage

The maximum operating DC voltage on the TDA 2003 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), oran excessive ambient temperature can be easily withstood.

2) the heat-sink can have a smaller factor compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

Fig. 24 - Output power and drain current vs. case temperature (R_L = 4 Ω)

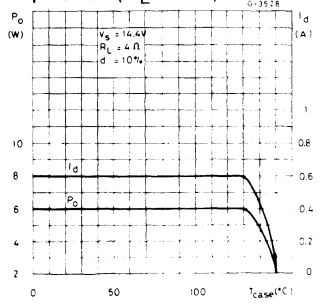
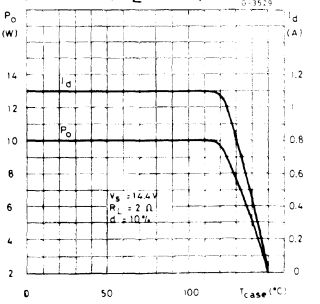


Fig. 25 - Output power and drain current vs. case temperature (R_L = 2Ω)



PRATICAL CONSIDERATION

Printed circuit board

The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion

No electrical insulation is required between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions

The recommended component values are those sjown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_X	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(G_V-1) \cdot R2$	Setting of gain		Increase of drain current
R2	2.2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_X	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

TDA2004

10 + 10W STEREO AMPLIFIER FOR CAR RADIO

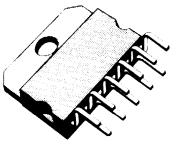
The TDA2004 is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio applications; stereo amplifiers are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6Ω).

Its main features are:

Low distortion.
Low noise.
High reliability of the chip and of the package with additional safety during operation thanks to protections against:

- output AC short circuit to ground;
- very inductive loads
- overrating chip temperature;
- load dump voltage surge;
- fortuitous open ground;

Space and cost saving: very low number of external components. very simple mounting system with no electrical isolation between the package and the heatsink.



Multiwatt-11

ORDERING NUMBER: TDA2004

ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Output peak current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Output peak current (repetitive f ⩾ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 60°C	30	W
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

(*) The max. output current is internally limited.

CONNECTION DIAGRAM

(Top view)

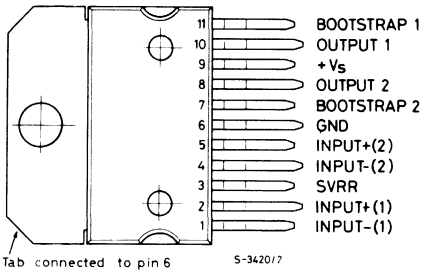


Fig. 1 - Test and application circuit

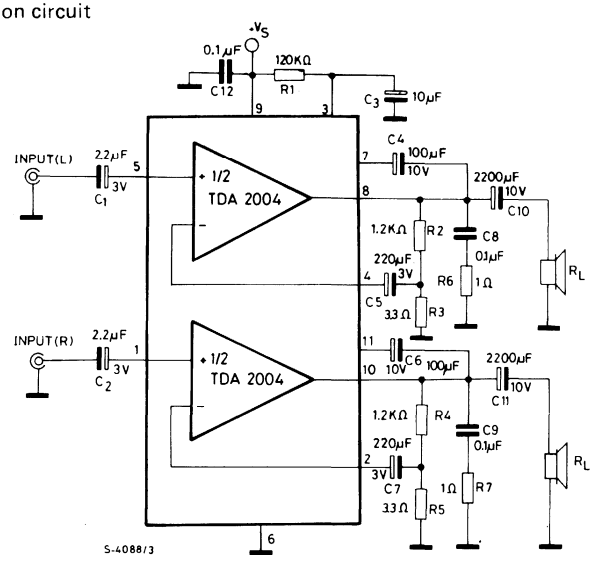
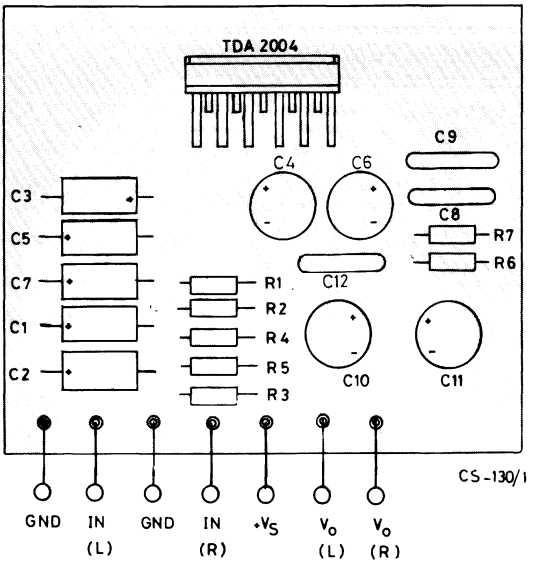


Fig. 2 - PC board and components layout (scale 1:1)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage	V_s = 14.4V V_s = 13.2V	6.6 6.0	7.2 6.6	7.8 7.2	V V
I_d	Total quiescent drain current	V_s = 14.4V V_s = 13.2V		65 62	120 120	mA mA
I_{SB}	Stand-by current	Pin 3 grounded		5		mA
P_o	Output power (each channel)	f = 1 KHz d = 10% V_s = 14.4V R_L= 4Ω R_L= 3.2Ω R_L= 2Ω R_L= 1.6Ω V_s = 13.2V R_L= 3.2Ω R_L= 1.6Ω V_s = 16V R_L= 2 Ω	 6 7 9 10 6 9 	 6.5 8 10(*) 11 6.5 10 12	 	 W W W W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o= 50 mW to 4W V_s = 14.4V R_L= 2Ω P_o= 50 mW to 6W V_s = 13.2V R_L= 3.2Ω P_o= 50 mW to 3W V_s = 13.2V R_L= 1.6Ω P_o= 50 mW to 6W		 0.2 0.3 0.2 0.3	 1 1 1 1	 % % % %
CT	Cross talk	V_s = 14.4V V_o= 4 V_{rms} R_L= 4Ω f = 1 KHz f = 10 KHz R_g = 5 KΩ	 50 40	 60 45	 	 dB dB
V_i	Input saturation voltage		300			mV
R_i	Input resistance (non inverting input)	f = 1 KHz	70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 4Ω R_L= 2Ω R_L= 3.2Ω R_L= 1.6Ω			35 50 40 55	Hz Hz Hz Hz
f_H	High frequency roll off (-3 dB)	R_L = 1.6Ω to 4Ω	15			KHz
G_v	Voltage gain (open loop)	f = 1 KHz		90		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
G_v	Voltage gain (closed loop)	f = 1 KHz	48	50	51	dB
	Closed loop gain matching			0.5		dB
e_N	Total input noise voltage	R_g= 10 KΩ(°)		1.5	5	μV
SVR	Supply voltage rejection	f_{ripple}= 100 Hz R_g= 10 KΩ C_3= 10 μF V_{ripple}=0.5V_{rms}	35	45		dB
η	Efficiency	V_s = 14.4V f = 1 KHz R_L= 4Ω P_o= 6.5W R_L= 2Ω P_o= 10W V_s = 13.2V f = 1 KHz R_L= 3.2Ω P_o= 6.5W R_L= 1.6Ω P_o= 10W		 70 60 70 60		 % % % %
T_j	Thermal shut down junction temperature			145		°C

(*) 9.3W without bootstrap.
(°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Quiescent output voltage vs. supply voltage

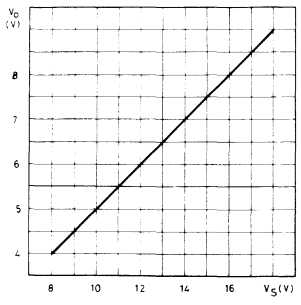


Fig. 4 - Quiescent drain current vs. supply voltage

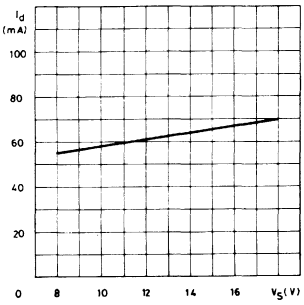


Fig. 5 - Distortion vs. output power

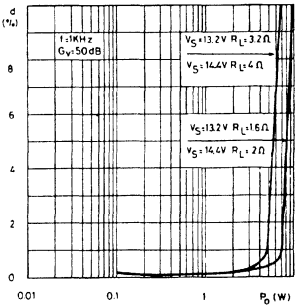


Fig. 6 - Output power vs. supply voltage

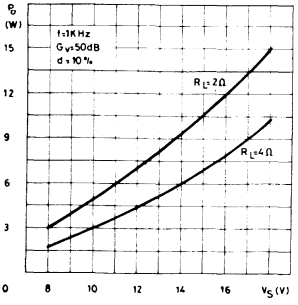


Fig. 7 - Output power vs. supply voltage

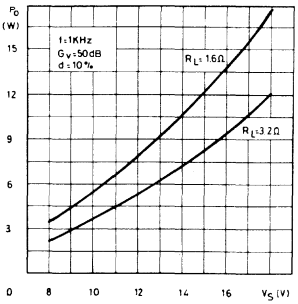


Fig. 8 - Distortion vs. frequency

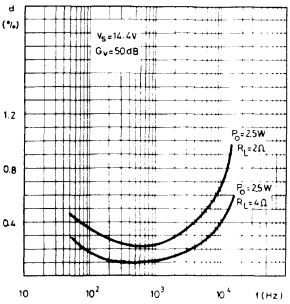


Fig. 9 - Distortion vs. frequency

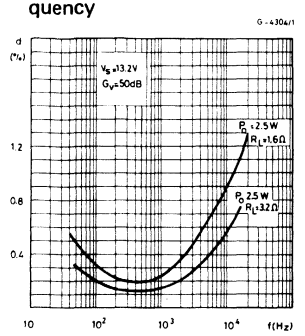


Fig. 10 - Supply voltage rejection vs. C_3

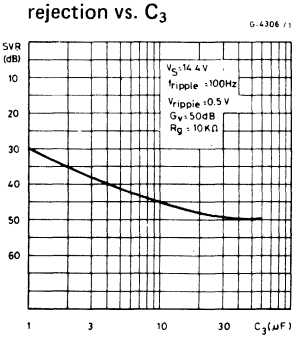


Fig. 11 - Supply voltage rejection vs. frequency

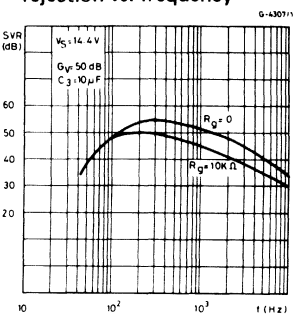


Fig. 12 - Supply voltage rejection vs. values of capacitors C_2 and C_3

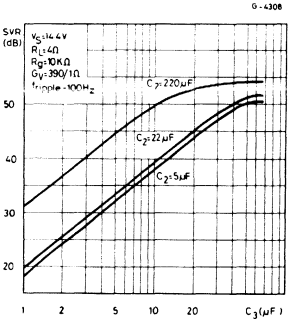


Fig. 13 - Supply voltage rejection vs. values of capacitors C_2 and C_3

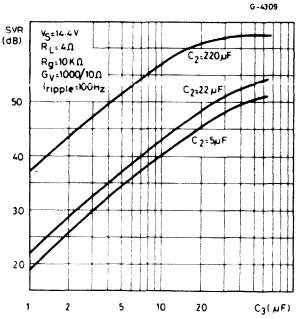


Fig. 14 - Gain vs. input sensitivity

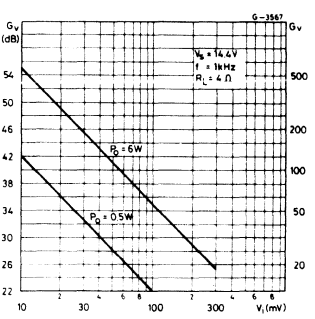


Fig. 15 - Maximum allowable power dissipation vs. ambient temperature

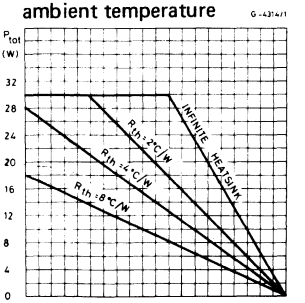


Fig. 16 - Total power dissipation and efficiency vs. output power

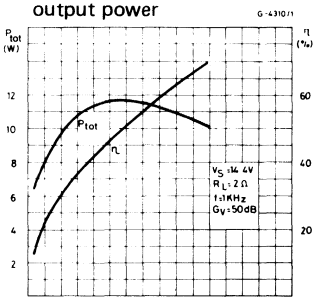
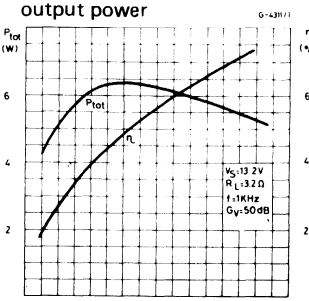


Fig. 17 - Total power dissipation and efficiency vs. output power



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R_1	120 KΩ	Optimisation of the output signal simmetry	Smaller $P_{o\ max}$	Smaller $P_{o\ max}$
R_2 and R_4	1 KΩ	Close loop gain setting (*)	Increase of gain	Decrease of gain
R_3 and R_5	3.3 Ω		Decrease of gain	Increase of gain
R_6 and R_7	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C_1 and C_2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise.
C_3	10 μF	Ripple rejection	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.
C_4 and C_6	100 μF	Bootstrapping		Increase of distortion at low frequency.
C_5 and C_7	100 μF	Feedback Input DC decoupling.		
C_8 and C_9	0.1 μF	Frequency stability.		Danger of oscillation.
C_{10} and C_{11}	1000 μF to 2200 μF	Output DC decoupling.		Higher low-frequency cut-off.

(*) The closed-loop gain must be higher than 26dB

BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA2004 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in Fig. 19.

If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in Fig. 18. With this network, a train of pulse with amplitude up to 120V and with of 2ms can be applied to point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

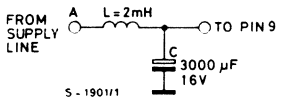
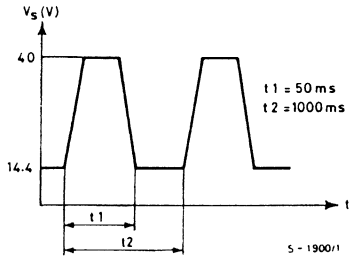


Fig. 19



Short circuit (AC conditions)

The TDA2004 can withstand an accidental short-circuit from the output to ground caused by a wrong connection during normal working.

Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2004 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided to allow use of the TDA2004 with inductive loads.

DC voltage

The maximum operating DC voltage on the TDA2004 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is the P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 20 shown this dissipable power as a function of ambient temperature for different thermal resistance.

TDA2005

20W BRIDGE AMPLIFIER FOR CAR RADIO

The TDA2005 is class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio application: **power booster amplifiers** are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6Ω in stereo applications) obtaining an output power of more than 20W (bridge configuration).

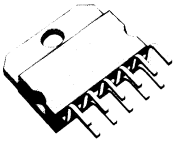
High output power: $P_o = 10 + 10W$ @ $R_L = 2\Omega$, $d = 10\%$; $P_o = 20W$ @ $R_L = 4\Omega$, $d = 10\%$.

High reliability of the chip and package with additional complete safety during operation thanks to protection against:

- output DC and AC short circuit to ground;
- overrating chip temperature
- load dump voltage surge
- fortuitous open ground
- very inductive loads

Flexibility in use: bridge or stereo booster amplifiers with or without boostrap and with programmable gain and bandwidth.

Space and cost saving: very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).
In addition, the circuit offers **loudspeaker protection** during short circuit for one wire to ground.



Multiwatt-11®

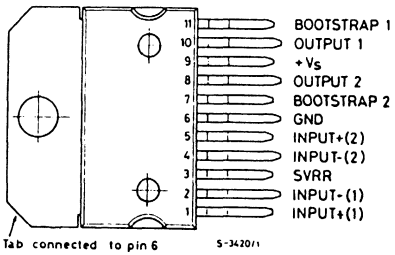
ORDERING NUMBERS:
TDA2005M - Bridge application
TDA2005S - Stereo application

ABSOLUTE MAXIMUM RATINGS

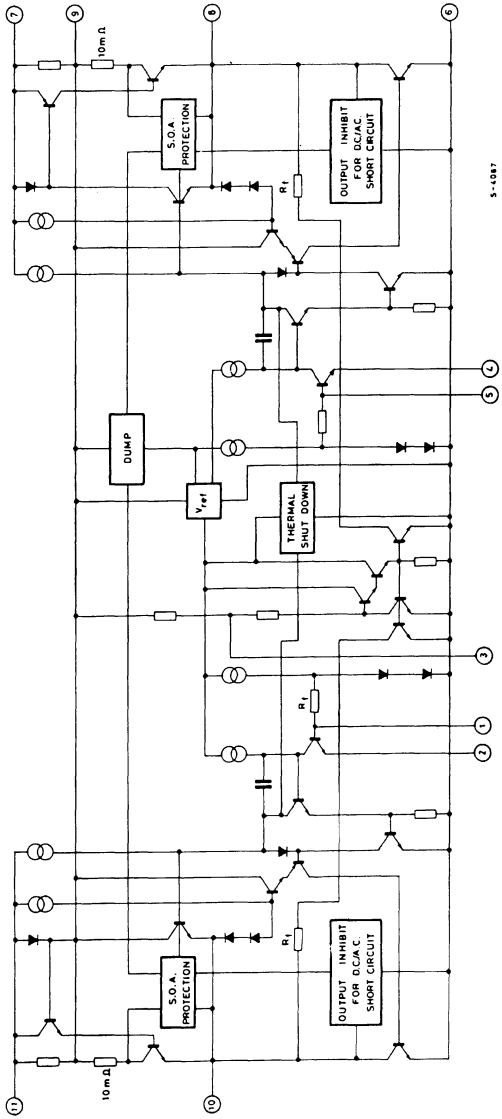
V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Output peak current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Output peak current (repetitive f ⩾ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 60°C	30	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

(*) The max. output current is internally limited.

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

BRIDGE AMPLIFIER APPLICATION (TDA 2005M)

Fig. 1 - Test and application circuit (Bridge amplifier)

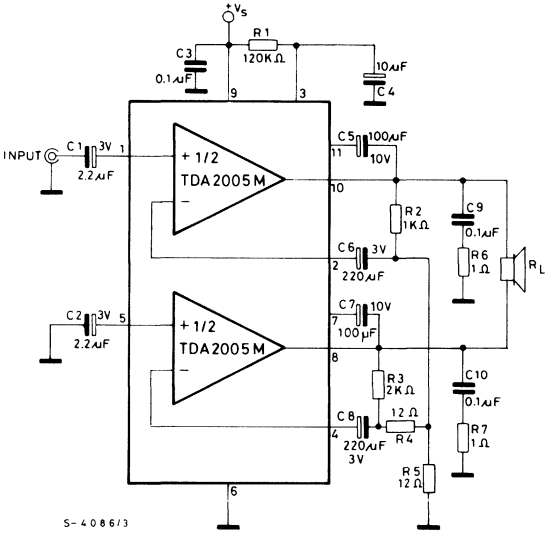
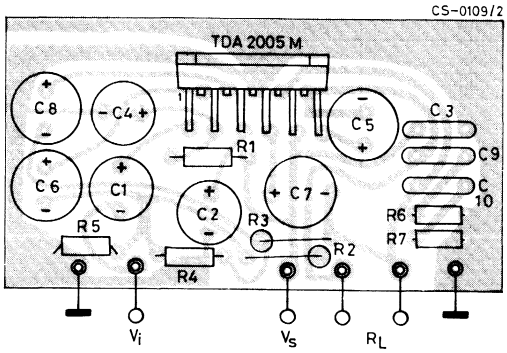


Fig. 2 - P.C. board and component layout (scale 1:1)



ELECTRICAL CHARACTERISTICS (Refer to the **bridge** application circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$= 4°C/W, unless otherwise specified).

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_{os}	Output offset voltage(°) (between pin 8 and 10)	V_s = 14.4V V_s = 13.2V			150 150	mV mV
I_d	Total quiescent drain current	V_s = 14.4V R_L= 4Ω		75	150	mA
		V_s = 13.2V R_L= 3.2 Ω		70	160	mA
P_o	Output power	d = 10% f = 1 KHz				
		V_s = 14.4V R_L= 4Ω	18	20		W
		R_L= 3.2Ω	20	22		W
		V_s = 13.2V R_L= 3.2Ω	17	19		W
d	Distortion	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o = 50 mW to 15W			1	%
		V_s = 13.2V R_L= 3.2Ω P_o = 50 mW to 13W			1	%
V_i	Input sensitivity	f = 1 KHz P_o = 2W R_L= 4Ω		9		mV
		P_o = 2W R_L= 3.2Ω		8		mV
R_i	Input resistance	f = 1 KHz	70			KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 3.2 Ω			40	Hz
f_H	High frequency roll off (-3 dB)	R_L= 3.2 Ω	20			KHz
G_v	Closed loop voltage gain	f = 1 KHz		50		dB
e_N	Total input noise voltage	R_g= 10 KΩ(°°)		3	10	μV
SVR	Supply voltage rejection	R_g= 10 KΩ C_4= 10 μF f_{ripple}= 100 Hz V_{ripple}= 0.5 V	45	55		dB
η	Efficiency	V_s = 14.4V f = 1 KHz P_o = 20W R_L= 4Ω		60		%
		P_o = 22W R_L= 3.2Ω		60		%
		V_s = 13.2V f = 1 KHz P_o = 19W R_L= 3.2Ω		58		%
T_j	Thermal shut-down junction temperature	V_s = 14.4V R_L= 4Ω f = 1 KHz P_{tot}= 13W		145		°C
V_{OSH}	Output voltage with one side of the speaker shorted to ground	V_s = 14.4V R_L= 4Ω V_s= 13.2V R_L= 3.2Ω			2	V

(°) For TDA 2005M only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Output offset voltage vs. supply voltage

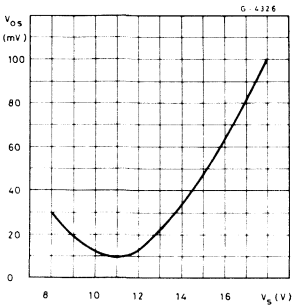


Fig. 4 - Distortion vs. output power (Bridge amplifier)

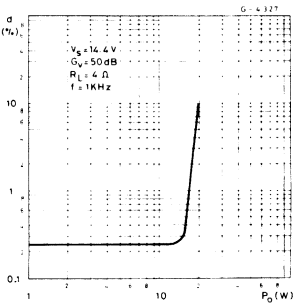
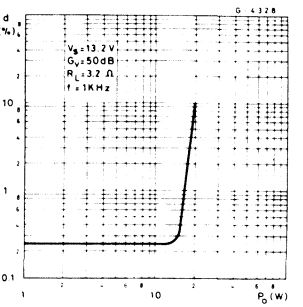


Fig. 5 - Distorsion vs. output power (Bridge amplifier)



BRIDGE AMPLIFIER DESIGN

The following considerations can be useful when designing a bridge amplifier.

Parameter		Single ended	Bridge
$V_{o\ max}$	Peak output voltage (before clipping)	$\frac{1}{2}(V_s - 2V_{CE\ sat})$	$V_s - 2V_{CE\ sat}$
$I_{o\ max}$	Peak output current (before clipping)	$\frac{1}{2}\frac{(V_s - 2V_{CE\ sat})}{R_L}$	$\frac{V_s - 2V_{CE\ sat}}{R_L}$
$P_{o\ max}$	rms output power (before clipping)	$\frac{1}{4}\frac{(V_s - 2V_{CE\ sat})^2}{2R_L}$	$\frac{(V_s - 2V_{CE\ sat})^2}{2R_L}$

where: $V_{CE\ sat}$ = output transistors saturation voltage
V_S = allowable supply voltage
R_L = load impedance.

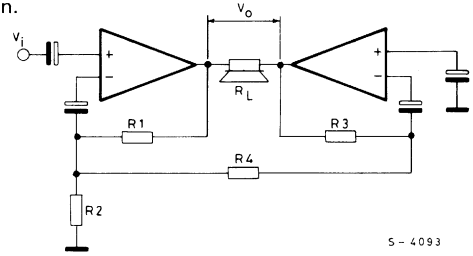
Voltage and current swings are twice for a bridge amplifier in comparison with single ended amplifier. In order words, with the same R_L the bridge configuration can deliver an output power that is four times the output power of a single ended amplifier, while, with the same max output current the bridge configuration can deliver an output power that is twice the output power of a single ended amplifier. Core must be taken when selecting V_s and R_L in order to avoid an output peak current above the absolute maximum rating.

From the expression for $I_{o\ max}$, assuming V_s = 14.4V and $V_{CE\ sat}$ = 2V, the minimum load that can be driven by TDA2005 in bridge configuration is:

$$R_{Lmin} = \frac{V_s - 2V_{CEsat}}{I_{o\ max}} = \frac{14.4 - 4}{3.5} = 2.97\ \Omega$$

BRIDGE AMPLIFIER DESIGN (continued)

Fig. 6 - Bridge configuration.



The voltage gain of the bridge configuration is given by (see fig. 6):

$$G_v = \frac{V_o}{V_i} = 1 + \frac{R_1}{\left(\frac{R_2 \cdot R_4}{R_2 + R_4}\right)} + \frac{R_3}{R_4}$$

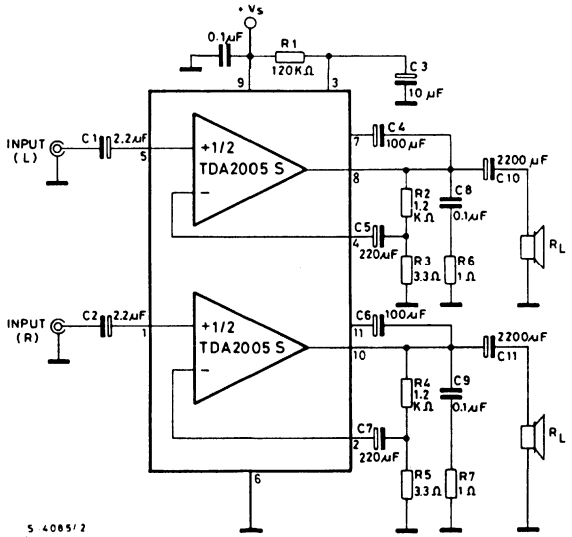
For sufficiently high gains (40 ÷ 50 dB) it is possible to put $R_2 = R_4$ and $R_3 = 2\,R_1$, simplifing the formula in:

$$G_v = 4\,\frac{R_1}{R_2}$$

G_v (dB)	R_1 (Ω)	$R_2 = R_4$ (Ω)	R_3 (Ω)
40	1000	39	2000
50	1000	12	2000

STEREO AMPLIFIER APPLICATION (TDA 2005S)

Fig. 7 - Typical application circuit



ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$= 4°C/W, unless otherwise specified).

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage	V_s = 14.4V V_s = 13.2V	6.6 6	7.2 6.6	7.8 7.2	V V
I_d	Total quiescent drain current	V_s = 14.4V V_s = 13.2V		65 62	120 120	mA mA
P_o	Output power (each channel)	f = 1 KHz d = 10% V_s = 14.4V R_L= 4Ω R_L= 3.2Ω R_L= 2Ω R_L= 1.6Ω V_s = 13.2V R_L= 3.2Ω R_L= 1.6Ω V_s = 16V R_L= 2Ω	 6 7 9 10 6 9	 6.5 8 10 11 6.5 10 12		 W W W W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o = 50 mW to 4W V_s = 14.4V R_L= 2Ω P_o = 50 mW to 6W V_s = 13.2V R_L= 3.2Ω P_o= 50 mW to 3W V_s = 13.2V R_L= 1.6Ω P_o = 40 mW to 6W		 0.2 0.3 0.2 0.3	 1 1 1 1	 % % % %
CT	Cross talk (°)	V_s= 14.4V R_L= 4Ω f = 1 KHz		60		dB
		V_o = 4V_{rms} R_g= 5 KΩ f = 10 KHz		45		dB
V_i	Input saturation voltage		300			mV
V_i	Input sensitivity	f = 1 KHz P_o = 1W R_L= 4Ω R_L= 3.2Ω		 6 5.5		mV
R_i	Input resistance	f = 1 KHz	70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 2Ω			50	Hz
f_H	High frequency roll off (-3 dB)	R_L= 2Ω	15			KHz
G_v	Voltage gain (open loop)	f = 1 KHz		90		dB
G_v	Voltage gain (closed loop)	f = 1 KHz	48	50	51	dB
ΔG_v	Closed loop gain matching			0.5		dB
e_N	Total input noise voltage	R_g= 10 KΩ (°°)		1.5	5	μV

(°) For TDA 2005S only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

ELECTRICAL CHARACTERISTICS (continued)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	R_g= 10 KΩ f_{ripple}= 100 Hz C_3= 10 μF V_{ripple}= 0.5V	35	45		dB
η	Efficiency	V_s = 14.4V f = 1 KHz R_L= 4Ω P_o= 6.5W R_L= 2Ω P_o= 10W V_s = 13.2V f = 1 KHz R_L= 3.2Ω P_o= 6.5W R_L= 1.6Ω P_o= 10W		 70 60 70 60		 % % % %
T_j	Thermal shut-down junction temperature			145		°C

Fig. 8 - Quiescent output voltage vs. supply voltage

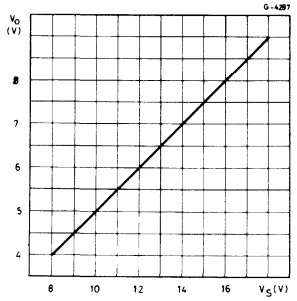


Fig. 9 - Quiescent drain current vs. supply voltage

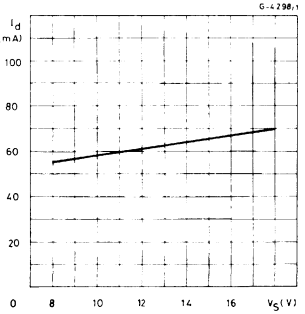


Fig. 10 - Distortion vs. output power

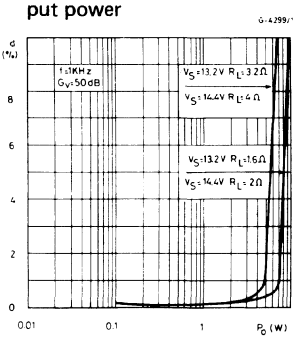


Fig. 11 - Output power vs. supply voltage

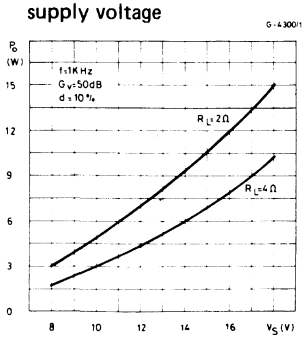


Fig. 12 - Output power vs. supply voltage

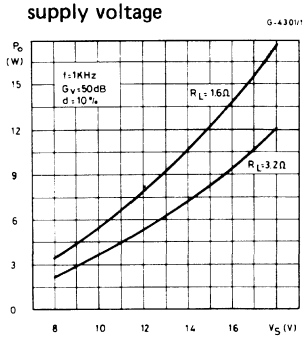


Fig. 13 - Distortion vs. frequency

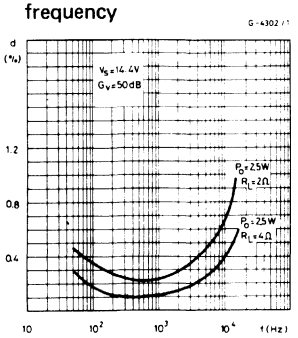


Fig. 14 - Distorsion vs. frequency

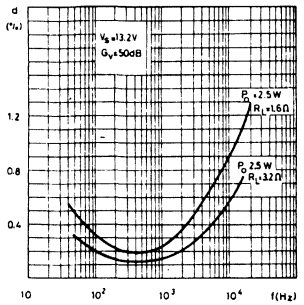


Fig. 15 - Supply voltage rejection vs. C_3

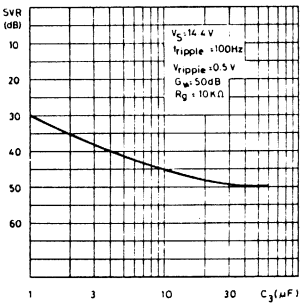


Fig. 16 - Supply voltage rejection vs. frequency

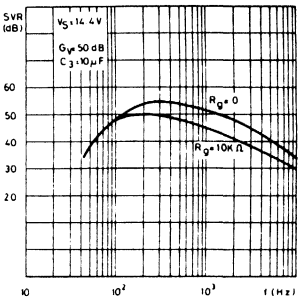


Fig. 17 - Supply voltage rejection vs. values of capacitors C_2 and C_3

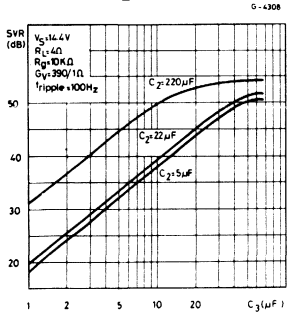


Fig. 18 - Supply voltage rejection vs. values of capacitors C_2 and C_3

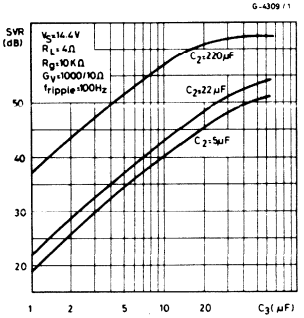


Fig. 19 - Gain vs. input sensitivity

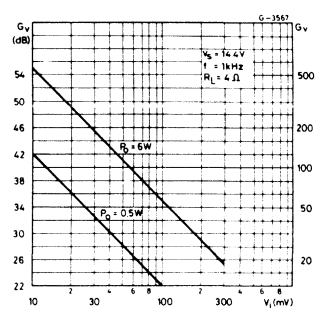


Fig. 20 - Gain vs. input sensitivity

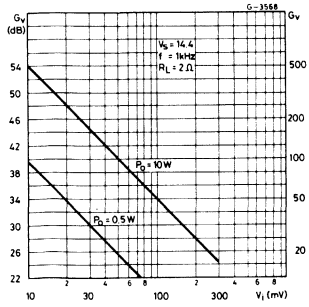


Fig. 21 - Total power dissipation and efficiency vs. output power (bridge)

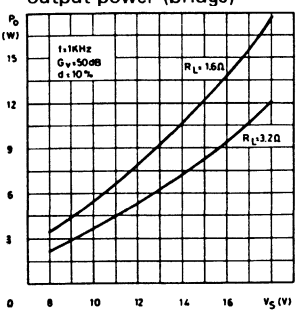
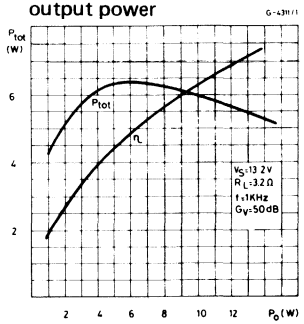


Fig. 22 - Total power dissipation and efficiency vs. output power



APPLICATION SUGGESTION

The recommended values of the components are those shown on Bridge application circuit of fig. 1. Different values can be used, the following table can help the designer.

Component	Recommended Value	Purpose	Larger than	Smaller than
R_1	120 KΩ	Optimization of the output symmetry	Smaller P_o max	Smaller P_o max
R_2	1 KΩ	Closed loop gain setting (see BRIDGE AMPLIFIER DESIGN) (*)		
R_3	2 KΩ			
R_4 and R_5	12 Ω			
R_6 and R_7	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive loads	
C_1	2.2 μF	Input DC decoupling	High turn on delay	Higher turn on pop. Higher low frequency cutoff. Increase of noise.
C_2	2.2 μF	Optimization of turn on pop and turn on delay.		
C_3	0.1 μF	Supply by pass		Danger of oscillation.
C_4	10 μF	Ripple Rejection	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.
C_5 and C_7	100 μF	Bootstrapping		Increase of distortion at low frequency.
C_6 and C_8	220 μF	Feedback input DC decoupling, low frequency cutoff.		Higher low frequency cutoff.
C_9 and C_{10}	0.1 μF	Frequency stability.		Danger of oscillation.

(*) The closed loop gain must be higher than 32dB.

APPLICATION INFORMATION

Fig. 23 - Bridge amplifier without boostrap

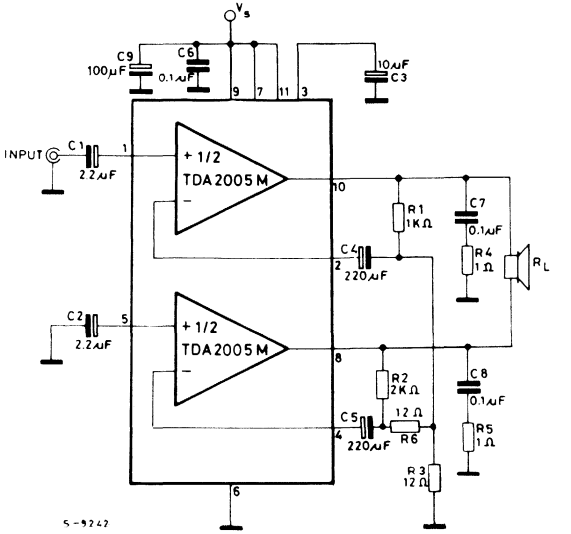
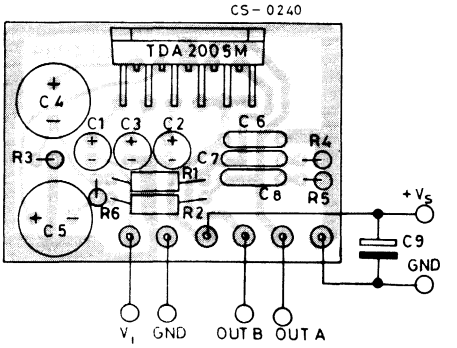


Fig. 24 - P.C. board and component layout of the circuit of Fig. 23 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Fig. 25 - Dual - Bridge amplifier

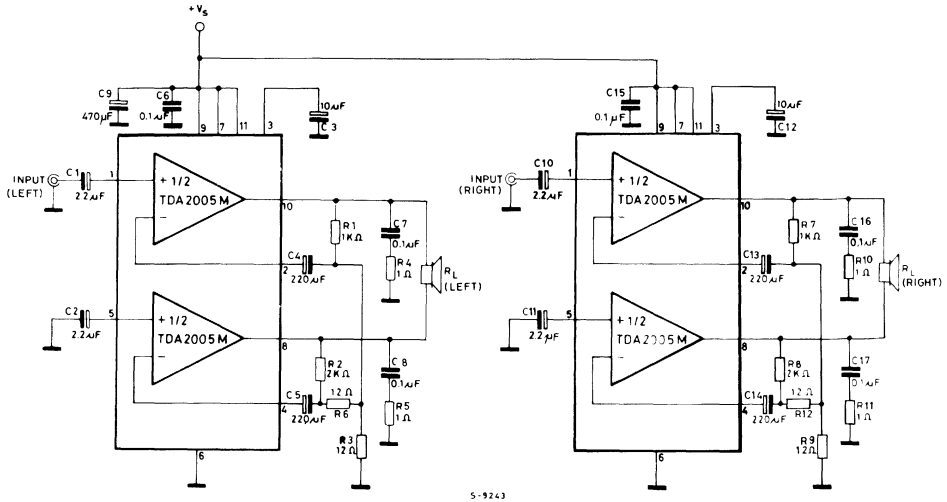
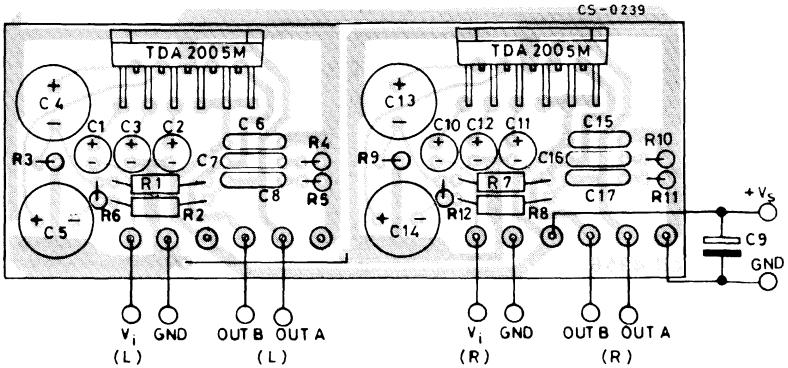


Fig. 26 - P.C. board and components layout of circuit of Fig. 25 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 27 - Low cost bridge amplifier (G_v = 42dB)

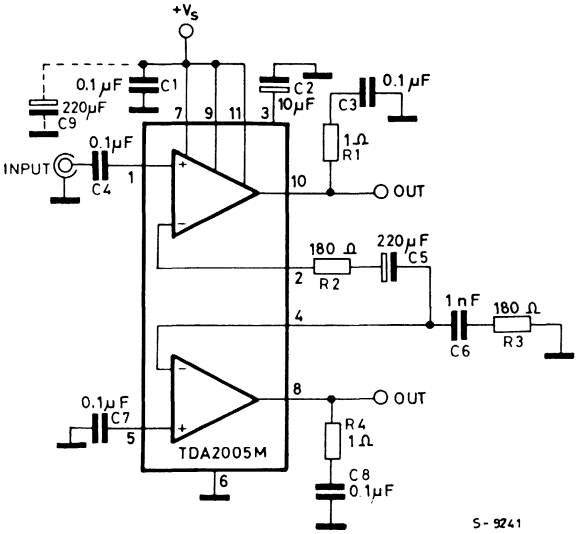
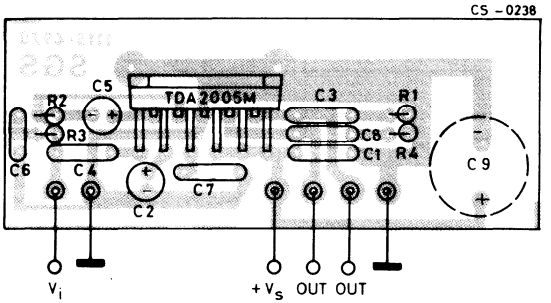


Fig. 28 - P.C. and component layout of the circuit of Fig. 27 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 29 - 10 + 10W stereo amplifier with tone balance and loudness control

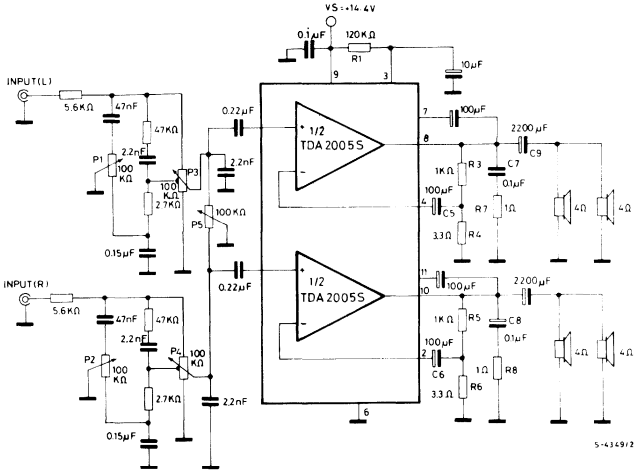


Fig. 30 - Tone control response (circuit of Fig. 29)

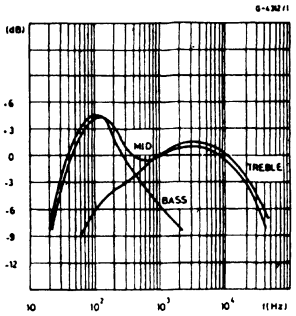


Fig. 31 - 20W Bus amplifier

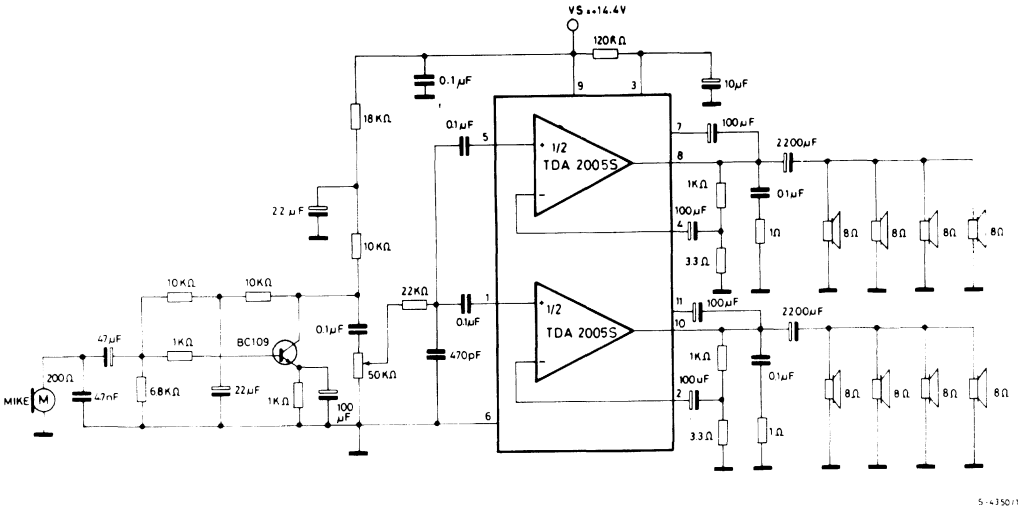


Fig. 32 - Simple 20W two way amplifier (F_c = 2KHz)

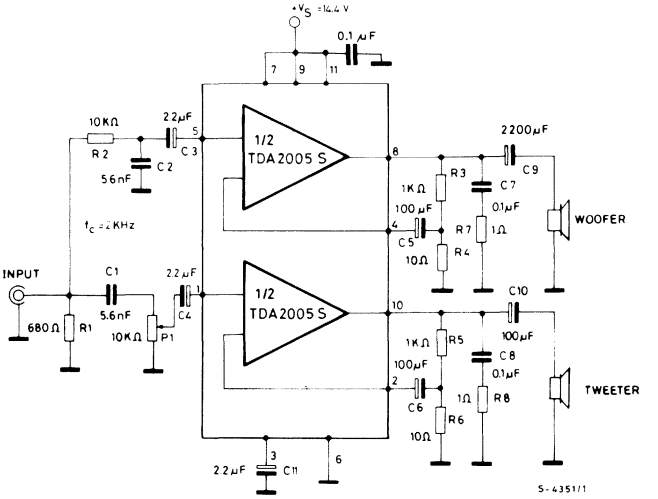
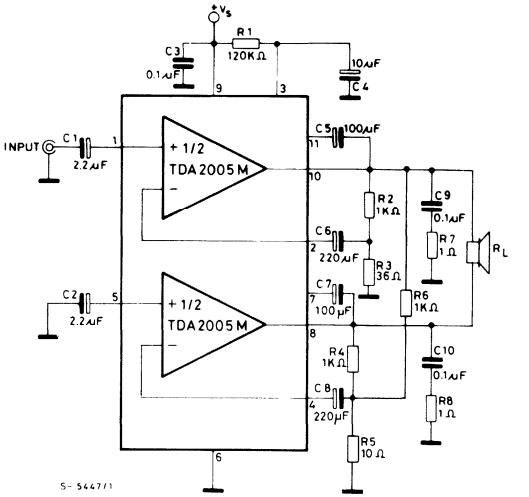
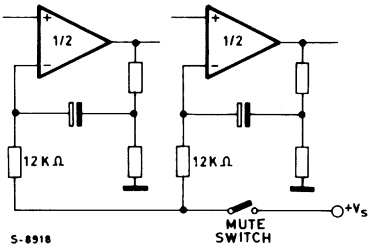


Fig. 33 - Bridge amplifier circuit suited for low-gain applications (G_v = 34dB)



APPLICATION INFORMATION (continued)

Fig. 34 - Example of muting circuit



BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA2005 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in Fig. 36.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held withing the limits shown.
A suggested LC network is shown in Fig. 35. With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 35

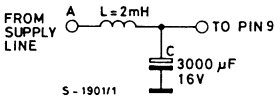
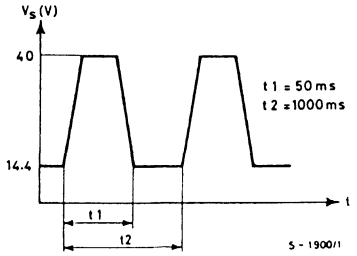


Fig. 36



Short circuit (AC and DC conditions)

The TDA2005 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2005 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided to allow use of the TDA2005 with inductive loads.

DC voltage

The maximum operating DC voltage for the TDA2005 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

BUILT-IN PROTECTION SYSTEMS (continued)

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 37 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Loudspeaker protection

The circuit offers loudspeaker protection during short circuit for one wire to ground.

Fig. 37 - Maximum allowable power dissipation vs. ambient temperature

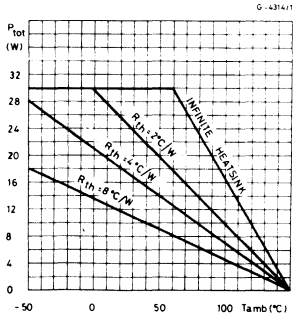


Fig. 38 - Output power and drain current vs. case temperature

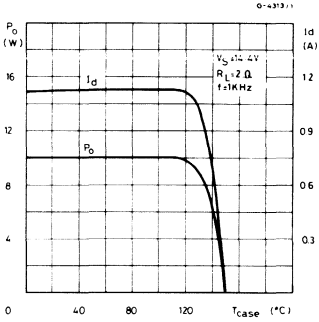
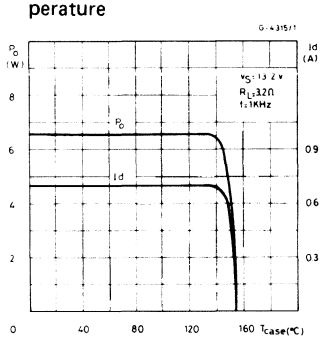


Fig. 39 - Output power and drain current vs. case temperature



12W AUDIO AMPLIFIER

The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At ± 12V, d = 10% typically it provides 12W output power on a 4Ω load and 8W on a 8Ω. The TDA2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.

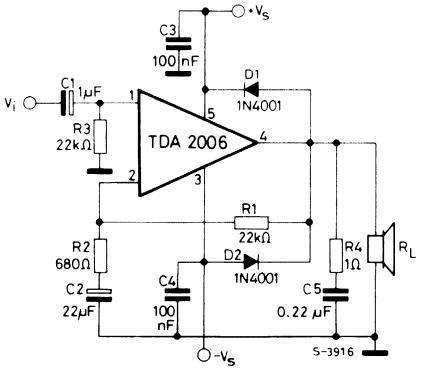
Pentawatt®

ORDER CODE: TDA2006H
TDA2006V

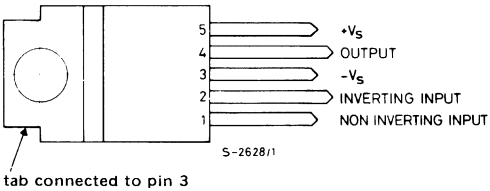
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 12	V
I_o	Output peak current (internally limited)	3	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

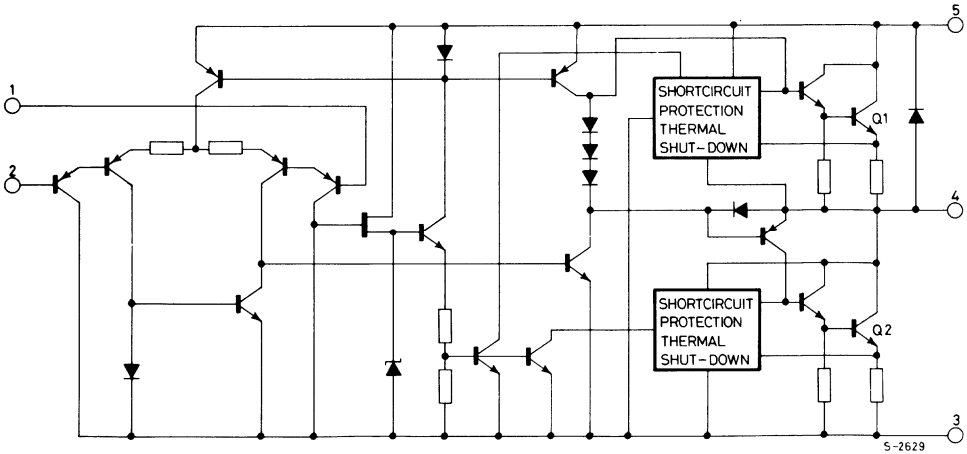
TEST AND APPLICATION CIRCUIT



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\text{-}j\ case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; $V_s = \pm 12V$, $T_{amb} = 25°C$ unless otherwise specified)

Paremeter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 15	V
I_d	Quiescent drain current	$V_s = \pm 15V$		40	80	mA
I_b	Input bias current			0.2	3	μA
V_{OS}	Input offset voltage			± 8		mV
I_{OS}	Input offset current			± 80		nA
V_{OS}	Output offset voltage			± 10	± 100	mV
P_o	Output power	d = 10% f = 1KHz $R_L = 4\Omega$ $R_L = 8\Omega$	 6	 12 8		 W W
d	Distortion	P_o = 0.1 to 8W $R_L = 4\Omega$ f = 1KHz		0.2		%
		P_o = 0.1 to 4W $R_L = 8\Omega$ f = 1KHz		0.1	1	%
V_i	Input sensitivity	P_o = 10W f = 1KHz $R_L = 4\Omega$ P_o = 6W $R_L = 8\Omega$		200 220		mV mV
B	Frequency response (-3dB)	P_o = 8W $R_L = 4\Omega$	20 Hz to 100 KHz			
R_i	Input resistance (pin 1)	f = 1KHz	0.5	5		MΩ
G_v	Voltage gain (open loop)			75		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB
e_N	Input noise voltage	B (-3dB) = 22Hz to 22KHz $R_L = 4\Omega$		3	10	μV
i_N	Input noise current			80	200	pA
SVR	Supply voltage rejection	$R_L = 4\Omega$ $R_g = 22K\Omega$ f_{ripple} = 100Hz (*)	40	50		dB
I_d	Drain current	P_o = 12W $R_L = 4\Omega$ P_o = 8W $R_L = 8\Omega$		850 500		mA mA
T_j	Thermal shutdown junction temperature				145	°C

(*) Referring to Fig. 15, single supply.

Fig. 1 - Output power vs. supply voltage

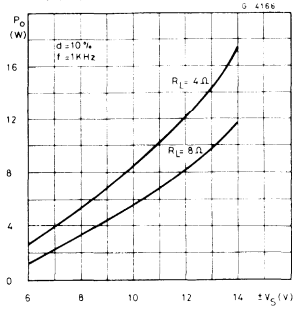


Fig. 2 - Distortion vs. output power

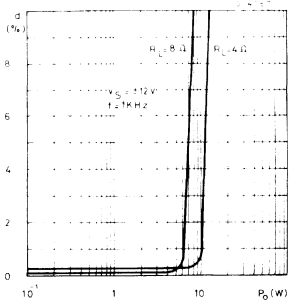


Fig. 3 - Distortion vs. frequency

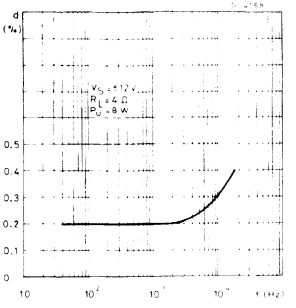


Fig. 4 - Distortion vs. frequency

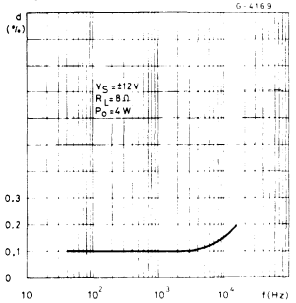


Fig. 5 - Sensitivity vs. output power

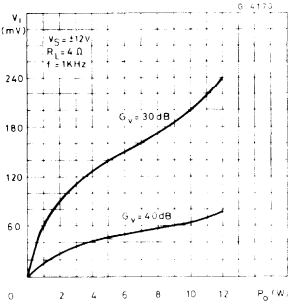


Fig. 6 - Sensitivity vs. output power

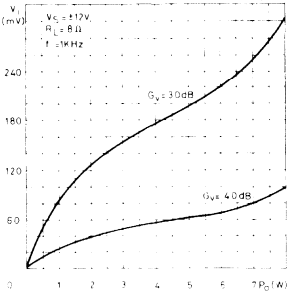


Fig. 7 - Frequency response with different values of the rolloff capacitor C_8 (see fig. 13)

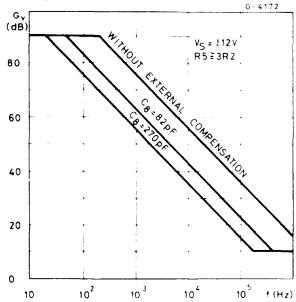


Fig. 8 - Value of C_8 vs. voltage gain for different bandwidths (see fig. 13)

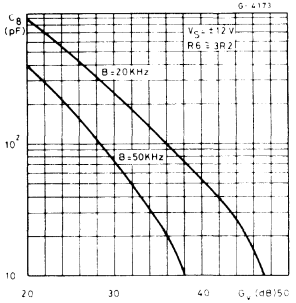


Fig. 9 - Quiescent current vs. supply voltage

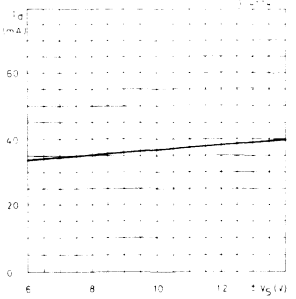


Fig. 10 - Supply voltage rejection vs. voltage gain

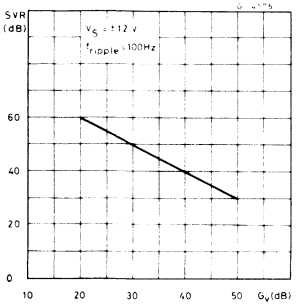


Fig. 11 - Power dissipation and efficiency vs. output power

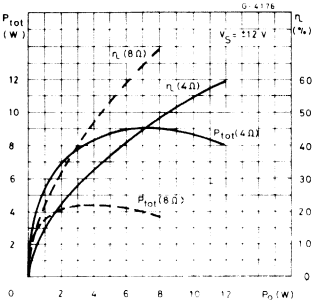


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)

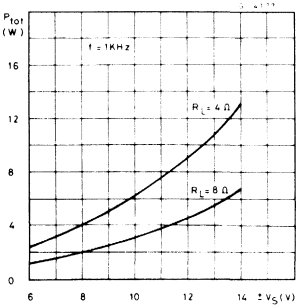


Fig. 13 - Application circuit with split power supply

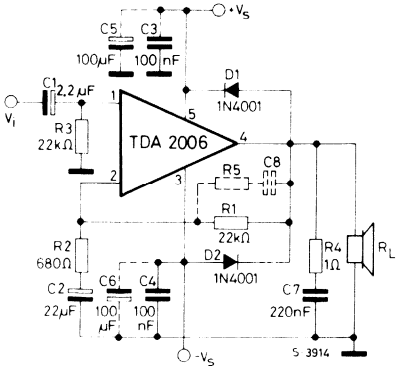


Fig. 14 - P.C. board and component layout for the circuit of fig. 13

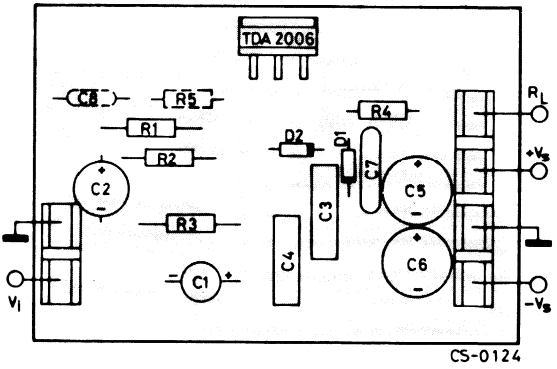


Fig. 15 - Application circuit with single power supply

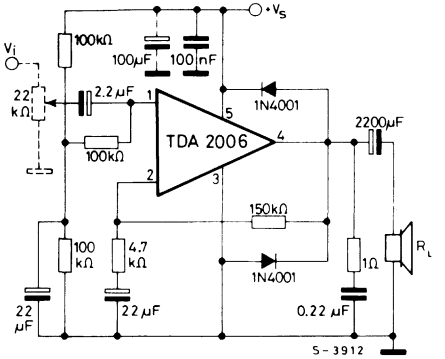


Fig. 16 - P.C. board and component layout for the circuit of fig. 15

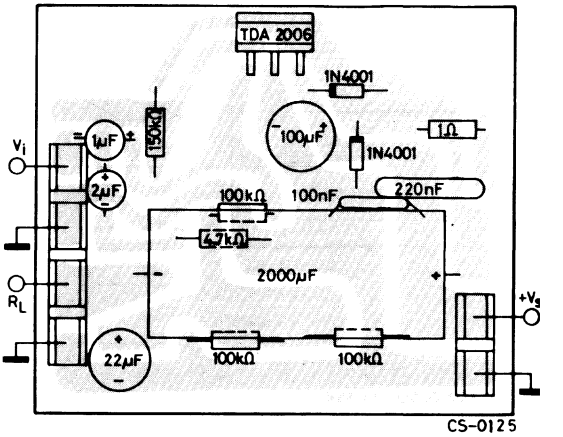
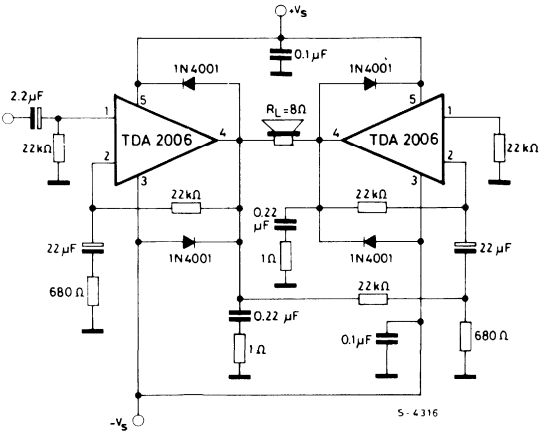


Fig. 17 - Bridge amplifier configuration with split power supply (Po = 24W, $V_S = \pm 12V$)



PRACTICAL CONSIDERATION

Printed circuit board

The layout shown in Fig. 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

Application suggestion

The recommended values of the components are the ones shown on application circuits of Fig. 13. Different values can be used. The following table can help the designers.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R_1	22 KΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R_2	680Ω	Closed loop gain setting	Decrease of gain (*)	Increase pf gain
R_3	22 KΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_5	$3\,R_2$	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C_1	2.2 μF	Input DC decoupling		Increase of low freqencies cut off
C_2	22 μF	Inverting input DC decoupling		Increase of low frequencies cutoff
C_3C_4	0.1 μF	Supply voltage by pass		Danger of oscillation
C_5C_6	100 μF	Supply voltage by pass		Danger of oscillation
C_7	0.22 μF	Frequency stability		Danger of oscillation
C_8	$\frac{1}{2\pi BR_1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
D_1D_2	1N4001	To protect the device against output voltage spikes.		

(*) Closed loop gain must be higher than 24dB

SHORT CIRCUIT PROTECTION

The TDA2006 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (Fig. 19).

This function can therefore be considered as being peak power limiting rather than simple current limiting.
It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

Fig. 18 - Maximum output current vs. voltage $V_{Ce(sat)}$ across each output transistor

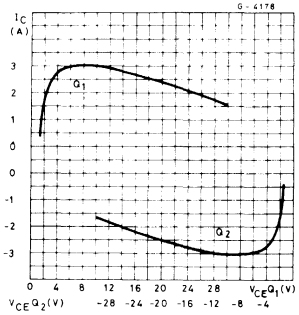
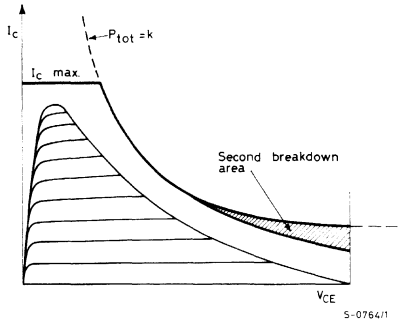


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

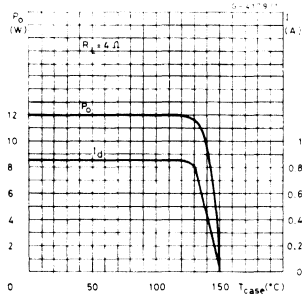
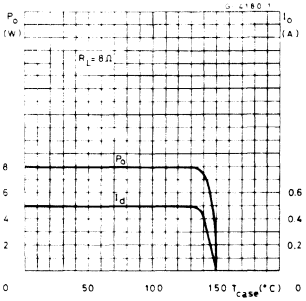


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistances.

Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

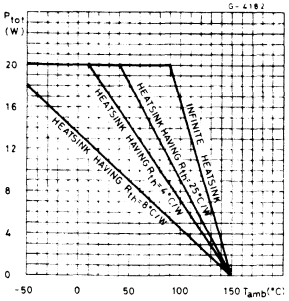
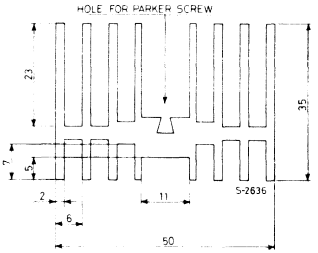


Fig. 23 - Example of heatsink



Dimension suggestion

The following table shows the lenght of the heatsink in fig. 23 for several values of P_{tot} and R_{th}.

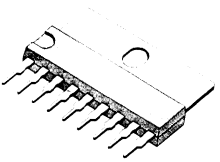
P_{tot} (W)	12	8	6
Lenght of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

TDA2007

6 + 6 W STEREO AMPLIFIER

The TDA 2007 is a class AB dual Audio power amplifier assembled in single in line 9 pins package, specially designed for stereo application in music centers TV receivers and portable radios. Its main features are:

- High output power
- High current capability
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the SIP. 9 package.



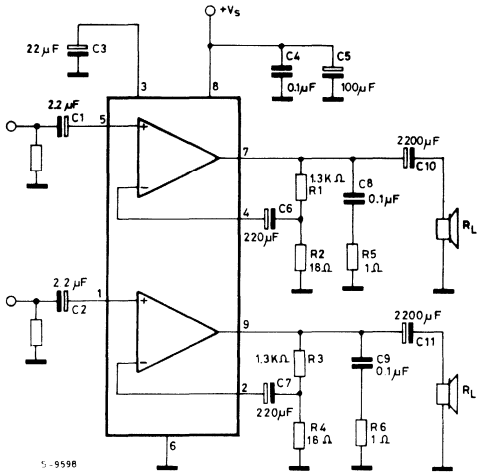
SIP. 9

ORDERING NUMBER: TDA 2007

ABSOLUTE MAXIMUM RATINGS

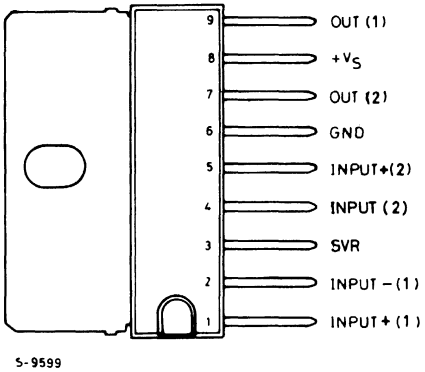
V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20 Hz)	3	A
I_o	Output peak current (non repetitive, t = 100 μs)	3.5	A
P_{tot}	Power dissipation at T_{case} = 70°C	10	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

STEREO TEST CIRCUIT



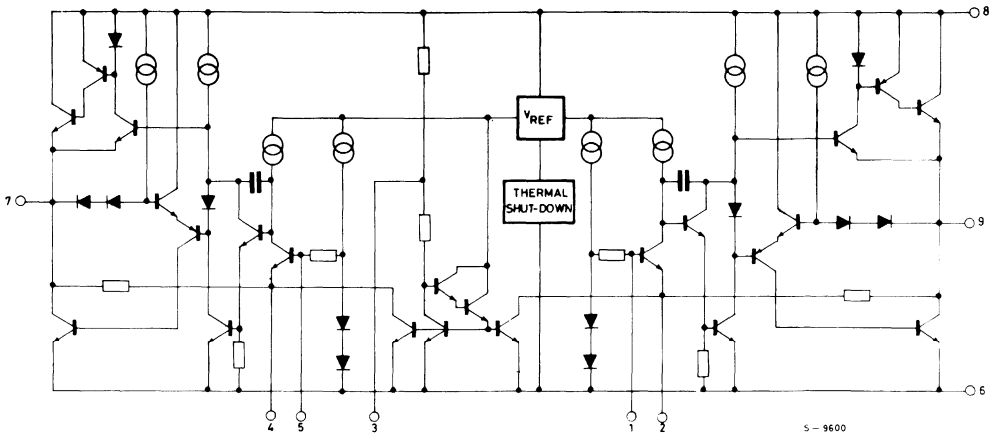
TDA2007

CONNECTION DIAGRAM
(Top view)



S-9599

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb}= 25°C, V_s = 18V, G_v = 36 dB, unless otherwise specified)

Parameters		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		26	V
V_o	Quiescent output voltage				8.5		V
I_d	Total quiescent drain current				48		mA
P_o	Output power (each channel)	f = 100 Hz to 16 KHz d = 0.5% V_s = 18V R_L = 4Ω V_s = 22V R_L = 8Ω		 5.5 5.5	 6 6		 W W
d	Distortion (each channel)	f = 1 KHz, V_s = 18V, R_L = 4Ω P_o = 100 mW to 3W			0.1	0.2	%
		f = 1 KHz, V_s = 22V, R_L = 8Ω P_o = 100 mW to 3W			0.05	0.1	%
CT	Cross talk (°°°)	R_L = ∞	f = 1 KHz	50	60		dB
		R_g = 10 KΩ	f = 10 KHz	40	50		dB
V_i	Input saturation voltage (rms)			300			mV
R_i	Input resistance	f = 1 KHz		70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L = 4Ω, C10 = C11= 2200 μF			40		Hz
f_H	High frequency roll off (-3 dB)				80		KHz
G_v	Voltage gain (closed loop)	f = 1 KHz		35.5	36	36.5	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ (°)			1.5		μV
		R_g = 10 KΩ (°°)			2.5	8	μV
SVR	Supply voltage rejection (each channel)	R_g = 10 KΩ f_{ripple}= 100 Hz V_{ripple}= 0.5V			55		dB
T_J	Thermal shut-down junction temperature				145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Fig. 1 - Stereo test circuit (G_v = 36 dB)

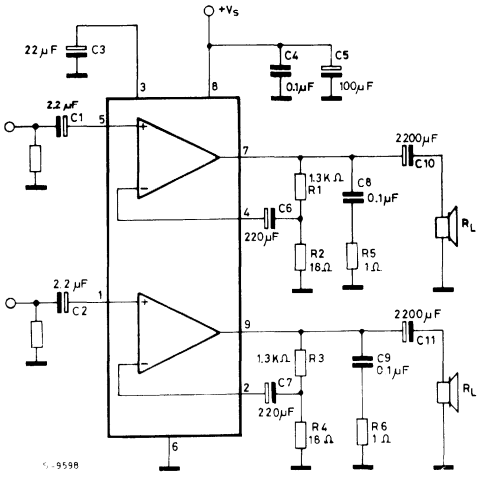


Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1 : 1 scale)

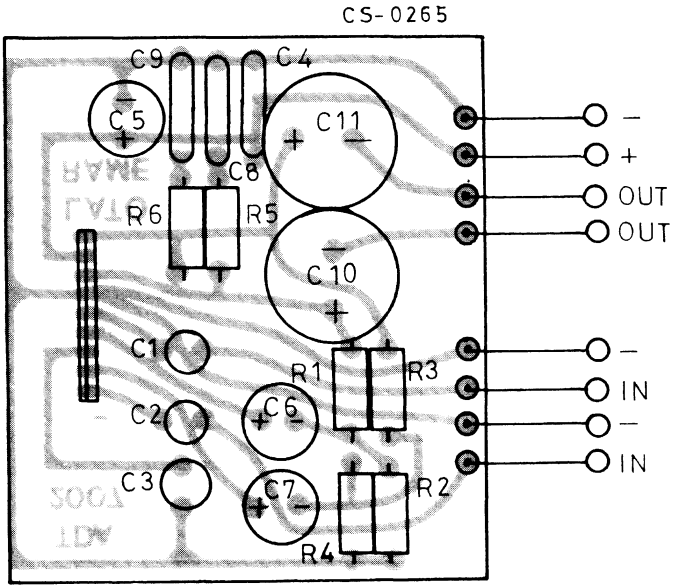


Fig. 3 - Output power vs. supply voltage (d = 0.5%)

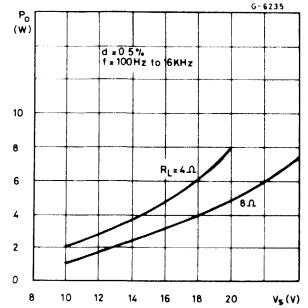


Fig. 4 - Output power vs. supply voltage (d = 10%)

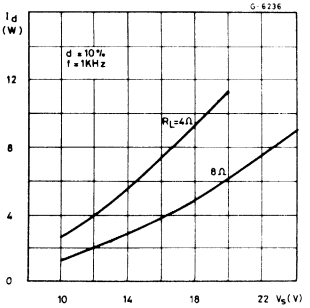


Fig. 5 - Quiescent current vs. supply voltage

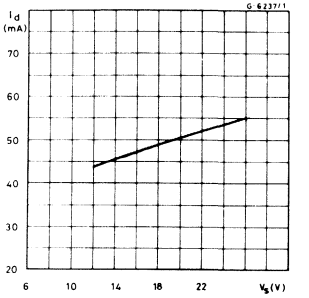


Fig. 6 - Supply voltage rejection vs. value of capacitor C3

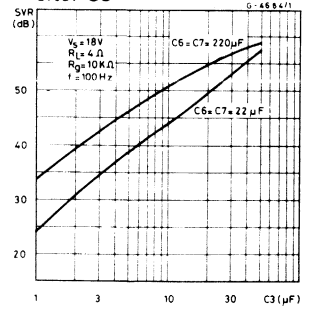


Fig. 7 - Supply voltage rejection vs. frequency

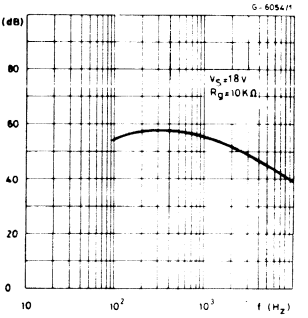


Fig. 8 - Total power dissipation vs. output power

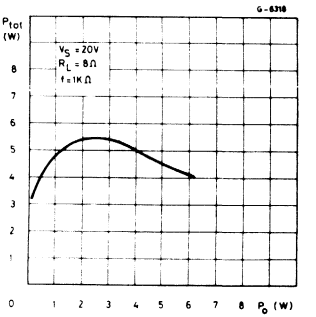


Fig. 9 - Cross-talk vs. frequency

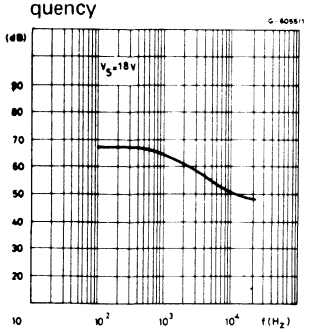


Fig. 10 - Simple short-circuit protection

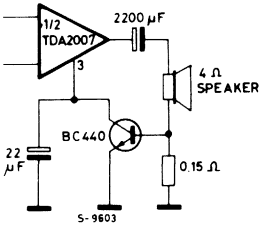
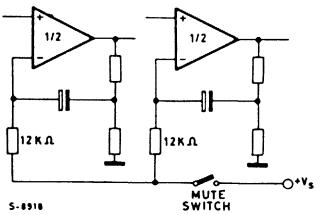
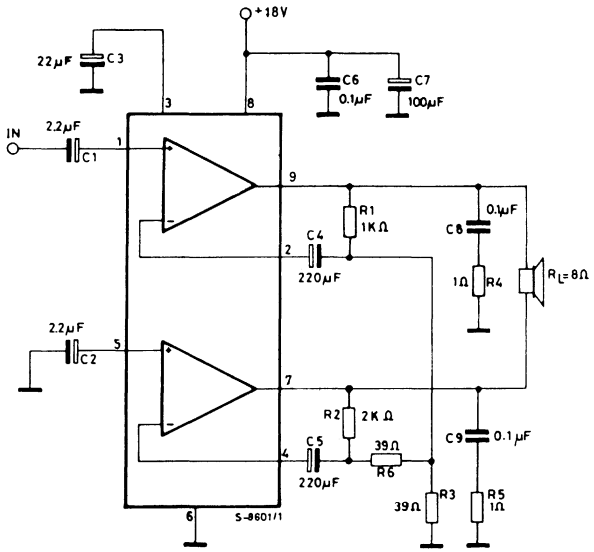


Fig. 11 - Example of muting circuit



APPLICATION INFORMATION

Fig. 12 - 12W bridge amplifier (d = 0,5%, G_v = 40dB)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.3 KΩ	Close loop gain setting(*)	Increase of gain	Decrease of gain
R2 and R4	18 Ω		Decrease of gain	Increase of gain
R5 and R6	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22 μF	Ripple rejection	Better SVR. Increase of the switch-on time	Degradation of SVR.
C6 and C7	220 μF	Feedback Input DC decoupling		
C8 and C9	0.1 μF	Frequency stability		Danger of oscillation
C10 and C11	1000 μF to 2200 μF	Output DC decoupling		Higher low-frequency cut-off

(*) The closed loop gain must be higher than 26 dB.

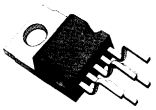
TDA2008

12W AUDIO AMPLIFIER (V_s = 22V, R_L = 4Ω)

The TDA2008 is a monolithic class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 3.2Ω). The device provides a high output current capability (up to 3A), very low harmonic and crossover distortion.

In addition, the device offers the following features:

- very low number of external components;
- assembly ease, due to Pentawatt® power package with no electrical insulation requirements;
- space and cost saving;
- high reliability;
- flexibility in use;
- thermal protection.



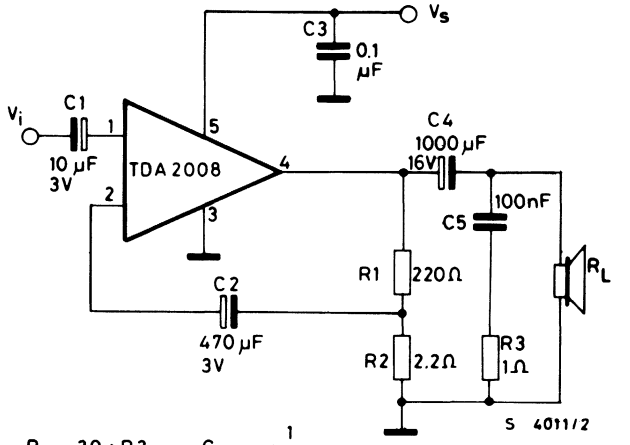
Pentawatt

ORDERING NUMBER: TDA2008V

ABSOLUTE MAXIMUM RATINGS

V_s	DC supply voltage	28	V
I_o	Output peak current (repetitive)	3	A
I_o	Output peak current (non repetitive)	4	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

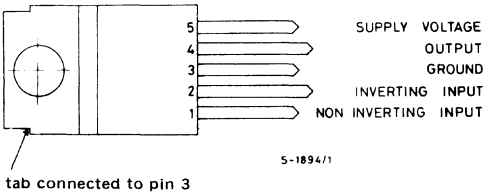
TYPICAL APPLICATION CIRCUIT



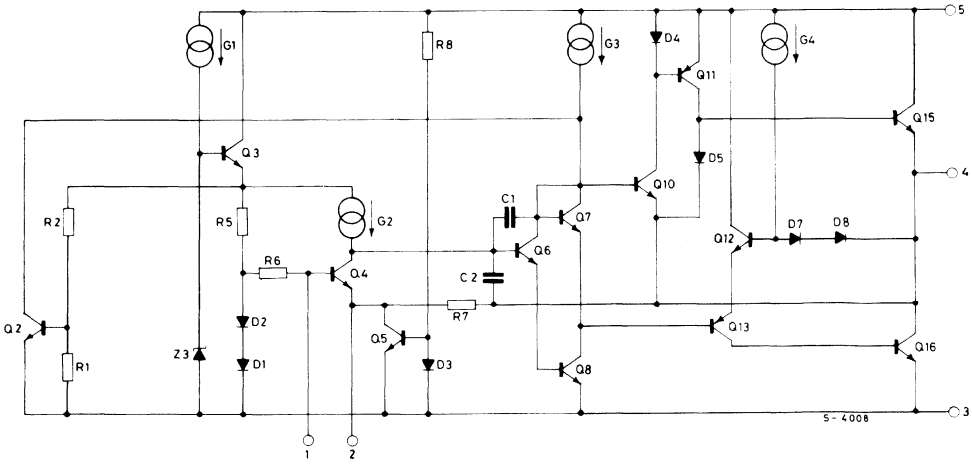
$$R_x = 20 \cdot R2 \quad ; \quad C_x = \frac{1}{2\pi BR1}$$

TDA2008

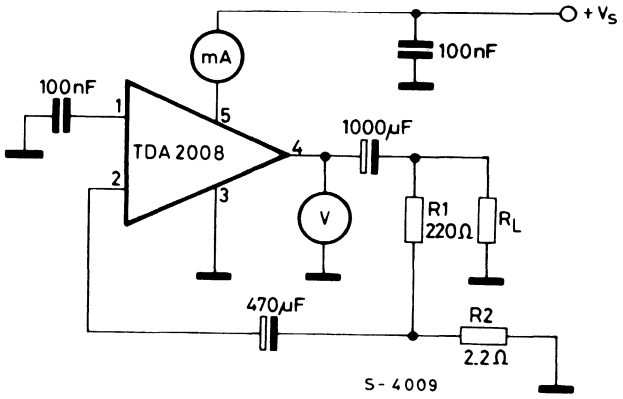
CONNECTION DIAGRAM (top view)



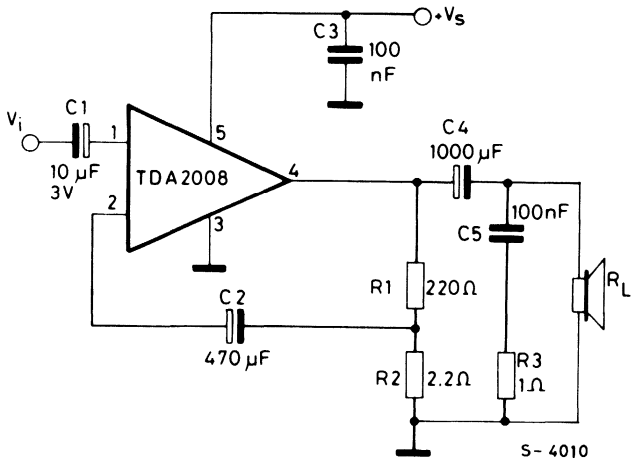
SCHEMATIC DIAGRAM



DC TEST CIRCUIT



AC TEST CIRCUIT



THERMAL DATA

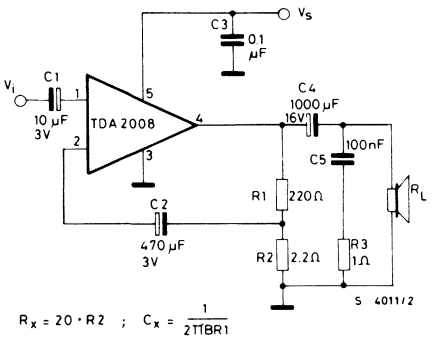
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 22V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			10		28	V
V_o	Quiescent output voltage (pin 4)				10.5		V
I_d	Quiescent drain current (pin 5)				65	115	mA
P_o	Output power	d = 10%	R_L = 8Ω		8		W
		f = 1 KHz	R_L = 4Ω	10	12		W
V_i (RMS)	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 KHz P_o = 0.5W P_o = 8W P_o = 0.5W P_o = 12W	 R_L = 8Ω R_L = 8Ω R_L = 4Ω R_L = 4Ω		 20 80 14 70		 mV mV mV mV
B	Frequency response (-3 dB)	P_o = 1W R_L = 4Ω		40 to 15 000			Hz
d	Distortion	f = 1 KHz P_o = 0.05 to 4W P_o = 0.05 to 6W	 R_L = 8Ω R_L = 4Ω		 0.12 0.12	 1 1	 % %
R_i	Input resistance (pin 1)	f = 1 KHz		70	150		KΩ
G_v	Voltage gain (open loop)	f = 1 KHz	R_L = 8Ω		80		dB
G_v	Voltage gain (closed loop)			39.5	40	40.5	dB
e_N	Input noise voltage	BW= 22Hz to 22 KHz			1	5	μV
i_N	Input noise current				60	200	pA
SVR	Supply voltage rejection	V_{ripple} = 0.5V R_g = 10KΩ R_L = 4Ω	f = 100 Hz	30	36		dB

APPLICATION INFORMATION

Fig. 1 - Typical application circuit



$R_x = 20 \cdot R2$; $C_x = \frac{1}{2\pi BR1}$

Fig. 2 - P.C. board and component layout for the circuit of fig. 1 (1:1 scale)

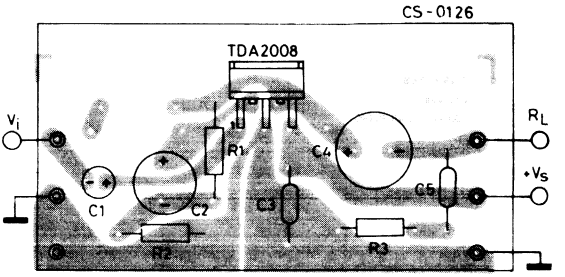


Fig. 3 - 25W bridge configuration application circuit (°)

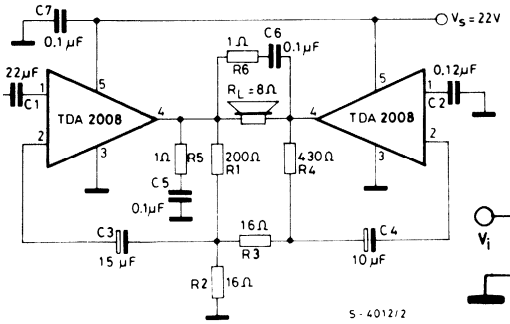
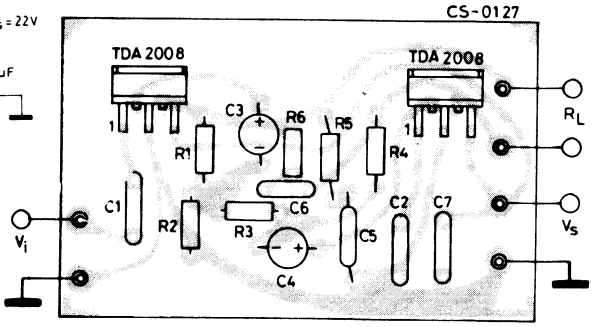


Fig. 4 - P.C. board and component layout for the circuit of fig. 3 (1:1 scale)



(°) The value of the capacitors C3 and C4 are different to optimize the SVR (Typ. = 40 dB)

Fig. 5 - Quiescent current vs. supply voltage

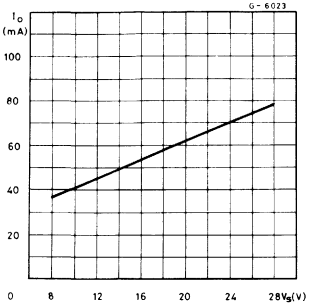


Fig. 6 - Output voltage vs. supply voltage

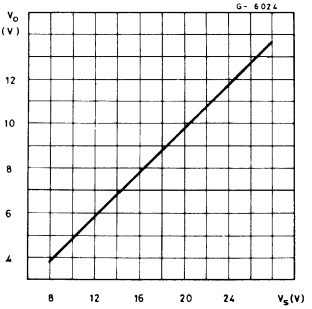


Fig. 7 - Output power vs. supply voltage

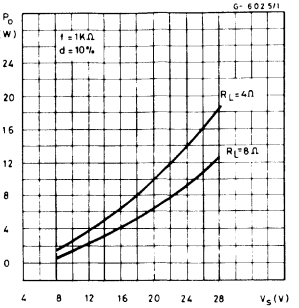


Fig. 8 - Distortion vs. frequency

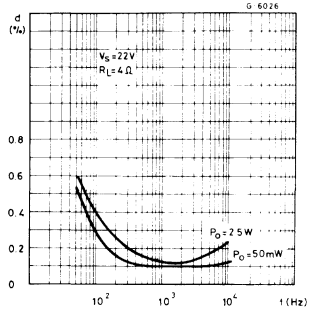


Fig. 9 - Supply voltage rejection vs. frequency

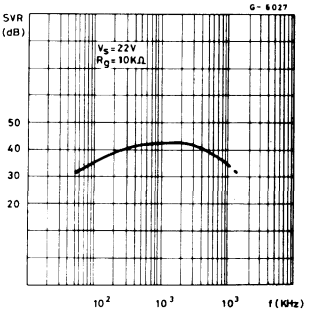
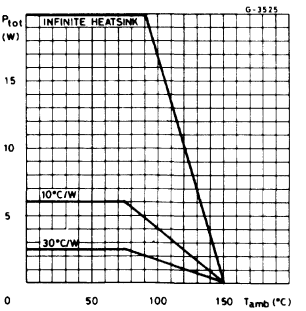


Fig. 10 - Maximum allowable power dissipation vs. ambient temperature



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in Fig. 2 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion

No electrical insulation is needed between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions

The recommended component values are those shown in the application circuits of Fig. 1. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2μF	Input DC decoupling.		Noise at switch-on, switch-off.
C2	470μF	Ripple rejection.		Degradation of SVR.
C3	0.1μF	Supply bypassing.		Danger of oscillation.
C4	1000μF	Output coupling.		Higher low frequency cutoff.
C5	0.1μF	Frequency stability.		Danger of oscillation at high frequencies with inductive loads.
R1	$(G_V-1) \cdot R2$	Setting of gain. (*)		Increase of drain current.
R2	2.2Ω	Setting of gain and SVR.	Degradation of SVR.	
R3	1Ω	Frequency stability.	Danger of oscillation at high frequencies with inductive loads.	

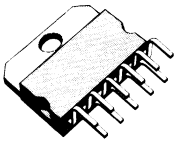
(*) The closed loop gain must be higher than 26dB.

TDA2009

10 + 10W HIGH QUALITY STEREO AMPLIFIER

The TDA2009 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo application as Hi-Fi and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 0.5%)
- High current capability (up to 3.5A)
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.



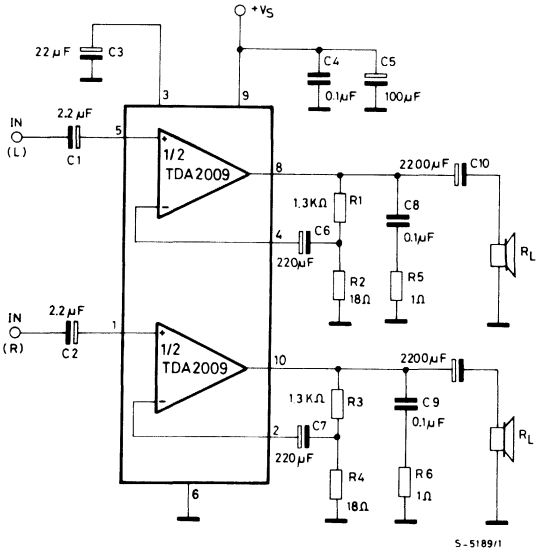
Multiwatt-11

ORDERING NUMBER: TDA2009

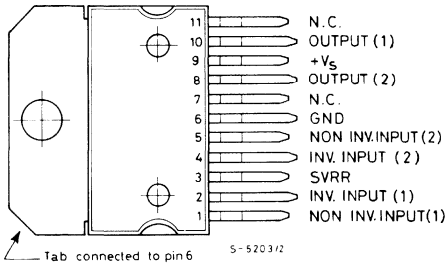
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20Hz)	3.5	A
I_o	Output peak current (non repetitive, t = 100μs)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

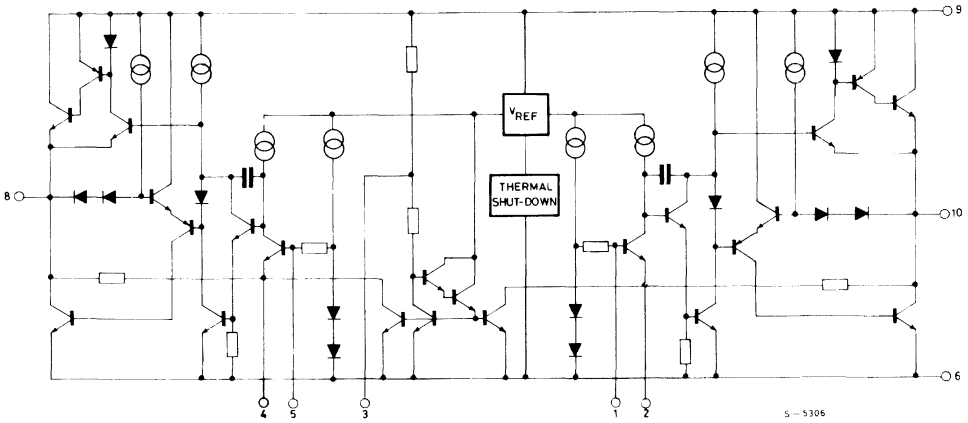
TEST CIRCUIT



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb}= 25°C, V_s = 23V, G_v = 36 dB, unless otherwise specified)

Parameters		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		28	V
V_o	Quiescent output voltage	V_s = 23V			11		V
I_d	Total quiescent drain current	V_s = 23V			55	120	mA
P_o	Output power (each channel)	f = 50 Hz to 16 KHz d = 0.5% V_s = 23V R_L= 4 Ω R_L= 8 Ω V_s = 18V R_L= 4 Ω R_L= 8 Ω		10 5.5	11 6.5 6.5 4		W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 23V R_L= 4 Ω P_o= 100 mW to 8W V_s = 23V R_L= 8 Ω P_o= 100 mW to 3W			0.05 0.05		%
CT	Cross talk (°°°)	R_L= ∞	f = 1 KHz	50	65		dB
		R_g = 10 KΩ	f = 10 KHz	40	50		dB
V_i	Input saturation voltage (rms)			300			mV
R_i	Input resistance	f = 1 KHz	non inverting input	70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L = 4Ω			20		Hz
f_H	High frequency roll off (-3 dB)				80		KHz
G_v	Voltage gain (closed loop)	f = 1 KHz		35.5	36	36.5	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ (°)			1.5		μV
		R_g = 10 KΩ (°°)			2.5	8	μV
SVR	Supply voltage rejection (each channel)	R_g = 10 KΩ f_{ripple}= 100 Hz V_{ripple}= 0.5V		43	55		dB
T_J	Thermal shut-down junction temperature				145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Fig. 1 - Test and application circuit (G_v = 36 dB)

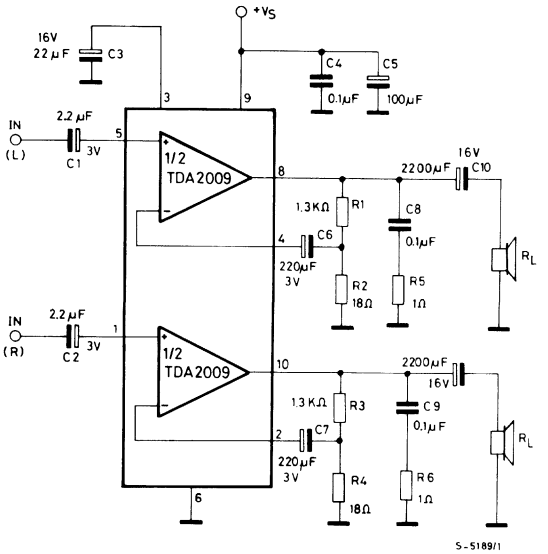


Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1 : 1 scale)

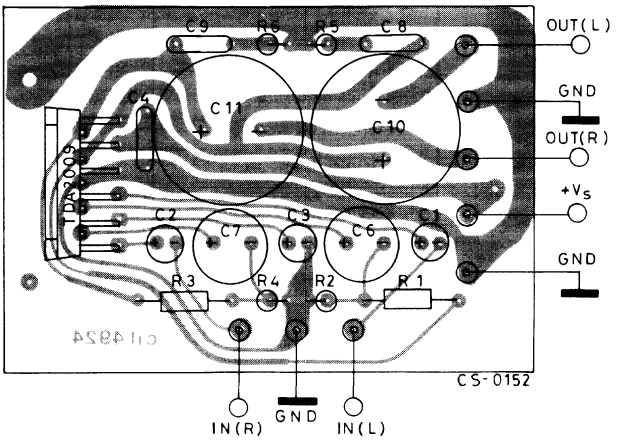


Fig. 3 - Output power vs. supply voltage

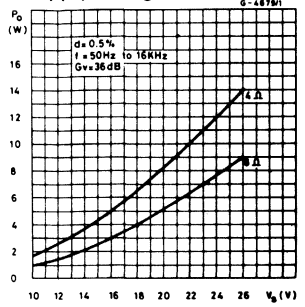


Fig. 4 - Output power vs. supply voltage

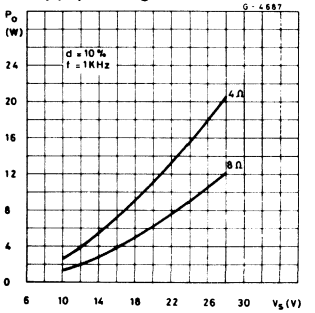


Fig. 5 - Distortion vs. output power

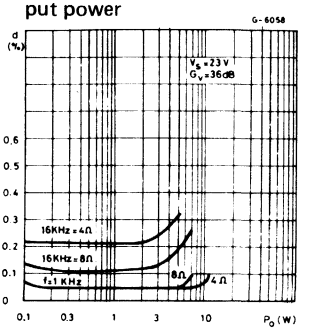


Fig. 6 - Distortion vs. frequency

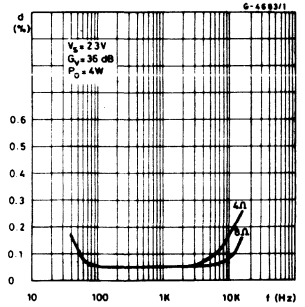


Fig. 7 - Quiescent current vs. supply voltage

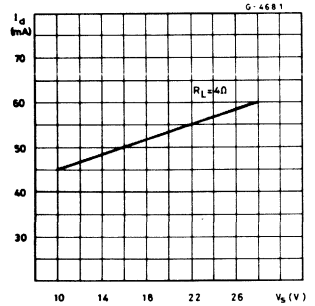


Fig. 8 - Supply voltage rejection vs. value of capacitor C3

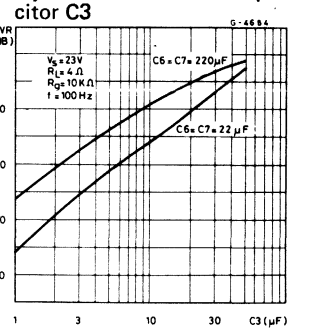


Fig. 9 - Supply voltage rejection vs. frequency

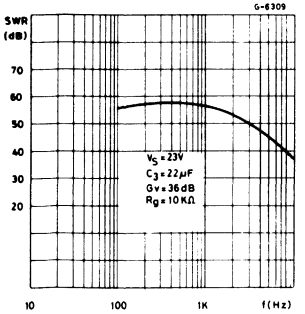


Fig. 10 - Total power dissipation an efficiency vs. output power

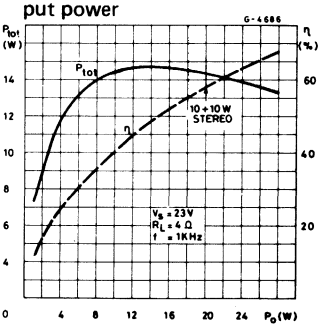


Fig. 11 - Total power dissipation and efficiency vs. output power

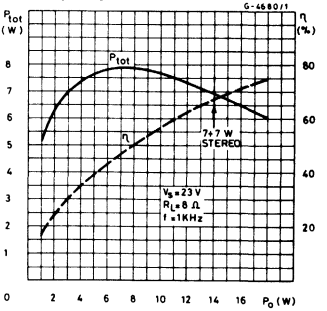


Fig. 12 - Cross-talk vs. frequency

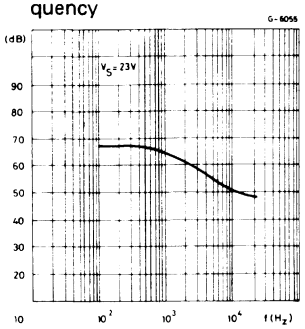


Fig. 13 - Output power vs. closed loop gain

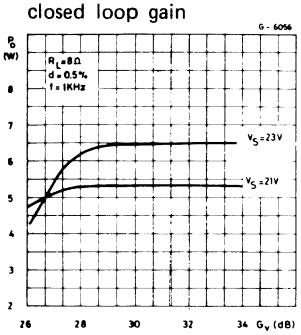
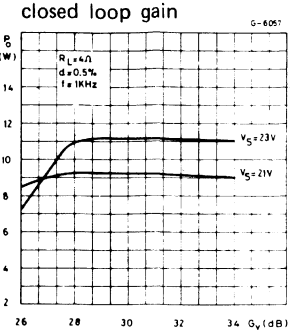


Fig. 14 - Output power vs. closed loop gain



APPLICATION INFORMATION

Fig. 15 - Simple short-circuit protection

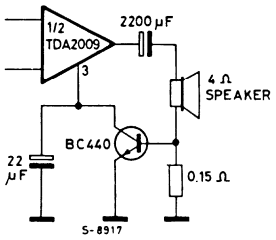


Fig. 16 - Example of muting circuit

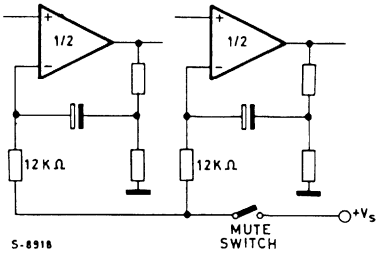


Fig. 17 - 10 + 10W stereo amplifier with tone balance and loudness control

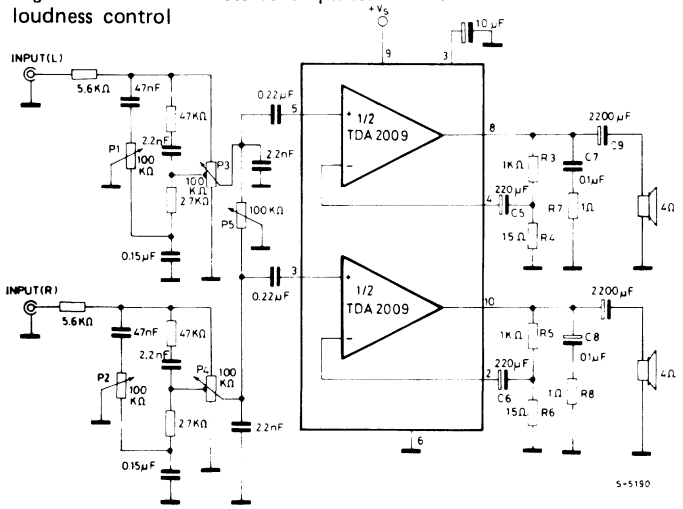
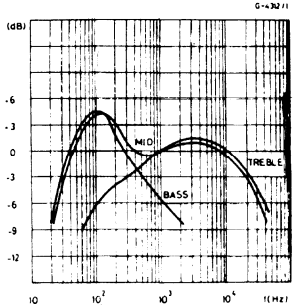


Fig. 18 - Tone control response (circuit of fig. 17)



APPLICATION INFORMATION (continued)

Fig. 19 - High quality 10 + 20W two way amplifier for stereo music center (one channel only)

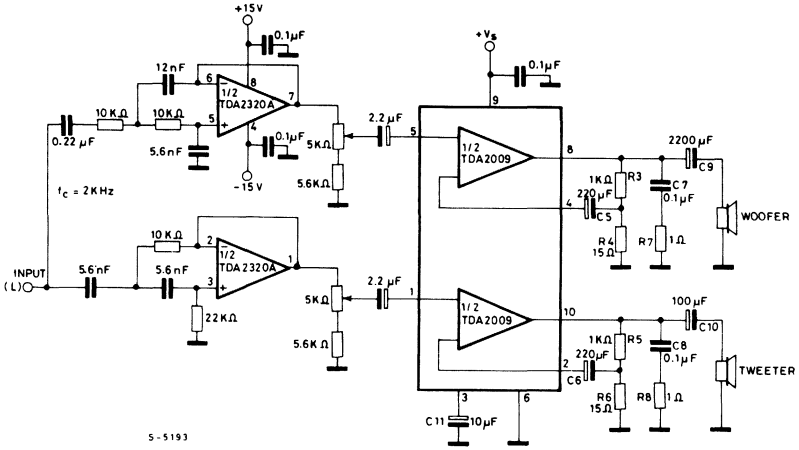


Fig. 20 - 18W bridge amplifier (d = 0.5%, G_v = 40dB)

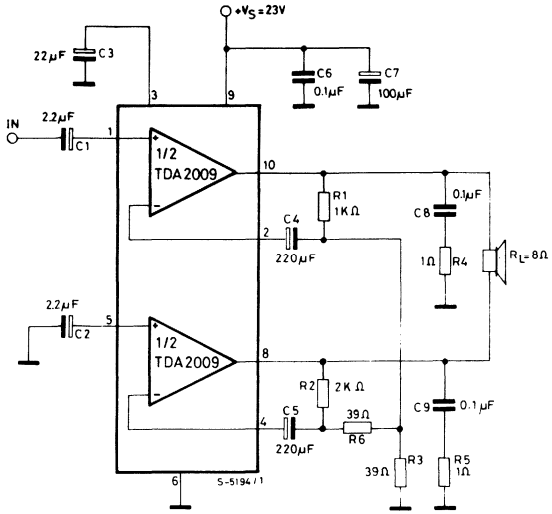
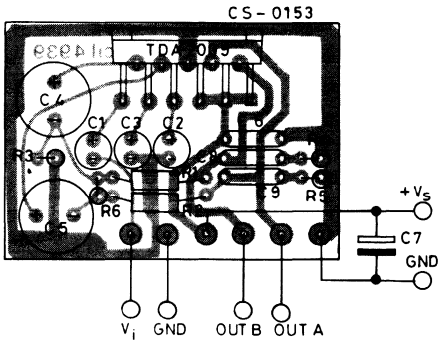


Fig. 21 - P.C. board and components layout of the circuit of fig. 20 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1 . Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.2 KΩ	Close loop gain setting(*)	Increase of gain	Decrease of gain
R2 and R4	18 Ω		Decrease of gain	Increase of gain
R5 and R6	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22 μF	Ripple rejection	Better SVR. Increase of the switch-on time	Degradation of SVR.
C6 and C7	220 μF	Feedback Input DC decoupling.		
C8 and C9	0.1 μF	Frequency stability.		Danger of oscillation.
C10 and C11	1000 μF to 2200 μF	Output DC decoupling.		Higher low-frequency cut-off.

(*) The closed loop gain must be higher than 26dB

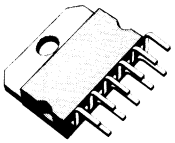
TDA2009A

ADVANCE DATA

10+10W SHORT CIRCUIT PROTECTED STEREO AMPLIFIER

The TDA2009A is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo application as Hi-Fi and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 1%)
- High current capability (up to 3.5A)
- AC short circuit protection
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.



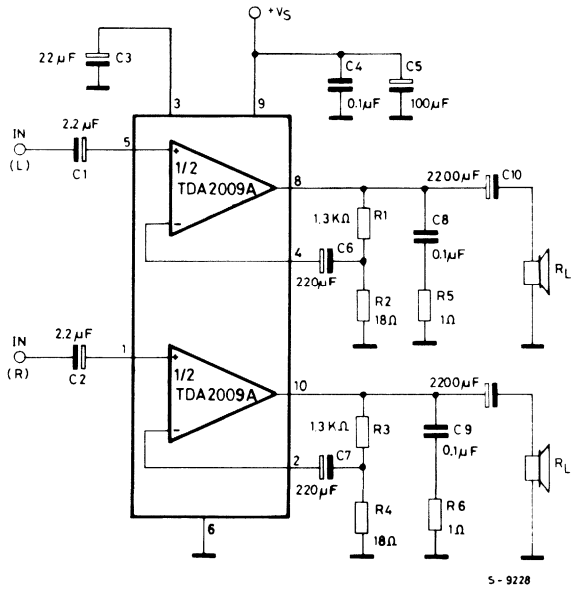
Multiwatt-11

ORDERING NUMBER: TDA2009A

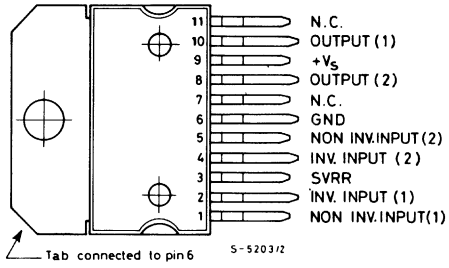
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20Hz)	3.5	A
I_o	Output peak current (non repetitive, t = 100μs)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

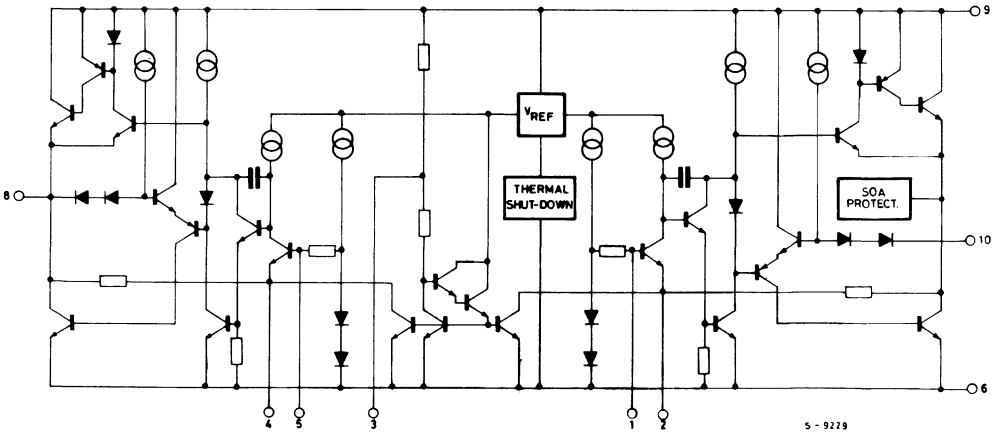
TEST CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

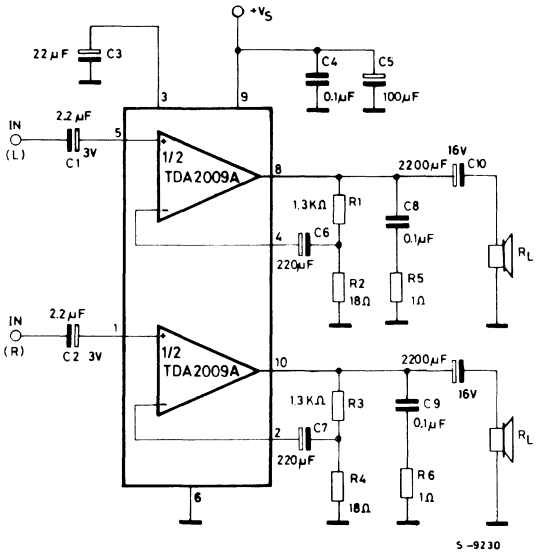
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the stereo application circuit, T_{amb} = 25°C, V_s = 24V, G_v = 36 dB, unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		28	V
V_o	Quiescent output voltage	V_s = 24V			11.5		V
I_d	Total quiescent drain current	V_s = 24V			60	120	mA
P_o	Output power (each channel)	d = 1% V_s = 24V f = 1KHz	R_L = 4Ω R_L = 8Ω		12.5 7		W W
		f = 40Hz to 12.5KHz R_L = 4Ω R_L = 8Ω		10 5			W W
		V_s = 18V f = 1KHz	R_L = 4Ω R_L = 8Ω		7 4		W W
d	Distortion (each channel)	f = 1KHz V_s = 24V P_o = 0.1 to 7W P_o = 0.1 to 3.5W	R_L = 4Ω R_L = 8Ω		0.2 0.1		% %
		V_s = 18V P_o = 0.1 to 5W P_o = 0.1 to 2.5W	R_L = 4Ω R_L = 8Ω		0.2 0.1		% %
CT	Cross talk (ooo)	R_L = ∞	f = 1KHz		60		dB
		R_g = 10KΩ	f = 10KHz		50		dB
V_i	Input saturation voltage (rms)			300			mV
R_i	Input resistance	f = 1KHz non inverting input		70	200		KΩ
f_L	Low frequency roll of (-3dB)	R_L = 4Ω			20		Hz
f_H	High frequency roll off (-3dB)				80		KHz
G_v	Voltage gain (closed loop)	f = 1KHz		35.5	36	36.5	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g = 10KΩ (o)			1.5		μV
		R_g = 10KΩ (oo)			2.5	8	μV
SVR	Supply voltage rejection (each channel)	R_g = 10KΩ f_{ripple} = 100Hz V_{ripple} = 0.5V			55		dB
T_j	Thermal shut-down junction temperature				145		°C

(o) Curve A (oo) 22Hz to 22KHz (ooo) Optimized test box.

Fig. 1 - Test and application circuit (G_v = 36dB)



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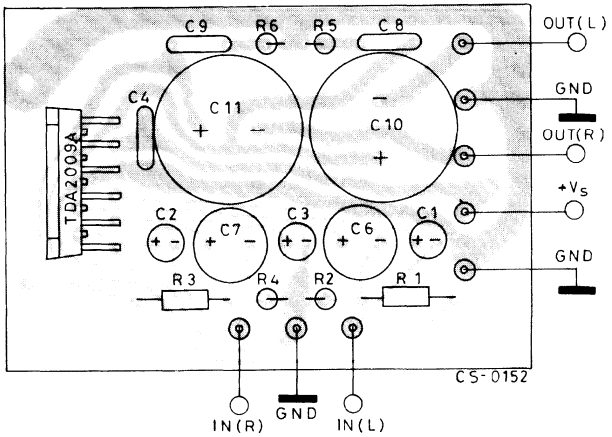


Fig. 3 - Output power vs. supply voltage

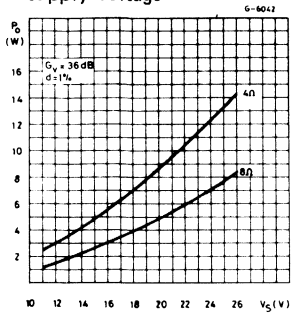


Fig. 4 - Output power vs. supply voltage

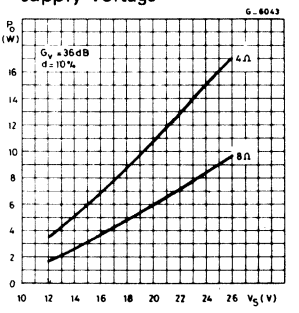


Fig. 5 - Distortion vs. output power

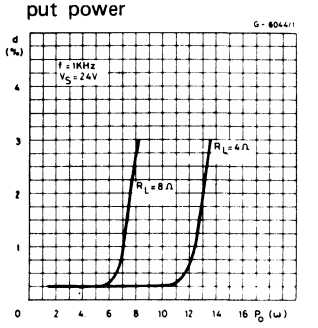


Fig. 6 - Distortion vs. frequency

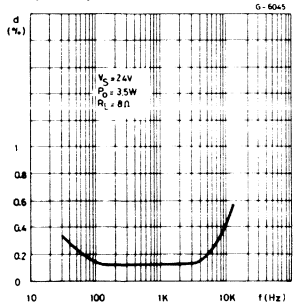


Fig. 7 - Distortion vs. frequency

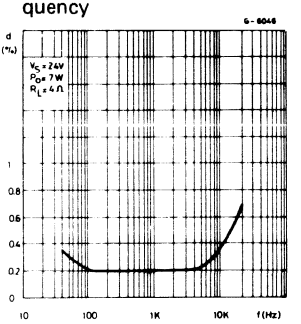


Fig. 8 - Quiescent current vs. supply voltage

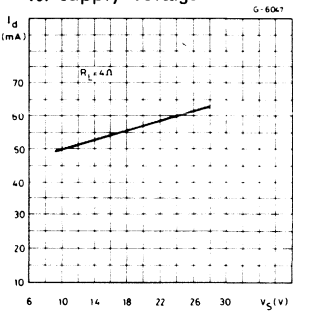


Fig. 9 - Supply voltage rejection vs. frequency

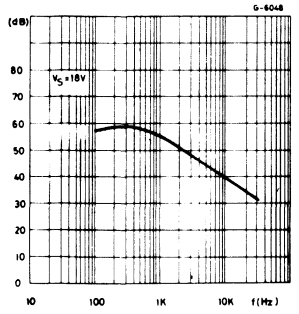


Fig. 10 - Total power dissipation and efficiency vs. output power

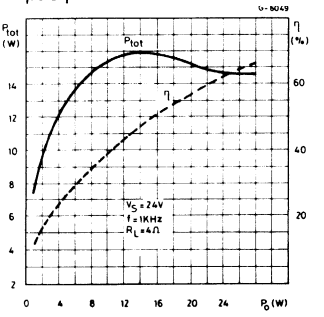
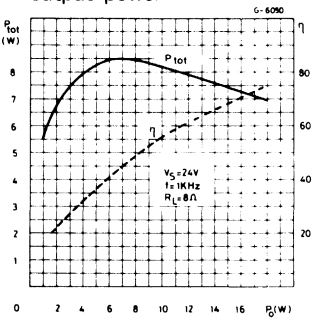


Fig. 11 - Total power dissipation and efficiency vs. output power



APPLICATION INFORMATION

Fig. 12 - Example of muting circuit

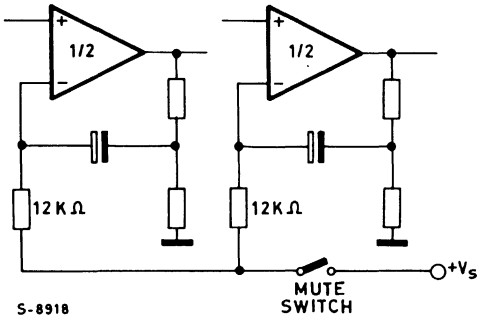


Fig. 13 - 10W + 10W stereo amplifier with tone balance and loudness control

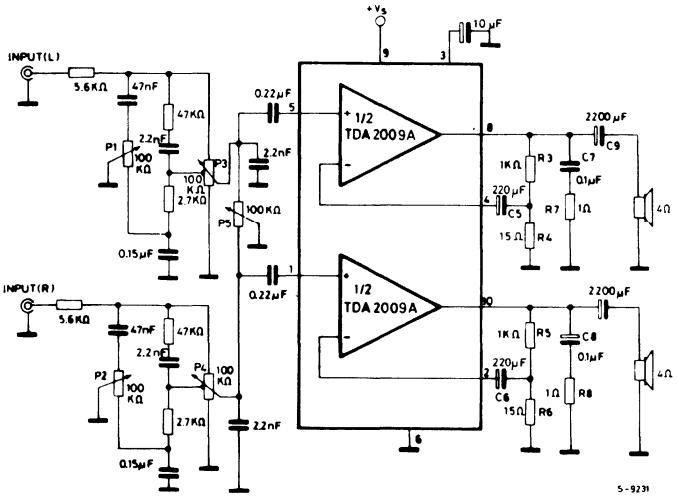
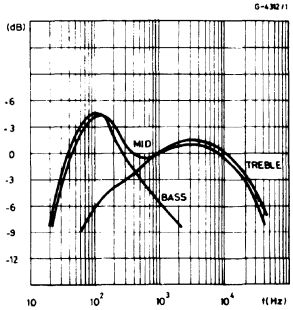


Fig. 14 - Tone control response (circuit of fig. 13)



APPLICATION INFORMATION (continued)

Fig. 15 - High quality 20 + 20W two way amplifier for stereo music center (one challel only)

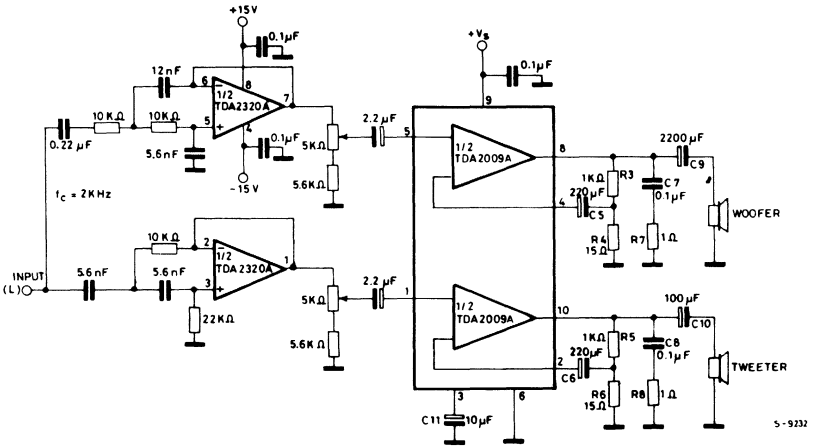


Fig. 16 - 18 W bridge amplifier (d = 1%, G_v = 40dB)

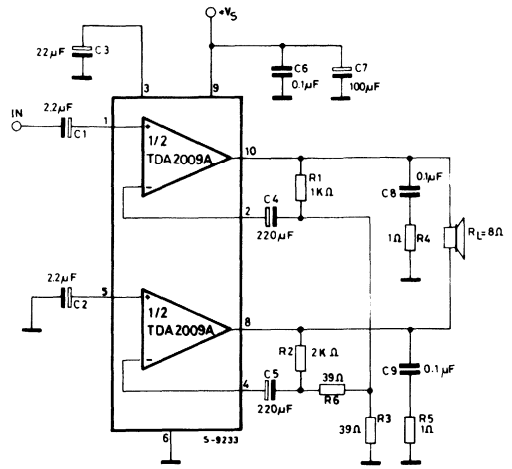
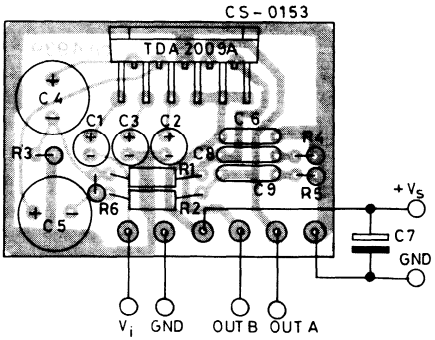


Fig. 17 - P.C. board and components layout of the circuit of fig. 16 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.2KΩ	Close loop gain setting (*)	Increase of gain	Decrease of gain
R2 and R4	18KΩ		Decrease of gain	Increase of gain
R5 and R6	1Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22μF	Ripple rejection	Better SVR. Increase of the Switch-on time	Degradation of SVR
C6 and C7	220μF	Feedback input DC decoupling.		
C8 and C9	0.1μF	Frequency stability		Danger of oscillation
C10 and C11	1000μF to 2200μF	Output DC decoupling.		Higher low-frequency cut-off

(*) Closed loop gain must be higher than 26dB

BUILD-IN PROTECTION SYSTEMS

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_o are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 18 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Short circuit (AC Conditions). The TDA2009A can withstand an accidental short circuit from the output and ground made by a wrong connection during normal play operation.

Fig. 18 - Maximum allowable power dissipation vs. ambient temperature

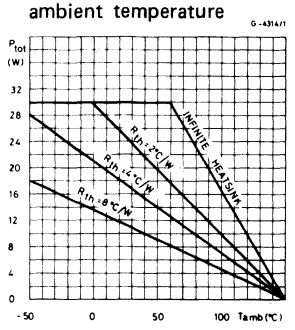


Fig. 19 - Output power vs. case temperature

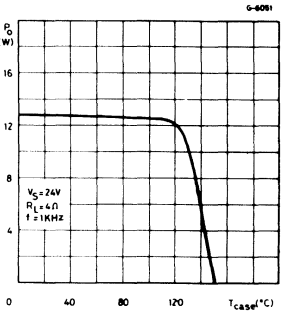
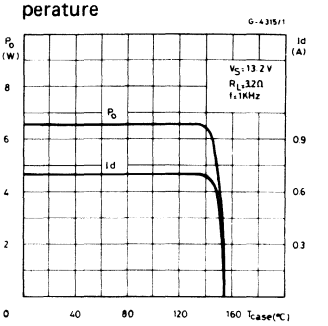


Fig. 20 - Output power and drain current vs. case temperature



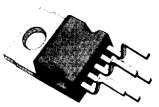
MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT®package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

TDA2030

14W Hi-Fi AUDIO AMPLIFIER

The TDA2030 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at 14V/4Ω; at ± 14V the guaranteed output power is 12W on a 4Ω load and 8W on a 8Ω (DIN45500). The TDA2030 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.



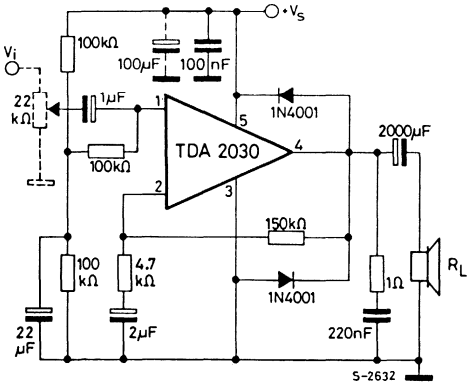
Pentawatt

ORDERING NUMBER: TDA2030H
TDA2030V

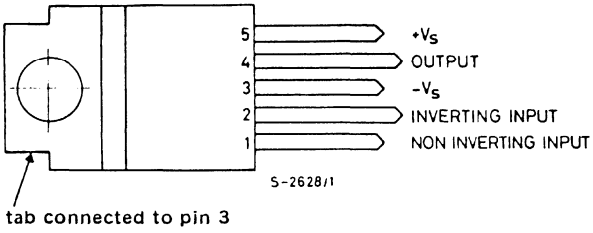
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

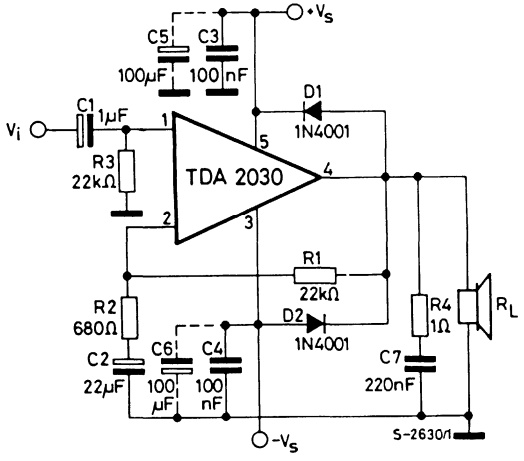
TYPICAL APPLICATION



CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 18	V
I_d	Quiescent drain current	$V_s = \pm 18V$		40	60	mA
I_b	Input bias current			0.2	2	μA
V_{os}	Input offset voltage			± 2	± 20	mV
I_{os}	Input offset current			± 20	± 200	nA
P_o	Output power	d = 0.5% G_v= 30 dB f = 40 to 15 000 Hz R_L= 4Ω R_L= 8Ω	 12 8	 14 9		 W W
		d = 10% G_v= 30 dB f = 1 kHz R_L= 4Ω R_L= 8Ω		 18 11		 W W
d	Distortion	P_o= 0.1 to 12W R_L= 4Ω G_v= 30 dB f = 40 to 15 000 Hz		0.2	0.5	%
		P_o = 0.1 to 8W R_L= 8Ω G_v= 30 dB f = 40 to 15 000 Hz		0.1	0.5	%
B	Power Bandwidth (-3 dB)	G_v= 30 dB P_o= 12W R_L= 4Ω	10 to 140 000			Hz
R_i	Input resistance (pin 1)		0.5	5		MΩ
G_v	Voltage gain (open loop)			90		dB
G_v	Voltage gain (closed loop)	f = 1 kHz	29.5	30	30.5	dB
e_N	Input noise voltage	B = 22 Hz to 22 KHz		3	10	μV
i_N	Input noise current			80	200	pA
SVR	Supply voltage rejection	R_L= 4Ω G_v= 30 dB R_g= 22 kΩ V_{ripple}= 0.5 V_{eff} f_{ripple}= 100 Hz	40	50		dB
I_d	Drain current	P_o= 14W R_L= 4Ω P_o= 9W R_L= 8Ω		900 500		mA mA
T_j	Thermal shut-down junction temperature			145		°C

Fig. 1 - Output power vs. supply voltage

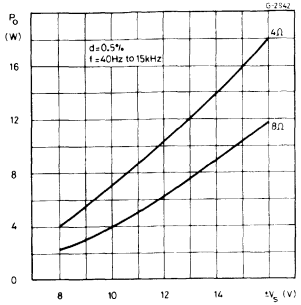


Fig. 2 - Output power vs. supply voltage

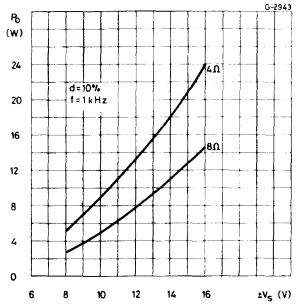


Fig. 3 - Distortion vs. output power

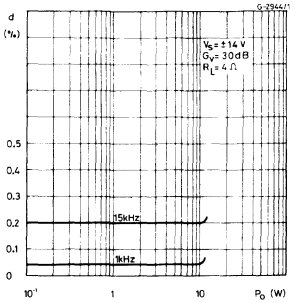


Fig. 4 - Distortion vs. output power

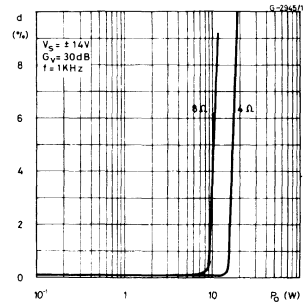


Fig. 5 - Distortion vs. output power

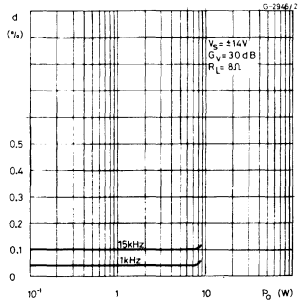


Fig. 6 - Distortion vs. frequency

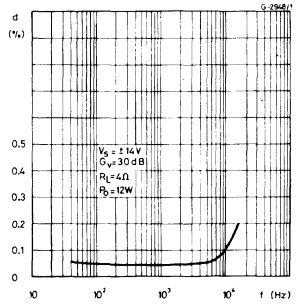


Fig. 7 - Distortion vs. frequency

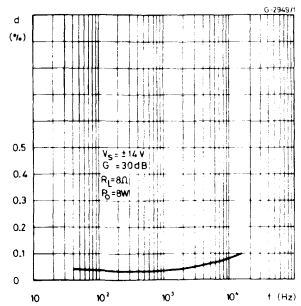


Fig. 8 - Frequency response with different values of the rolloff capacitor C8 (see fig. 13)

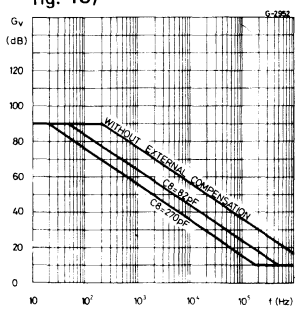


Fig. 9 - Quiescent current vs. supply voltage

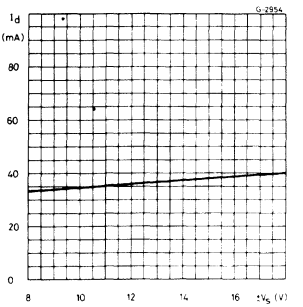


Fig. 10 - Supply voltage rejection vs. voltage gain

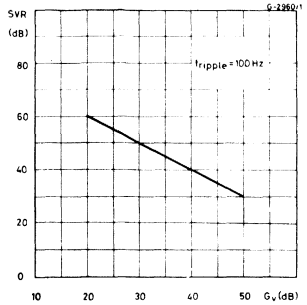


Fig. 11 - Power dissipation and efficiency vs. output power

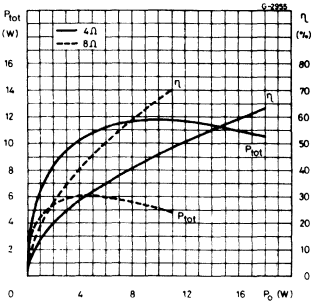
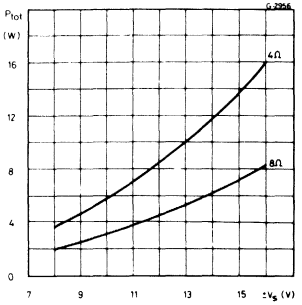


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)



APPLICATION INFORMATION

Fig. 13 - Typical amplifier with split power supply

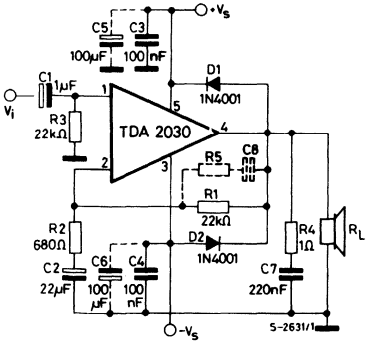
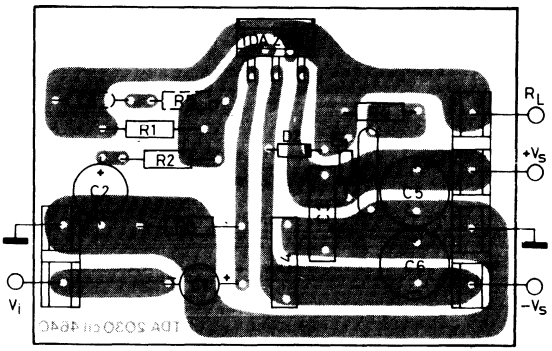


Fig. 14 - P.C. board and component layout for the circuit of fig. 13 (1:1 scale)



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APPLICATION INFORMATION (continued)

Fig. 15 - Typical amplifier with single power supply

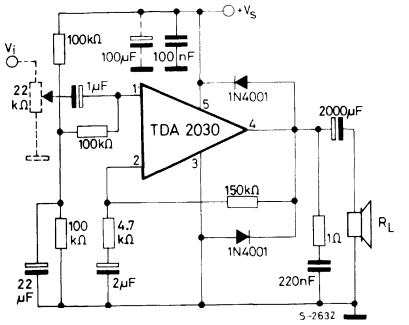


Fig. 16 - P.C. board and component layout for the circuit of fig. 15 (1:1 scale)

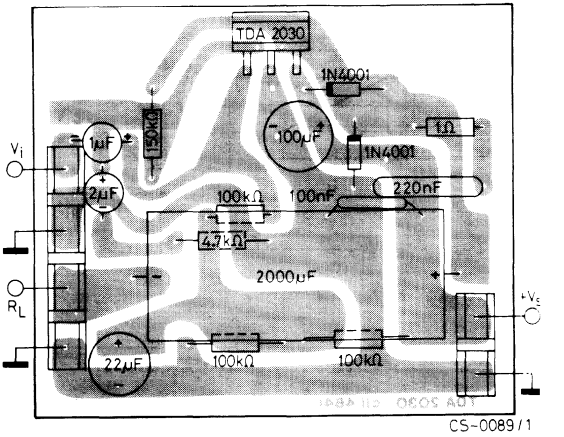
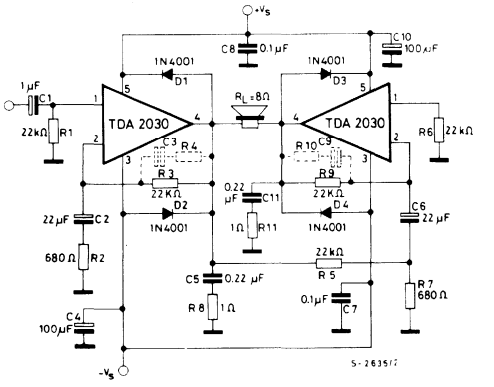


Fig. 17 - Bridge amplifier configuration with split power supply (P_o = 28W, V_s = ±14V)



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in Fig. 16 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application suggestions

The recommended values of the components are those shown on application circuit of fig. 13. Different values can be used. The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R2	680 Ω	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillat. at high frequencies with induct. loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μ F	Inverting DC decoupling		Increase of low frequencies cutoff
C3,C4	0.1 μF	Supply voltage bypass		Danger of oscillation
C5,C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0.22 μF	Frequency stability		Danger of oscillat.
C8	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D1,D2	1N4001	To protect the device against output voltage spikes		

(*) Closed loop gain must be higher than 24dB

SHORT CIRCUIT PROTECTION

The TDA2030 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (Fig. 2). This function can therefore be considered as being peak power limiting rather than simple current limiting.
It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

Fig. 18 - Maximum output current vs. voltage [V_{CEsat}] across each output transitor

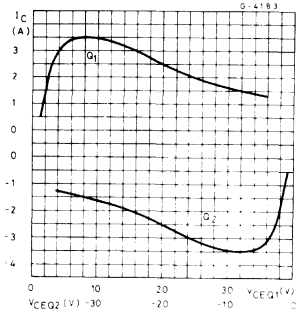
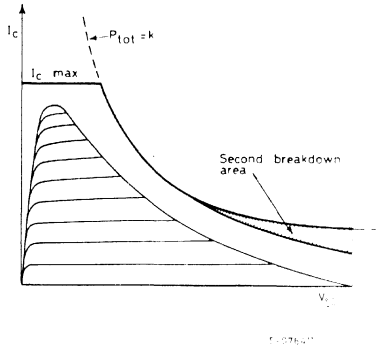


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation at the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

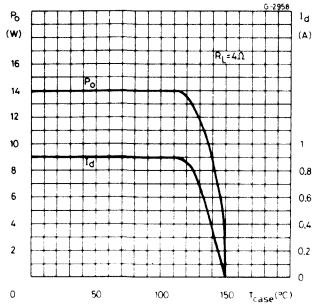


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)

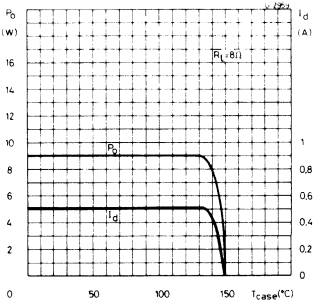


Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

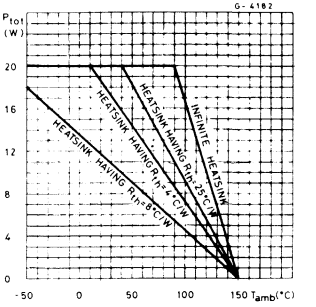
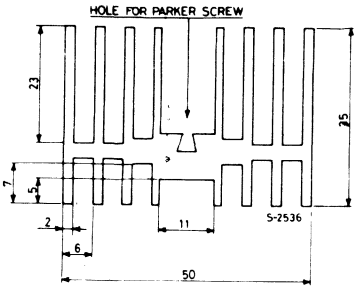


Fig. 23 - Example of heat-sink



Dimension : suggestion.

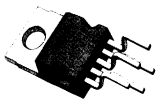
The following table shows the length that the heatsink in fig. 23 must have for several values of P_{tot} and R_{th}.

P_{tot}(W)	12	8	6
Length of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

TDA2030A

18W Hi-Fi AMPLIFIER AND 35W DRIVER

The TDA2030A is a monolithic IC in Pentawatt® package intended for use as low frequency class AB amplifier.
With $V_{s\,max}$ = 44V it is particularly suited for more reliable applications without regulated supply and for 35W driver circuits using low-cost complementary pairs.
The TDA2030A provides high output current and has very low harmonic and cross-over distortion.
Further the device incorporates a short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included



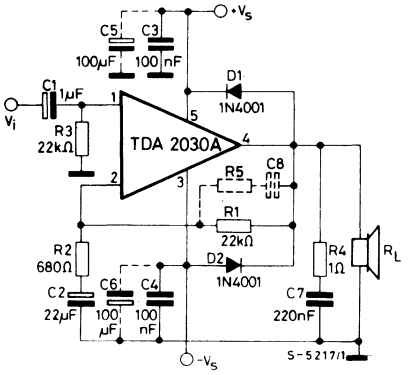
Pentawatt

ORDERING NUMBERS: TDA2030A
TDA2030AH

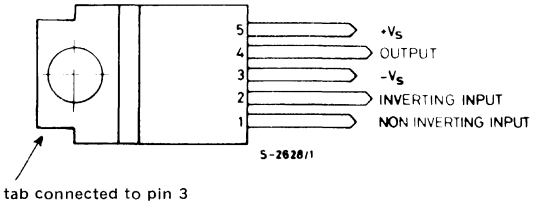
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 22	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Total power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

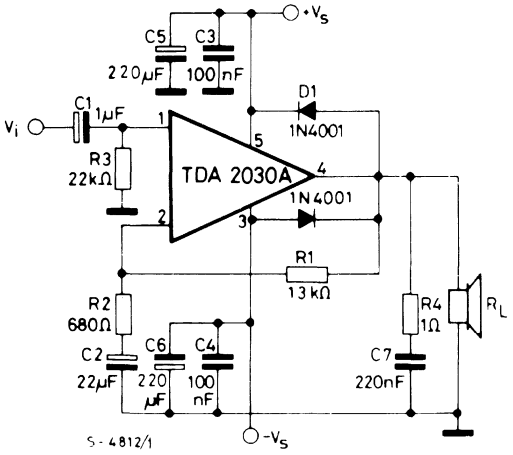
TYPICAL APPLICATION



CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= ±16V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 6		± 22	V
I_d	Quiescent drain current				50	80	mA
I_b	Input bias current	V_s = ± 22V			0.2	2	μA
V_{os}	Input offset voltage				± 2	± 20	mV
I_{os}	Input offset current				± 20	± 200	nA
P_o	Output power	d = 0.5% G_v = 26 dB f = 40 to 15000 Hz R_L= 4 Ω R_L= 8 Ω		15 10	18 12		W
		V_s = ± 19V R_L= 8Ω		13	16		
BW	Power bandwidth	P_o= 15W R_L= 4 Ω			100		KHz
SR	Slew Rate				8		V/μsec
G_v	Open loop voltage gain	f = 1 KHz			80		dB
G_v	Closed loop voltage gain			25.5	26	26.5	dB
d	Total harmonic distortion	P_o= 0.1 to 14W R_L= 4 Ω f = 40 to 15000 Hz f = 1 KHz			0.08 0.03		%
		P_o = 0.1 to 9W R_L= 8 Ω f = 40 to 15000 Hz			0.05		%
d_2	Second order CCIF intermodulation distortion	P_o= 4W R_L= 4Ω	f_2-f_1 = 1 KHz		0.03		%
d_3	Third order CCIF intermodulation distortion	f_1= 14 KHz f_2= 15 KHz	2 f_1-f_2= 13KHz		0.08		%
e_N	Input noise voltage	B = curve A			2		μV
		B = 22 Hz to 22 KHz			3	10	
i_N	Input noise current	B = curve A			50		pA
		B = 22 Hz to 22 KHz			80	200	
S/N	Signal to noise ratio	R_L= 4Ω R_g= 10 KΩ B = curve A	P_o = 15W		106		dB
			P_o = 1W		94		

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
R_i	Input resistance (pin 1)	(open loop)	f = 1 KHz	0.5	5		MΩ
SVR	Supply voltage rejection	R_L = 4 Ω R_g = 22 KΩ	G_v = 26 dB f = 100 Hz		54		dB
T_j	Thermal shut-down junction temperature				145		°C

Fig. 1 - Single supply amplifier

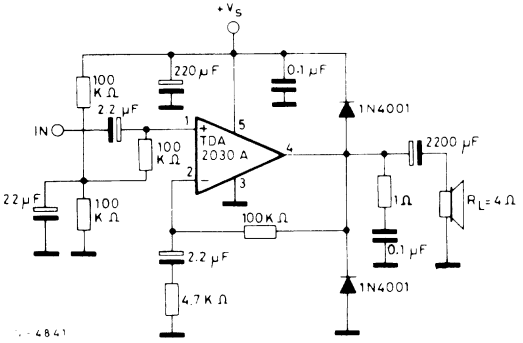


Fig. 2 - Open loop-frequency response

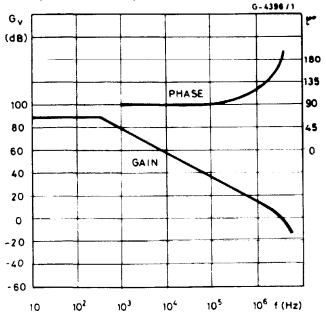


Fig. 3 - Output power vs. supply voltage

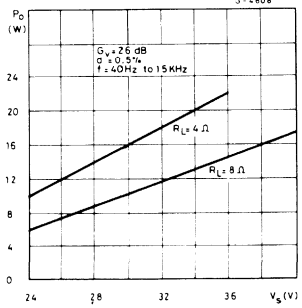
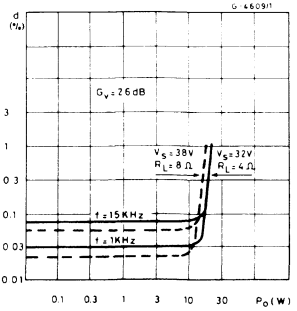


Fig. 4 - Total harmonic distortion vs. output power(*)



*) Test using noise filters.

Fig. 5 - Two tone CCIF intermodulation distortion

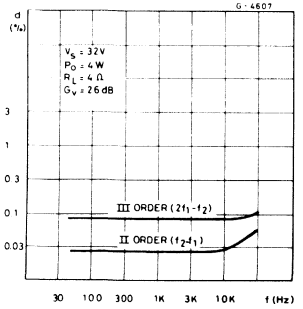


Fig. 6 - Large signal frequency response

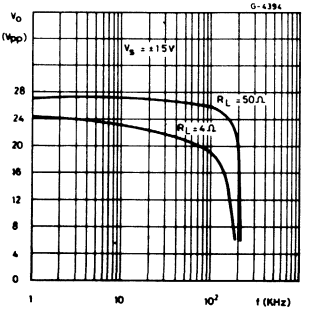


Fig. 7 - Maximum allowable power dissipation vs. ambient temperature

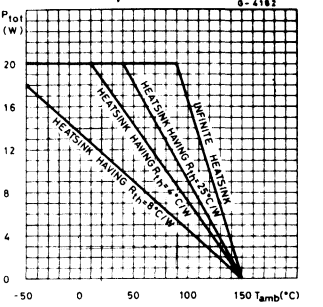


Fig. 8 - Single supply high power amplifier (TDA 2030A + BD907/BD908)

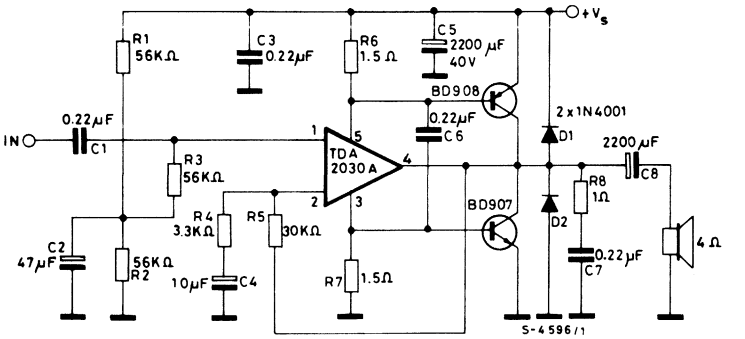
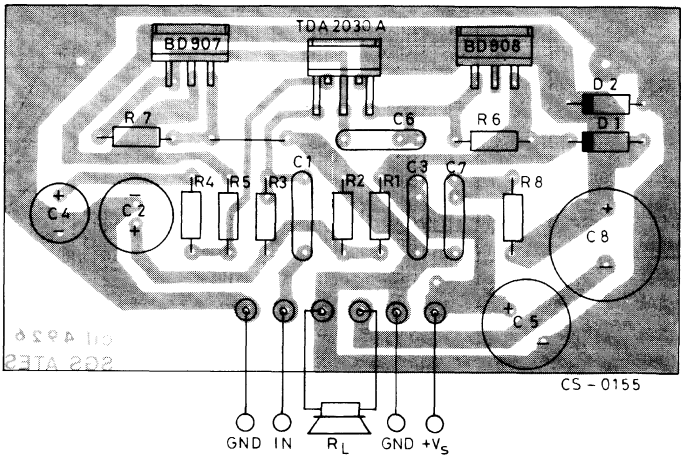


Fig. 9 - P.C. board and component layout for the circuit of fig. 8 (1:1 scale)



Typical performance of the circuit of fig. 8

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage				36	44	V
I_d	Quiescent drain current	V_s = 36V			50		mA
P_o	Output power	d = 0.5% R_L = 4Ω f = 40Hz to 15KHz	V_s = 39V		35		W
			V_s = 36V		28		
		d = 10%; f = 1KHz	V_s = 39V		44		W
		R_L = 4Ω	V_s = 36V		35		
G_v	Voltage gain	f = 1 KHz		19.5	20	20.5	dB
SR	Slew Rate				8		V/μsec
d	Total harmonic distortion		f = 1KHz		0.02		%
		P_o = 20W	f = 40 Hz to 15 KHz		0.05		
V_i	Input sensitivity	G_v = 20 dB P_o = 20W	f = 1 KHz R_L = 4Ω		890		mV
S/N	Signal to noise ratio	R_L = 4Ω R_g = 10 KΩ B = curve A	P_o = 25W		108		dB
			P_o = 4W		100		

Fig. 10 - Output power vs. supply voltage

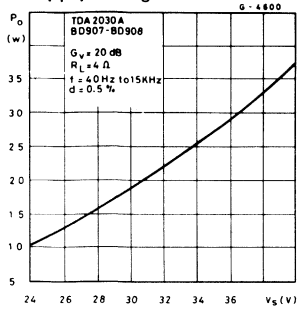


Fig. 11 - Total harmonic distortion vs. output power

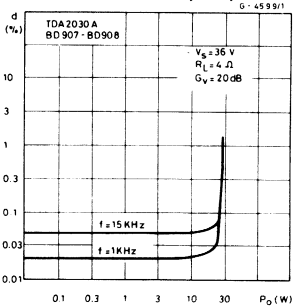


Fig. 12 - Output power vs. input level

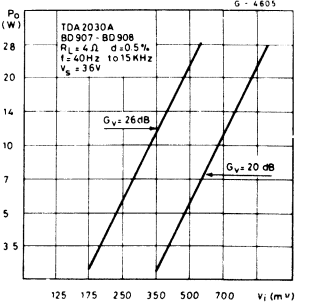


Fig. 13 - Power dissipation vs. output power

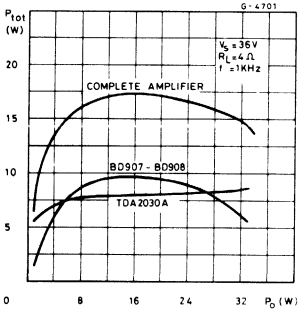


Fig. 14 - Typical amplifier whit split power supply

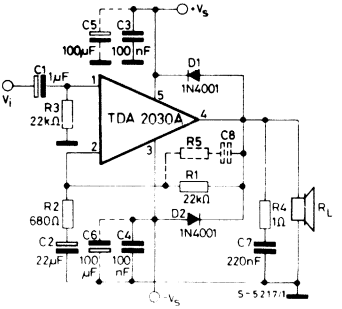


Fig. 15 - P.C. board and component layout for the circuit of fig. 14 (1 : 1 scale)

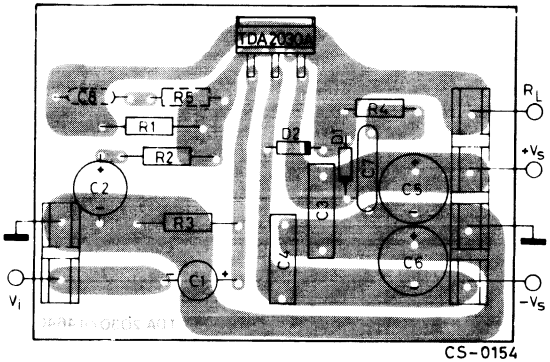


Fig. 16 - Bridge amplifier whit split power supply (P_o= 34W, V_s= ±16V)

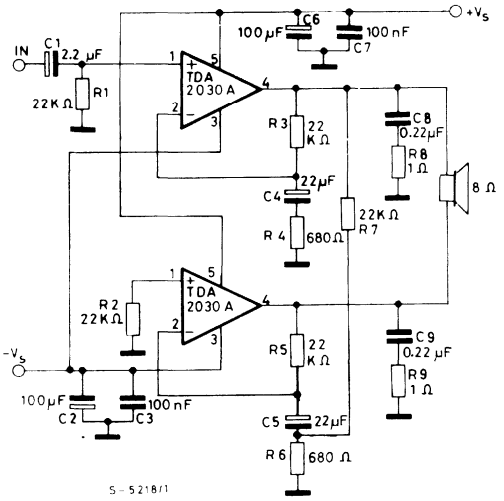
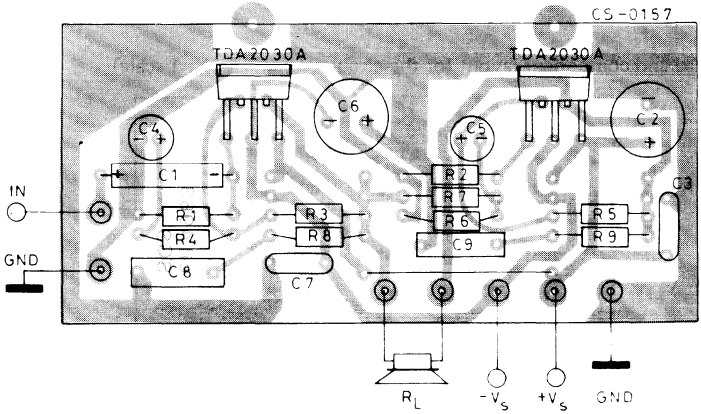


Fig. 17 - P.C. board and component layout for the circuit in fig. 16 (1:1 scale)



Multiway speaker systems and active boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two or three bands.
To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segmento of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see Fig. 18). As an example, a 100W three-way system with crossover frequencies of 400Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.
Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power less;
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance.

Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers.
In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6dB/octave) can be recommended.
The result obtained are excellent beceuse this is the best type of audio filter and the only one free from phase and transient distortion.
The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.
A more effective solution, named "Active Power Filter" by SGS is shown in Fig. 19.
The proposed circuit can realize combined power amplifiers and 12dB/octave or 18dB/octave high-pass or low-pass filters.
In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (-) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

Fig. 18 - Power distribution vs. frequency

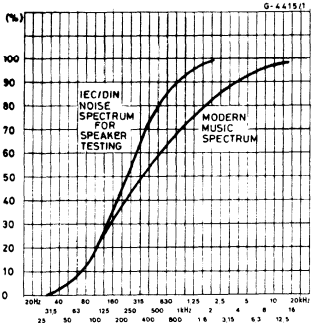
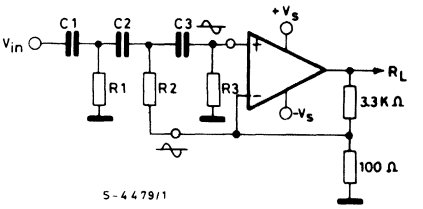


Fig. 19 - Active power filter



The component values calculated for $f_c = 900Hz$ using a Bessel 3rd order Sallen and Key structure are:

$C_1 = C_2 = C_3$	R_1	R_2	R_3
22nF	8.2KΩ	5.6KΩ	33KΩ

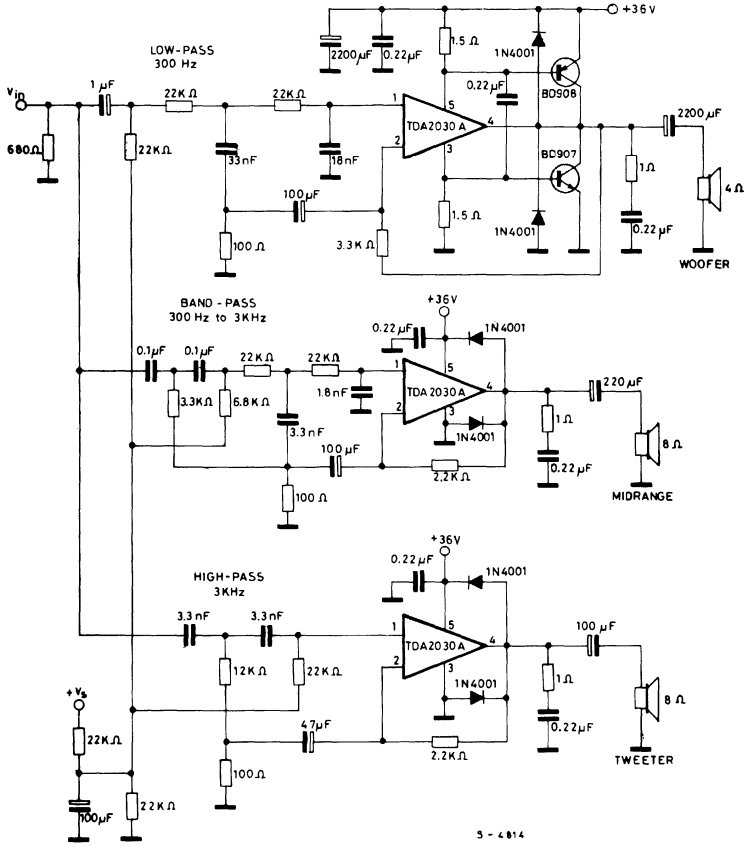
Using this type of crossover filter, a complete 3-way 60W active loudspeaker system is shown in Fig. 20.

It employs 2nd order Buttherworth filters with the crossover frequencies equal to 300Hz and 3KHz.

The midrange section consists of two filters, a high pass circuit followed by a low pass network. With $V_s = 36V$ the output power delivered to the woofer is 25W at d = 0.06% (30W at d = 0.5%). The power delivered to the midrange and the tweeter can be optimized in the design phase taking in account the loudspeaker efficiency and impedance ($R_L = 4\Omega$ to 8Ω).

It is quite common that midrange and tweeter speakers have an efficiency 3dB higher than woofers.

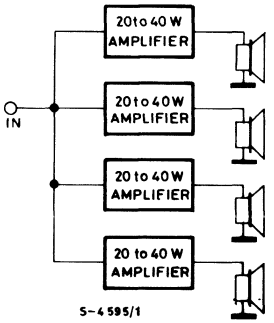
Fig. 20 - 3 way 60W active loudspeaker system ($V_s = 36V$)



Musical instruments amplifiers

Another important field of application for active systems is music.
In this area the use of several medium power amplifiers is more convenient than a single high power amplifier, and it is also more realiable. A typical example (see Fig. 21) consist of four amplifiers each driving a low-cost, 12 inch loudspeaker. This application can supply 80 to 160W rms.

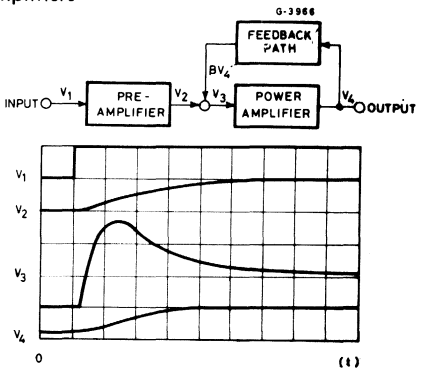
Fig. 21 - High power active box for musical instrument



Transient intermodulation distortion (TIM)

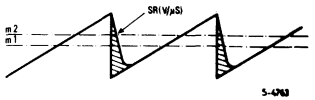
Transient intermodulation distortion is an unfortunate phenomen associated with negative-feedback amplifiers. When a feedback amplifier receives an input signal which rises very steeply, i.e. contains high-frequency components, the feedback can arrive too late so that the amplifiers overloads and a burst of intermodulation distortion will be produced as in Fig. 22. Since transients occur frequently in music this obviously a problem for the designer of audio amplifiers. Unfortunately, heavy negative feedback is frequency used to reduce the total harmonic distortion of an amplifier, which tends to aggravate the transient intermodulation (TIM situation. The best known method for the measurement of TIM consists of feeding sine waves superimposed onto square waves, into the amplifier under test. The output spectrum is then examined using a

Fig. 22 - Overshoot phenomenon in feedback amplifiers



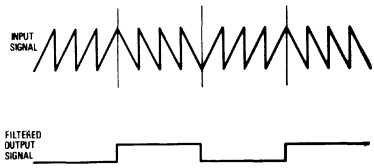
spectrum analyser and compared to the input. This method suffers from serious disadvantages: the accuracy is limited, the measurement is a rather delicate operation and an expensive spectrum analyser is essential. A new approach (see Technical Note 143) applied by SGS to monolithic amplifiers measurement is fast cheap- it requires nothing more sophisticated than an oscilloscope - and sensitive - and it can be used down to the values as low as 0.002% in high power amplifiers.
The "inverting-sawtooth" method of measurement is based on the response of an amplifier to a 20KHz sawtooth waveform. The amplifier has no difficulty following the slow ramp but it cannot follow the fast edge. The output will follow the upper line in Fig. 23 cutting of the shaded area and thus increasing the mean level. If this output signal is filtered to remove the sawtooth, direct voltage remains which indicates the amount of TIM distortion, although it is difficult to measure because it is indistinguishable from the DC offset of the amplifier. This problem is neatly avoided in the IS-TIM method

Fig. 23 - 20KHz sawtooth waveform



by periodically inverting the sawtooth waveform at a low audio frequency as shown in Fig. 24. In the case of the sawtooth in Fig. 25 the mean level was increased by the TIM distortion, for a sawtooth in the other direction the opposite is true.

Fig. 24 - Inverting sawtooth waveform

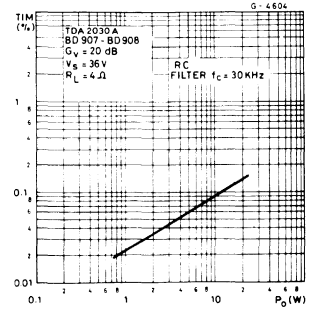


The result is an AC signal at the output whole peak-to-peak value is the TIM voltage, which can be measured easily with an oscilloscope. If the peak-to-peak value of the signal and the peak-to-peak of the inverting sawtooth are measured, the TIM can be found very simply from:

$$TIM = \frac{V_{out}}{V_{sawtooth}} \cdot 100$$

In Fig. 25 the experimental results are shown for the 30W amplifier using the TDA2030A as a driver and a low-cost complementary pair. A simple RC filter on the input of the amplifier to limit the maximum signal slope (SS) is an effective way to reduce TIM.

Fig. 25 - TIM distortion vs. output power



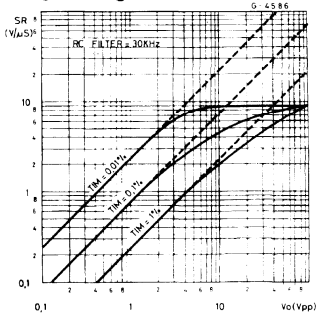
The diagram of Fig. 26 originated by SGS can be used to find the Slew-Rate (SR) required for a given output power or voltage and a TIM design target.

For example if an anti-TIM filter with a cutoff at 30KHz is used and the max. peak-to-peak output voltage is 20V then, referring to the diagram, a Slew-Rate of 6V/μs is necessary for 0.1% TIM.

As shown Slew-Rates of above 10V/μs do not contribute to a further reduction in TIM.

Slew-Rates of 100/μs are not only useless but also a disadvantage in Hi-Fi audio amplifiers because they tend to turn the amplifier into a radio receiver.

Fig. 26 - TIM design diagram (f_C = 30KHz)



Power supply

Using monolithic audio amplifier with non-regulated supply voltage it is important to design the power supply correctly. In any working case it must provide a supply voltage less than the maximum value fixed by the IC breakdown voltage.

It is essential to take into account all the working conditions, in particular mains fluctuations and supply voltage variations with and without load. The TDA2030A ($V_{s\,max}$ = 44V) is particularly suitable for substitution of the standard IC power amplifiers (with $V_{s\,max}$ = 36V) for more reliable applications.

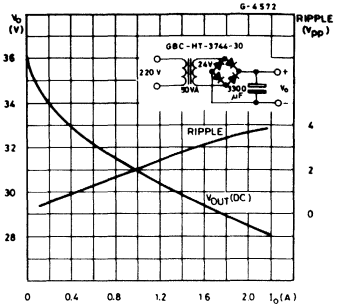
An example, using a simple full-wave rectifier followed by a capacitor filter, is shown in the table and in the diagram of Fig. 27.

A regulated supply is not usually used for the power output stages because of its dimensioning must be done taking into account the power to supply in the signal peaks. They are only a small percentage of the total music signal, with consequently large overdimensioning of the circuit.

Even if with a regulated supply higher output power can be obtained (V_s is constant in all working conditions), the additional cost and power dissipation do not usually justify its use. Using non-regulated supplies, there are fewer designe restriction. In fact, when signal peaks are present, the capacitor filter acts as a flywheel supplying the required energy.

In average conditions, the continuous power supplied is lower. The music power/continuous power ratio is greater in this case than for the case of regulated supplied, with space saving and cost reduction.

Fig. 27 - DC characteristics of 50W non-regulated supply



Mains (220V)	Secondary voltage	DC output voltage (V_O)		
		I_O = 0	I_O = 0.1A	I_O = 1A
+20%	28.8V	43.2V	42V	37.5V
+15%	27.6V	41.4V	40.3V	35.8V
+10%	26.4V	39.6V	38.5V	34.2V
–	24V	36.2V	35V	31V
-10%	21.6V	32.4V	31.5V	27.8V
-15%	20.4V	30.6V	29.8V	26V
-20%	19.2V	28.8V	28V	24.3V

Application suggestion

The recommended values of the components are those shown on application circuit of Fig. 14. Different values can be used. The following table can help the designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22KΩ	Closed loop gain setting.	Increase of gain.	Decrease of gain. *
R2	680Ω	Closed loop gain setting.	Decrease of gain. *	Increase of gain.
R3	22KΩ	Non inverting input biasing.	Increase of input impedance.	Decrease of input impedance.
R4	1Ω	Frequency stability.	Danger of oscillation at high frequencies with inductive loads.	
R5	≅ 3 R2	Upper frequency cutoff.	Poor high frequencies attenuation.	Danger of oscillation.
C1	1μF	Input DC decoupling.		Increase of low frequencies cutoff.
C2	22μF	Inverting DC decoupling.		Increase of low frequencies cutoff.
C3, C4	0.1μF	Supply voltage bypass.		Danger of oscillation.
C5, C6	100μF	Supply voltage bypass.		Danger of oscillation.
C7	0.22μF	Frequency stability.		Larger bandwidth.
C8	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff.	Smaller bandwidth.	Larger bandwidth.
D1, D2	1N4001	To protect the device against output voltage spikes.		

* The value of closed loop gain must be higher than 24dB.

SHORT CIRCUIT PROTECTION

The TDA2030A has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUT-DOWN

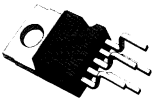
The presence of a thermal limiting circuit offers the following advantages:

1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

TDA2040

20W Hi-Fi AUDIO POWER AMPLIFIER

The TDA2040 is a monolithic integrated circuit in Pentawatt® package, intended for use as an audio class AB amplifier. Typically it provides 22W output power (d = 0.5%) at $V_s = 32V/4\Omega$. The TDA2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.



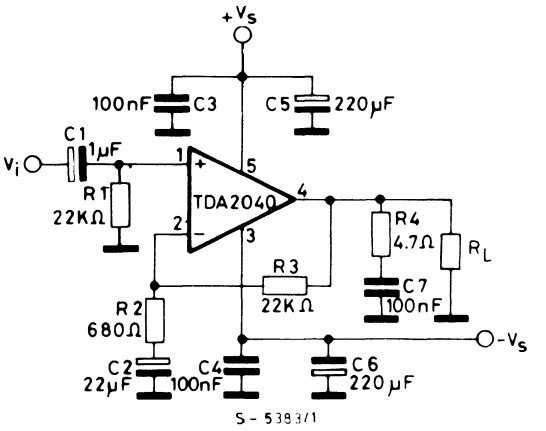
Pentawatt

ORDERING NUMBER: TDA2040V
TDA2040H

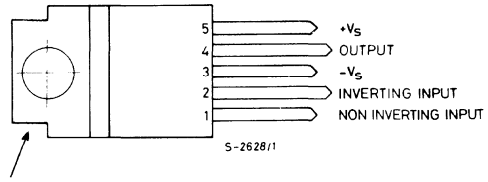
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o.	Output peak current (internally limited)	4	A
P_{tot}	Power dissipation at $T_{case} = 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

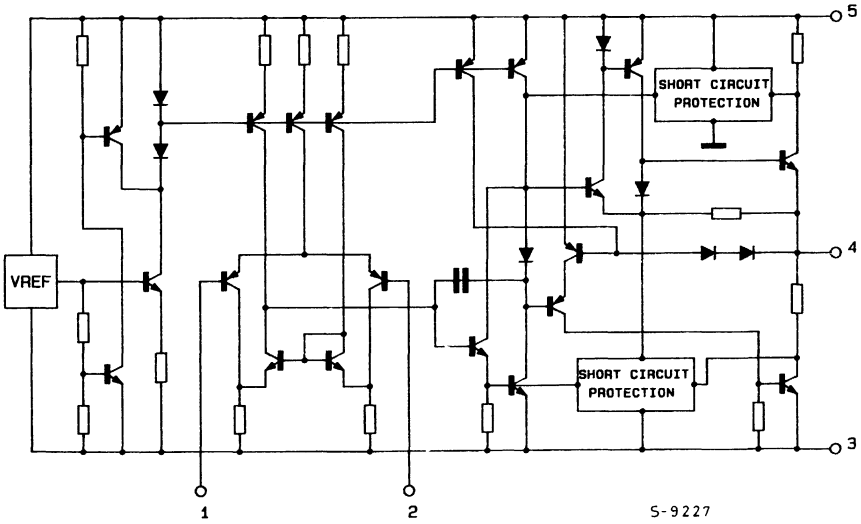
TEST CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 16V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 2.5		± 20	V
I_d	Quiescent drain current	$V_s = \pm 4.5V$			30	mA
		$V_s = \pm 20V$		45	100	mA
I_b	Input bias current	$V_s = \pm 20V$		0.3	1	μA
V_{os}	Input offset voltage	$V_s = \pm 20V$		± 2	± 20	mV
I_{os}	Input offset current				±200	nA
P_o	Output power	d = 0.5% f = 1 KHz $T_{case} = 60°C$ $R_L = 4\Omega$	20	22		W
		d = 0.5% f = 1 KHz $T_{case} = 60°C$ $R_L = 8\Omega$		12		W
		f = 15 KHz $R_L = 4\Omega$	15	18		W
BW	Power bandwidth	$P_o = 1W$ $R_L = 4\Omega$		100		KHz
G_v	Open loop voltage gain	f = 1 KHz		80		dB
G_v	Closed loop voltage gain	f = 1 KHz	29.5	30	30.5	dB
d	Total harmonic distortion	$P_o = 0.1$ to 10W $R_L = 4\Omega$ f = 40 to 15000Hz		0.08		%
		$P_o = 0.1$ to 10W $R_L = 4\Omega$ f = 1 KHz		0.03		%
e_N	Input noise voltage	B = curve A		2		μV
		B = 22 Hz to 22 KHz		3	10	μV
i_N	Input noise current	B = curve A		50		pA
		B = 22 Hz to 22 KHz		80	200	pA
R_i	Input resistance (pin 1)		0.5	5		MΩ
SVR	Supply voltage rejection	$R_L = 4\Omega$ $G_v = 30$ dB $R_g = 22$ KΩ f = 100 Hz $V_{ripple} = 0.5\ V_{rms}$	40	50		dB
η	Efficiency	f = 1 KHz $P_o = 12W$ $R_L = 8\Omega$		66		%
		f = 1 KHz $P_o = 22W$ $R_L = 4\Omega$		63		%
T_j	Thermal shut-down junction temperature			145		°C

Fig. 1 - Output power vs. supply voltage

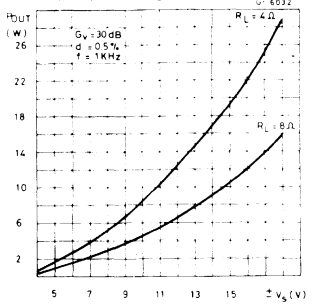


Fig. 2 - Output power vs. supply voltage

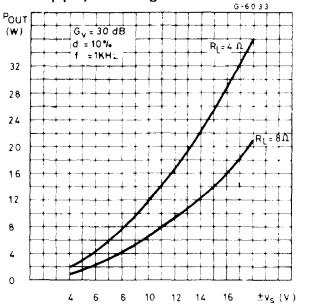


Fig. 3 - Output power vs. supply voltage

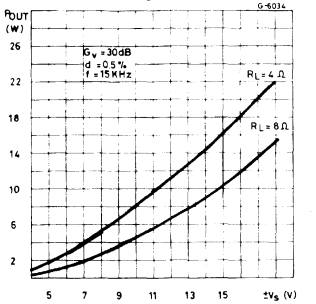


Fig. 4 - Distortion vs. frequency

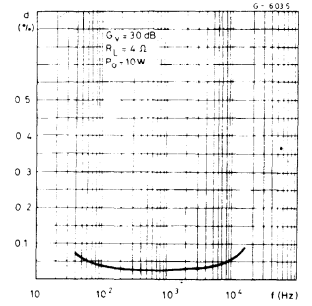


Fig. 5 - Supply voltage rejection vs. frequency

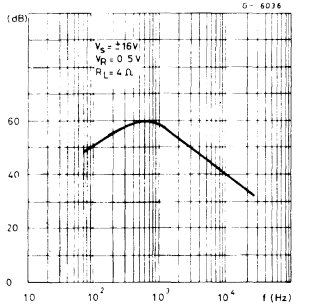


Fig. 6 - Supply voltage rejection vs. voltage gain

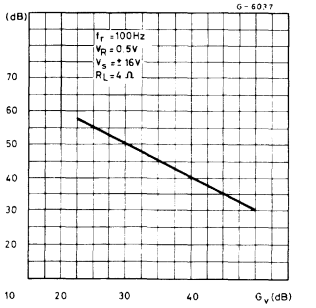


Fig. 7 - Quiescent drain current vs. supply voltage

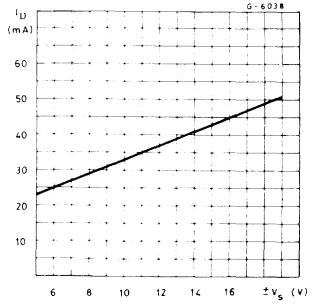


Fig. 8 - Open loop gain vs. frequency

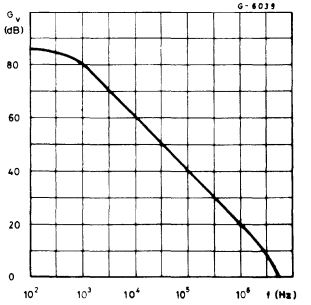
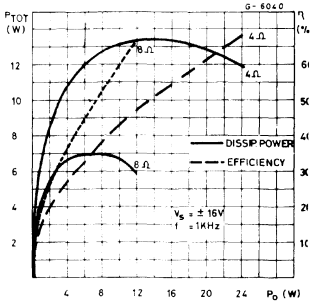
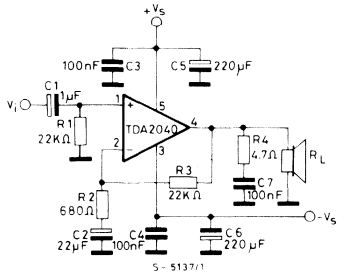


Fig. 9 - Power dissipation vs. output power



APPLICATION INFORMATION

Fig. 10 - Amplifier with split power supply (*)



V_s = ± 16V
R_L = 4Ω
P_o ⩾ 15W (d = 0.5%)

Fig. 11 - P.C. board and components layout of the circuit of fig. 10 (1:1 scale)

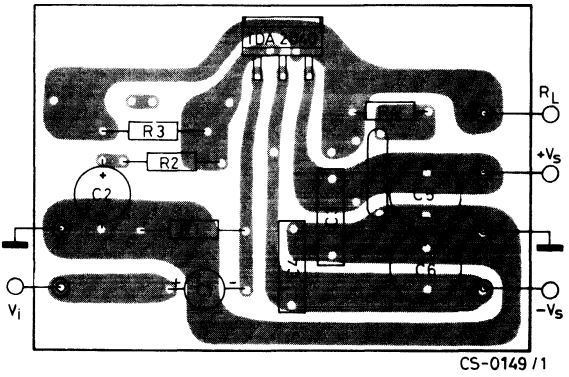
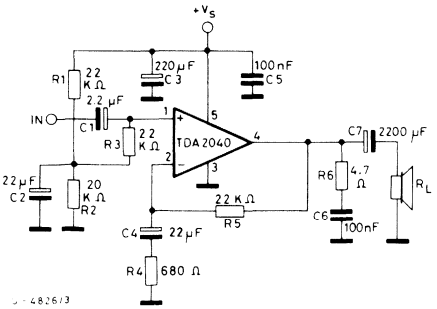
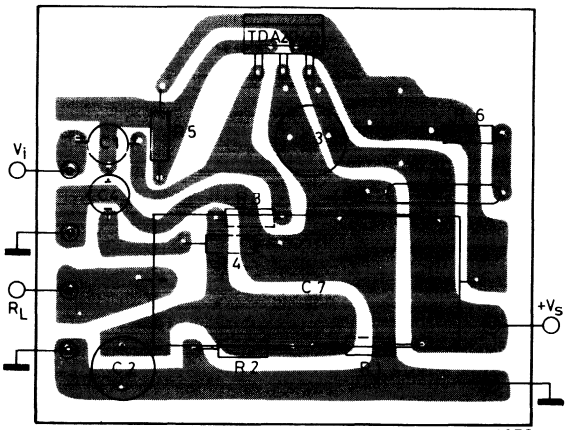


Fig. 12 - Amplifier with single supply (*)



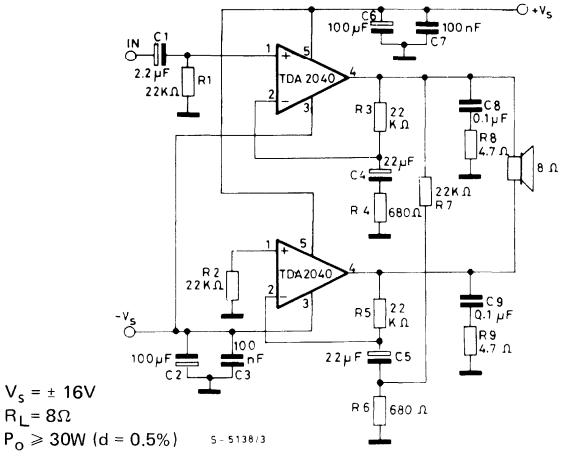
* In the case of highly inductive loads protection diodes may be necessary.

Fig. 13 - P.C. board and components layout of the circuit of fig. 12 (1:1 scale)



APPLICATION INFORMATION (continued)

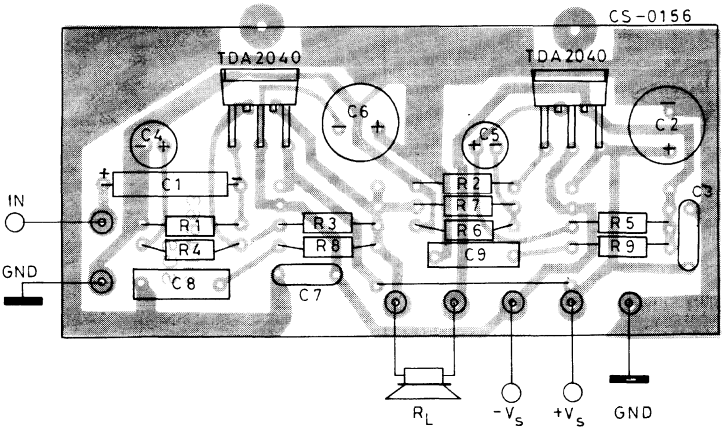
Fig. 14 - 30W Bridge amplifier with split power supply



$V_s = \pm 16V$
$R_L = 8\Omega$
$P_o \geqslant 30W$ (d = 0.5%)

S-5138/3

Fig. 15 - P.C. board and components layout for the circuit of fig. 14 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 16 - Two way Hi-Fi system with active crossover

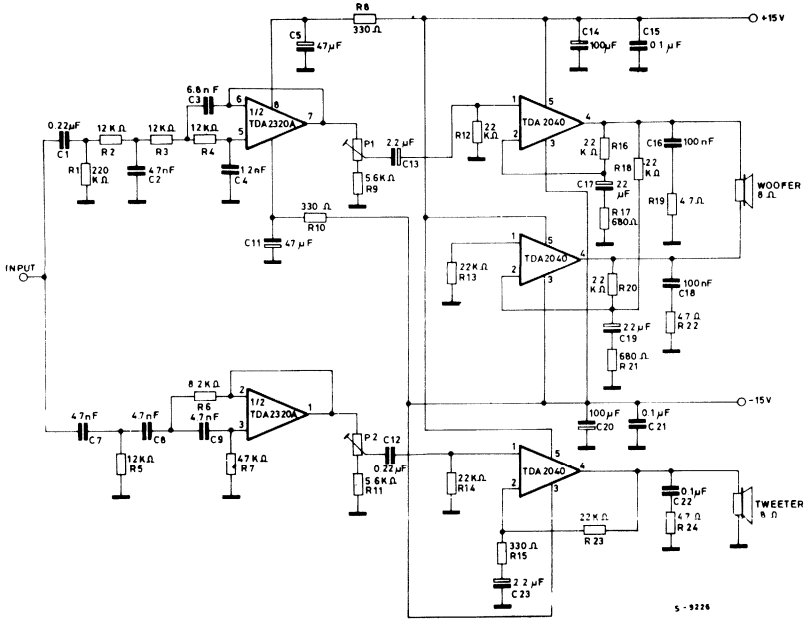
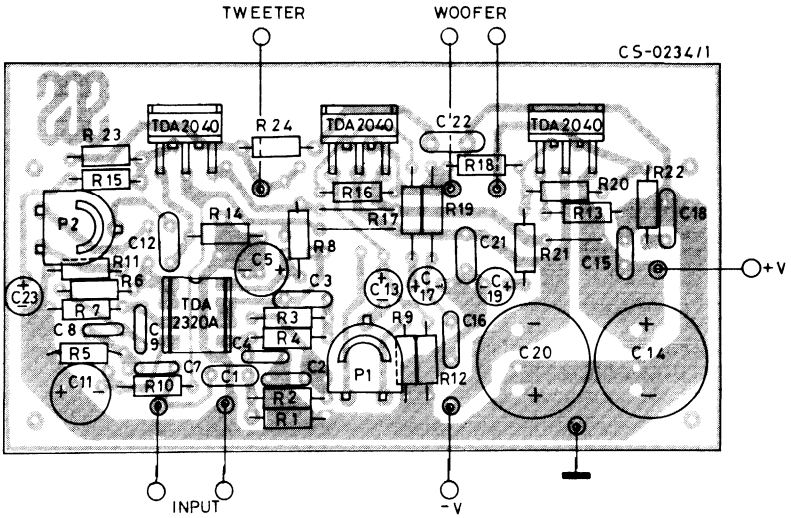


Fig. 17 - P.C. board and component layout of the circuit of fig. 16 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 18 - Frequency response

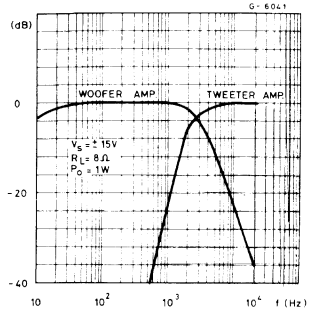
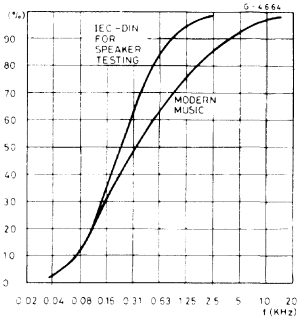


Fig. 19 - Power distribution vs. frequency



Multiway speaker systems and active boxes

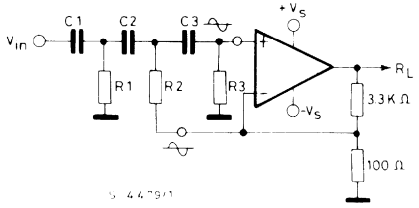
Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two, three or four bands.

To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum determine the cutoff frequencies of the crossover filters (see Fig. 19). As an example, a 100W three-way system with crossover frequencies of 400Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.

Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance

Fig. 20 - Active power filter



Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers. In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6dB/octave) can be recommended.

The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.

The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.

A more effective solution, named "Active Power Filter" by SGS is shown in Fig. 20.

The proposed circuit can realize combined power amplifiers and 12dB/octave or 18dB/octave high-pass or low-pass filters.

APPLICATION INFORMATION (continued)

In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (-) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for $f_c = 900Hz$ using a Bessel 3rd order Sallen and Key structure are:

C1 = C2 = C3	R1	R2	R3
22nF	8.2KΩ	5.6KΩ	33KΩ

In the block diagram of Fig. 21 is represented an active loudspeaker system completely realized using power integrated circuit, rather than the traditional discrete transistors on hybrids, very high quality is obtained by driving the audio spectrum into three bands using active crossovers (TDA2320A) and a separate amplifier and loudspeakers for each band.
A modern subwoofer/midrange/tweeter solution is used.

SHORT CIRCUIT PROTECTION

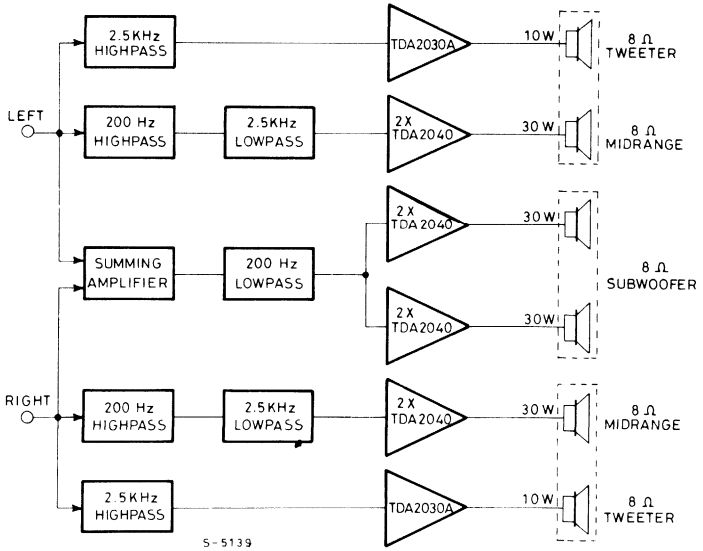
The TDA2040 has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. The TDA2030A is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time the thermal shut down protection keeps the junction temperature within safe limits.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

Fig. 21 - High power active loudspeaker system using TDA2030A and TDA2040



PRACTICAL CONSIDERATION

Printed circuit board

The layout shown in Fig. 11 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the gorund return of the output in which a high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application suggestions

The recommended values of the components are those shown on application circuit of Fig. 10. Different values can be used. The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22KΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R2	680Ω	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	22KΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R4	4.7Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
C1	1μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0.1μF	Supply voltage bypass		Danger of oscillation
C5, C6	220μF	Supply voltage bypass		Danger of oscillation
C7	0.1μF	Frequency stability		Danger of oscillation

(*) The value of closed loop gain must be higher than 24dB.

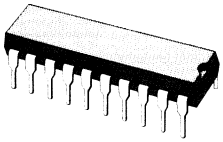
TDA2220

NOT FOR NEW DESIGN

AM/FM RADIO

- VERY WIDE RANGE OF SUPPLY VOLTAGE 3 to 16V
- HIGH RECOVERED AUDIO SIGNAL (100 mV, $\Delta f = \pm 22.5$ KHz or m = 0.3)
- DESIGNED FOR USE WITH EXTERNAL RATIO DETECTOR OR INTERNAL QUADRATURE DETECTOR
- VERY GOOD AM SIGNAL HANDLING (1V; m = 0.8)
- VERY SIMPLE DC SWITCHING OF AM-FM SECTIONS
- SUITABLE FOR CAPACITANCE, VARICAP AND INDUCTIVE TUNING
- VERY LOW TWEET
- COMMON (AM-FM) FIELD STRENGTH METER OUTPUT PIN

The TDA 2220 is a high performance AM/FM radio IC designed for use in a wide range of car radio, portable radio and home radio applications, operating on a supply voltage from 3 to 16V. A special feature of this device is that it may be used with an internal quadrature detector or an external ratio detector. The TDA 2220 is supplied in a 20 pin plastic DIP package.



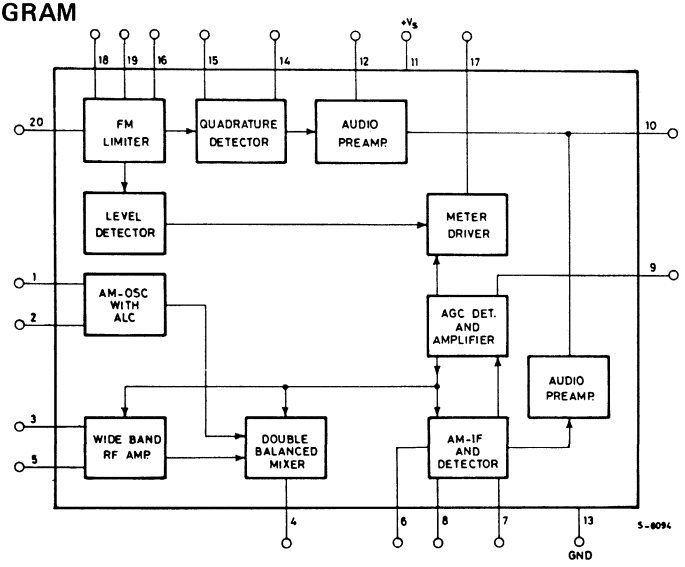
DIP-20 Plastic (0.4)

ORDERING NUMBER: TDA 2220

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{op}	Operating temperature	-40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

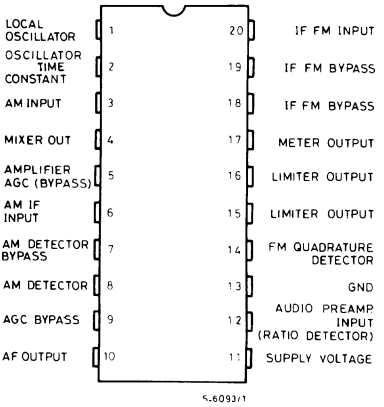
BLOCK DIAGRAM



TDA2220

CONNECTION DIAGRAM

(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max 100 °C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb}= 25°C, V_s = 9V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		3	9	16	V
I_d	Current drain	AM Section	10	16	21	mA
		FM Section	10	14	21	

AM SECTION (f_o = 1MHz; f_m = 1KHz)

V_i	Input sensitivity	S/N = 26 dB m = 0.3		12	25	μV
$\frac{S+N}{N}$	Signal to noise ratio	V_i = 10mV m = 0.3	45			dB
V_i	AGC range	ΔV_{out} = 10dB m = 0.8	100			dB
V_o	Recovered audio signal (pin 10)	V_i = 1 mV m = 0.3	75	120	170	mV
d	Distortion			0.5		%
d	Distortion	V_i = 1 mV m = 0.8		2	3	%
V_H	Max input signal handling capability	m = 0.8 d < 10%	1			V
R_i	Input resistance between pins 3 and 5	m = 0		7.5		KΩ
C_i	Input capacitance between pins 3 and 5	m = 0		18		pF
R_o	Output resistance (pin 10)		4.5	7	9.5	KΩ
	Tweet 2 IF	m = 0.3 V_i = 1mV		38		dB
	Tweet 3 IF			55		dB
V_m(*)	Meter output	V_i = 1 mV m = 0.3		130		mV

(*) Meter resistance = 1.3 KΩ.

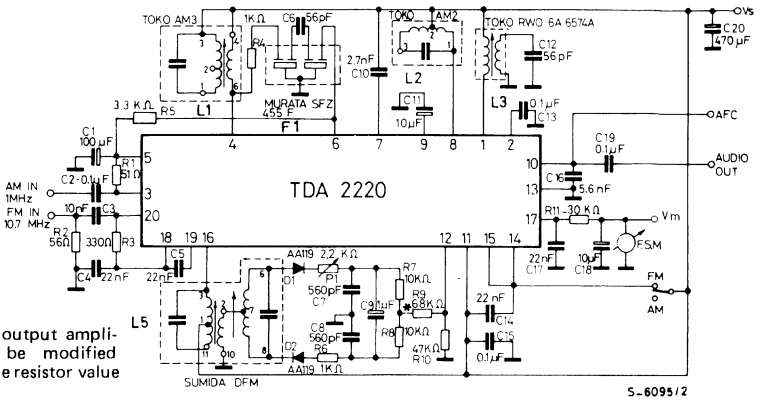
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
FM SECTION (f_o = 10.7MHz; f_m = 1KHz)						**(RATIO DETECTOR)**
V_i	Input limiting voltage	-3 dB limiting point		25	36	μV
AMR	Amplitude modulation rejection	$\Delta f = \pm 22.5$KHz m = 0.3 V_i = 3mV	50	60		dB
$\frac{S+N}{N}$	Signal to noise ratio	$\Delta f = \pm 22.5$KHz V_i = 10mV	55	65		dB
d	Distortion	$\Delta f = \pm 75$KHz V_i = 1mV		0.4	0.7	%
d	Distortion	$\Delta f = \pm 22.5$ KHz V_i = 1mV		0.2		%
V_o	Recovered audio signal (pin 10)	$\Delta f = \pm 22.5$KHz V_i = 1mV	75	120	170	mV
R_i	Input resistance between pin 20 and ground	Δf = 0		6.5		KΩ
C_i	Input capacitance between pin 20 and ground	Δf = 0		14		pF
R_o	Output resistance (pin 10)		4.5	7	9.5	KΩ
V_m(*)	Meter output	V_i = 1 mV Δf = + 22.5 KHz		110		mV

FM SECTION (f_o = 10.7MHz, f_m = 1KHz)						**(QUADRATURE DETECTOR)**
V_i	Input limiting voltage	-3dB limiting point		25	36	μV
AMR	Amplitude modulation rejection	$\Delta f = \pm 22.5$KHz m = 0.3 V_i = 3mV	35	44		dB
$\frac{S+N}{N}$	Signal to noise ratio	$\Delta f = \pm 22.5$KHz V_i = 10mV	55	65		dB
d	Distortion	$\Delta f = \pm 75$KHz V_i = 1mV		0.7	1.5	%
d	Distortion	$\Delta f = \pm 22.5$KHz V_i = 1mV		0.25		%
d	Distortion (double tuned)			0.1		%
V_o	Recovered audio signal (pin 10)	$\Delta f = \pm 22.5$KHz V_i = 1mV	60	90	130	mV
R_i	Input resistance between pin 20 and ground	Δf = 0		6.5		KΩ
C_i	Input capacitance between pin 20 and ground	Δf = 0		14		pF
R_o	Output resistance (pin 10)		4.5	7	9.5	KΩ
V_m(*)	Meter output	V_i = 1 mV Δf = ± 22.5 KHz		110		mV

(*) Meter resistance = 1.3 KΩ.

Fig. 1 - Test circuit with FM ratio detector



(*) The audio output amplitude can be modified changing the resistor value

Fig. 2 - P.C. board and component layout of the circuit of fig. 1 (1:1 scale)

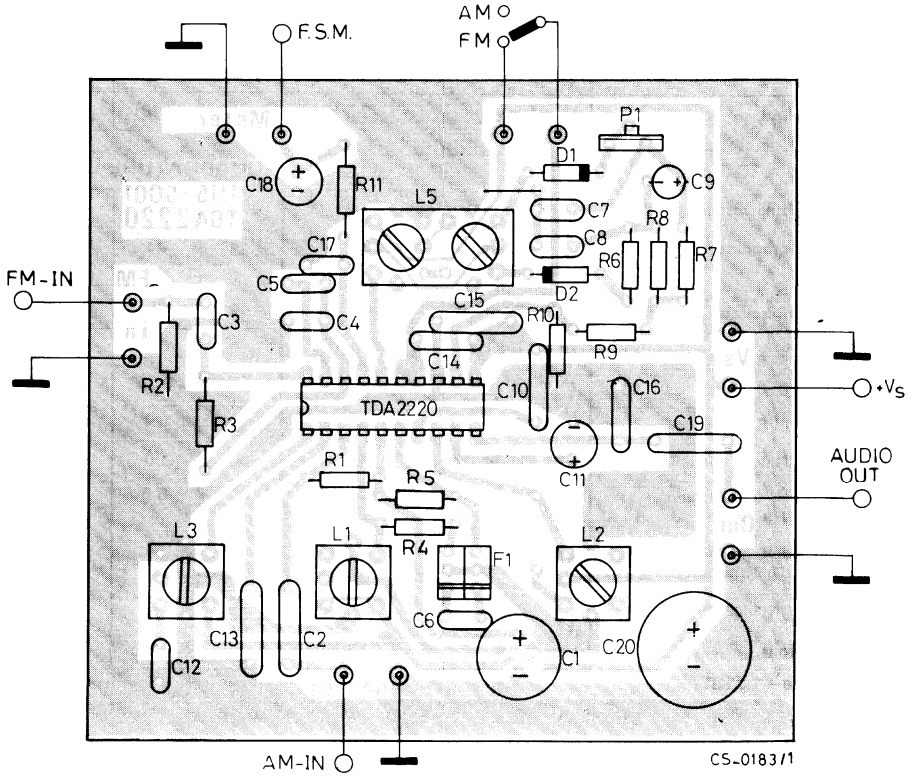


Fig. 3 - Test circuit with FM quadrature detector

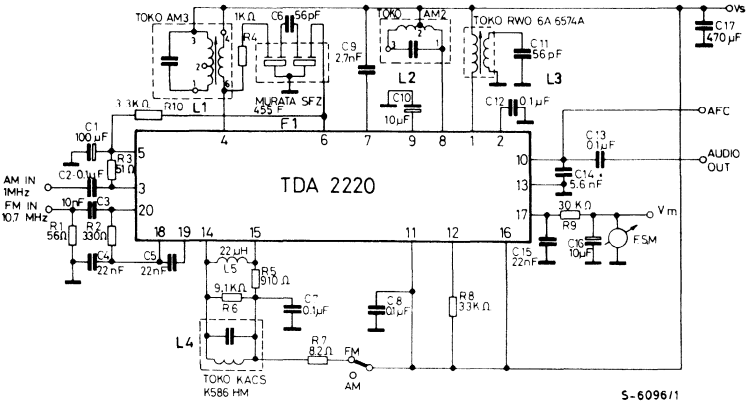
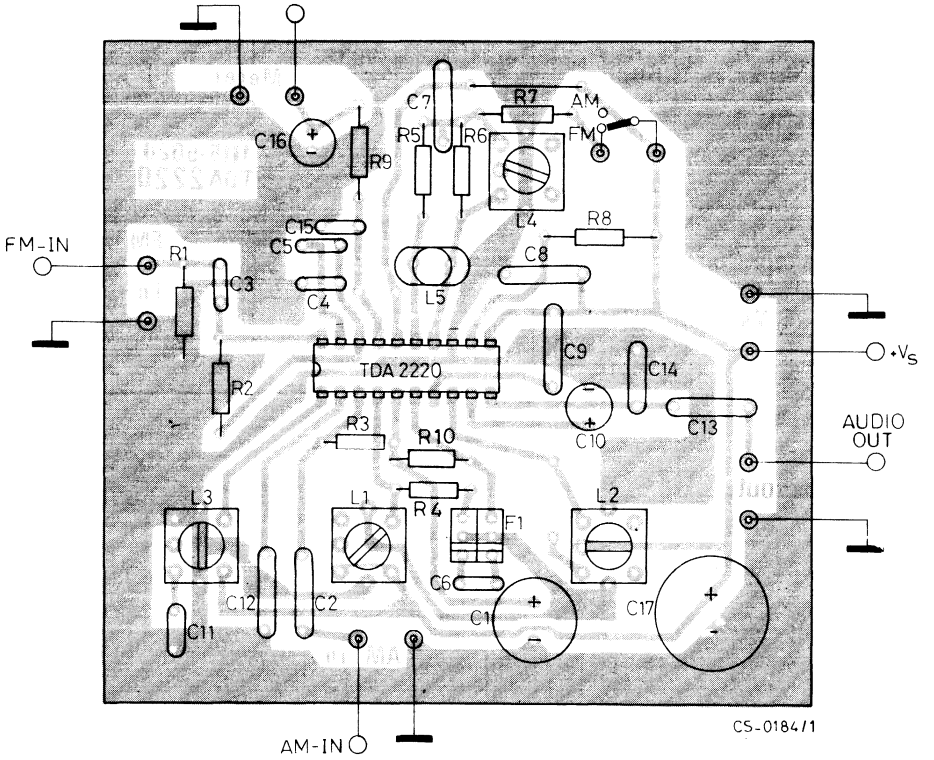
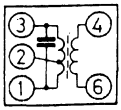


Fig. 4 - P.C. board and component layout of the circuit of fig. 3 (1:1 scale)



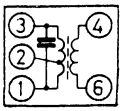
L1 - 455 kHz IF Coil



C_o(pF)	f (MHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	57	116	24

TOKO AM3 - 10x10 mm
RLC - 4A7525N

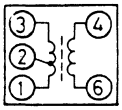
L2 - AM Detector Coil



C_o(pF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	173	94	9

TOKO AM2 - 10x10 mm.
RLC - 4A7524EK

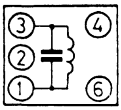
L3 - AM Oscillator Coil



f (kHz)	L (μH)	Q_o	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	220	80	2	75	8

TOKO - 10x10 mm.
RWO - 6A6574N

L4 - FM Detector Coil

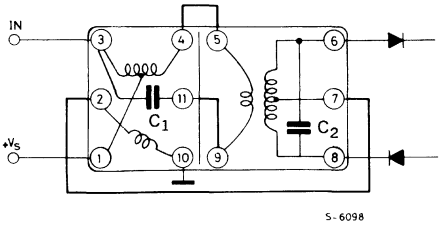


S-6097

C_o(pF)	f (MHz)	Q_o	TURNS		
1-3		1-3	1-3	–	–
82	10.7	100	12	–	–

TOKO - 10x10 mm
KACS - K586 HM

L5 - Ratio Detector



S-6098

C_1(pF)	C_2(pF)	f (MHz)	Q_o
3-11	6-8		3-11/4-8
27	47	10.7	70

TURNS					
1-3	1-4	2-10	5-9	6-7	7-8
11	6½	5½	½	7	7

SUMIDA
DFM

APPLICATION INFORMATION

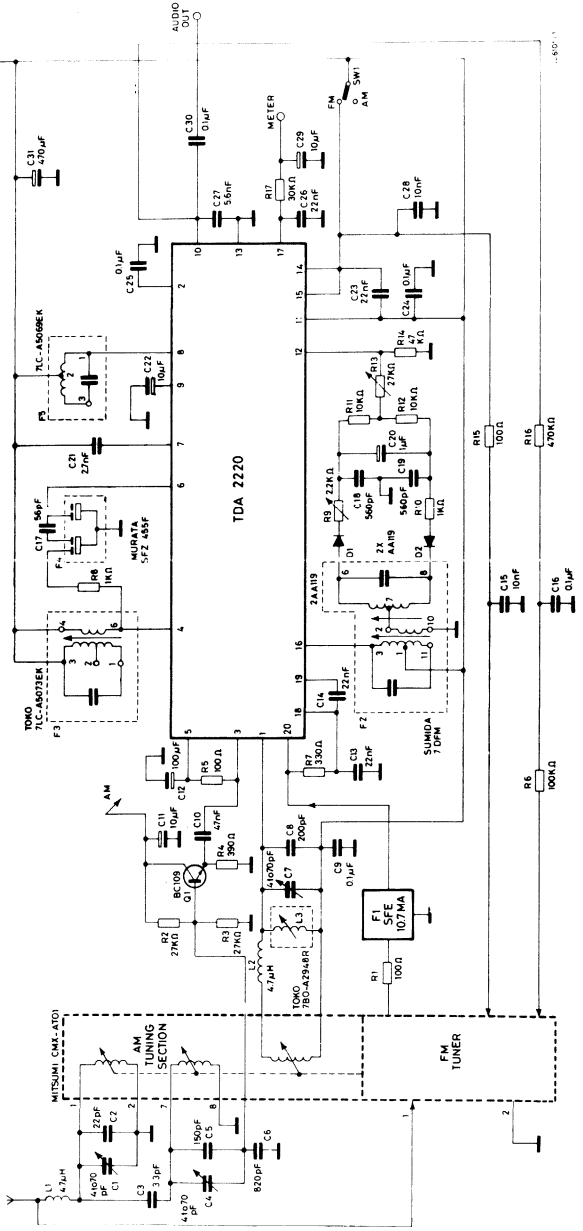
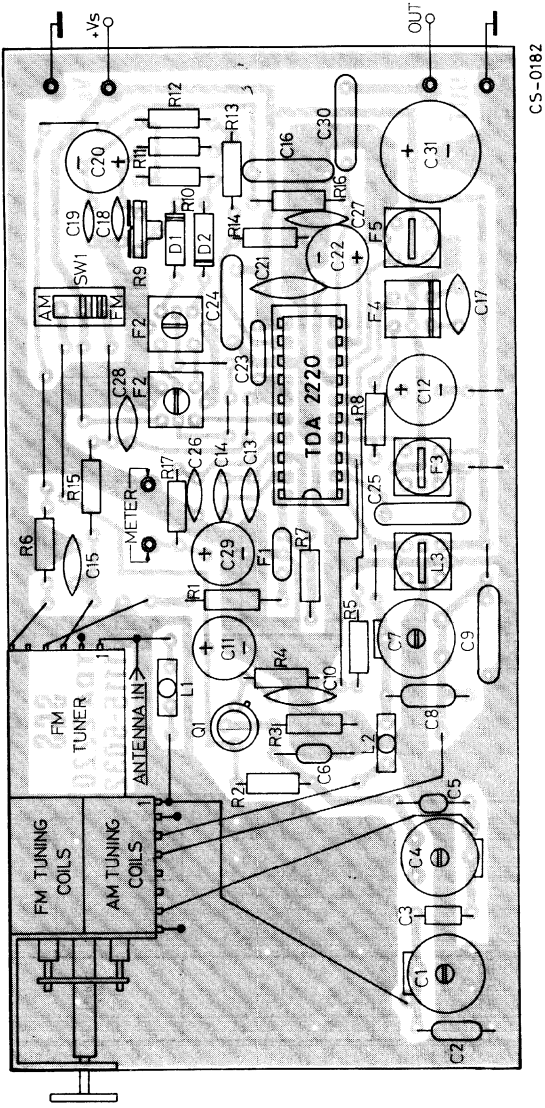


Fig. 5 - AM/FM car radio receiver

Note - The transistor Q1 can be eliminated using the tuner of fig. 7.

Fig. 6 - P.C. board and component layout of the circuit of fig. 5 (1:1 scale)

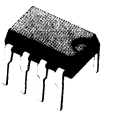


TDA2320

PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

The TDA2320 is a monolithic integrated circuit in Minidip package specially designed to amplify the IR signal in remot controlled TV or radio sets. It directly interfaces with the digital control circuitry.
The TDA 2320 incorporates a two stages amplifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and flash or carrier transmission modes as provided for example by the M709/M710C/ MOS transmitter.

The TDA2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.



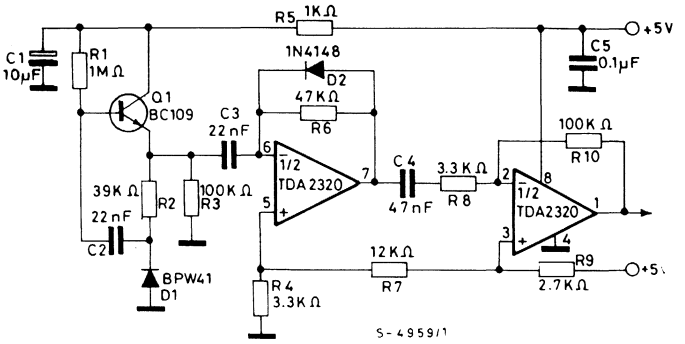
Minidip Plastic

ORDERING NUMBER: TDA2320

ABSOLUTE MAXIMUM RATINGS

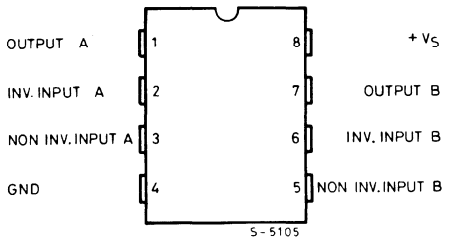
V_s	Supply voltage	20	V
$T_{stg,\ j}$	Storage and Junction temperature	-40 to 150	°C
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW

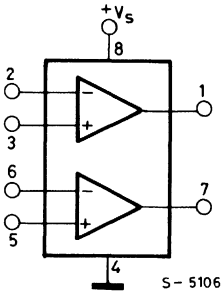
APPLICATION CIRCUIT (Flash mode preamplifier)



CONNECTION AND BLOCK DIAGRAM

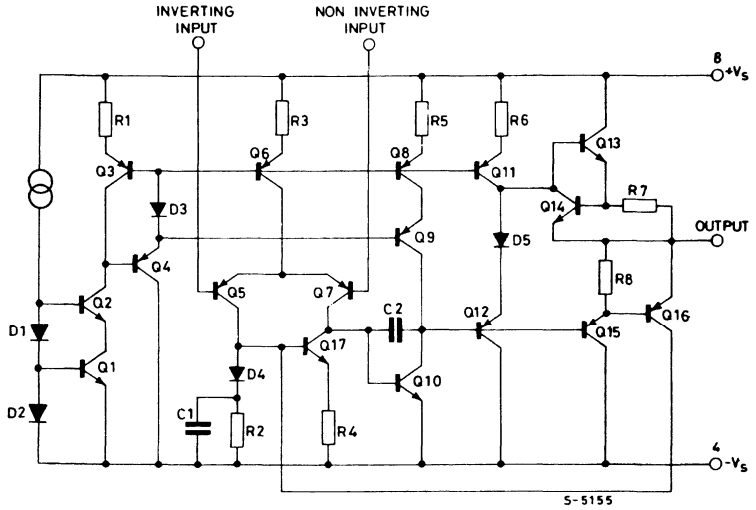
(top view)





SCHEMATIC DIAGRAM

(one section)



THERMAL DATA

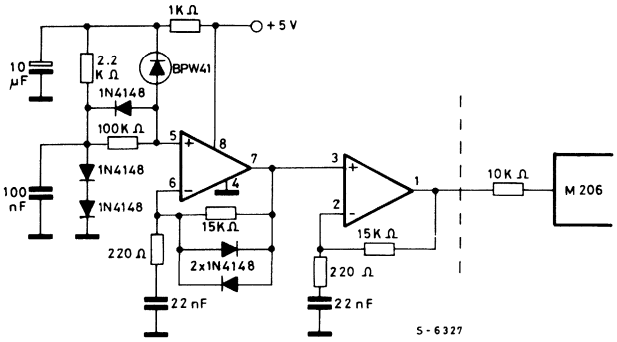
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 5V, T_{amb}= 25°C, single amplifier, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_s	Total supply current	V_s = 20V		0.8	2	mA
I_b	Input bias current			100	500	nA
V_{os}	Input offset voltage	R_g < 10 KΩ		0.5		mV
I_{os}	Input offset current			15		nA
G_v	Open loop voltage gain	f = 1 KHz	64	70		dB
		f = 100 KHz		30		dB
B	Gain bandwidth product	f = 40 KHz	1.5	3		MHz
SR	Slew rate	R_L= 2 KΩ		1.5		V/μs
e_N	Total input noise voltage	f = 40 KHz Rg= 10KΩ		20		$nV\sqrt{Hz}$
V_o	DC output voltage swing			2.5		Vpp
SVR	Supply voltage rejection	f = 100 Hz		80		dB

APPLICATION INFORMATION

Fig. 1 - Application circuit for carrier transmission mode



APPLICATION INFORMATION (continued)

Fig. 2 - Flash mode preamplifier

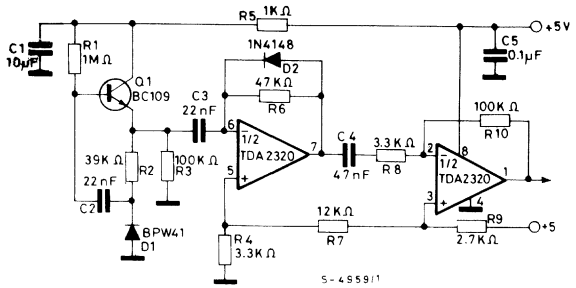


Fig. 3 - P.C. and components layout of the circuit of fig. 2 (1 : 1 scale)

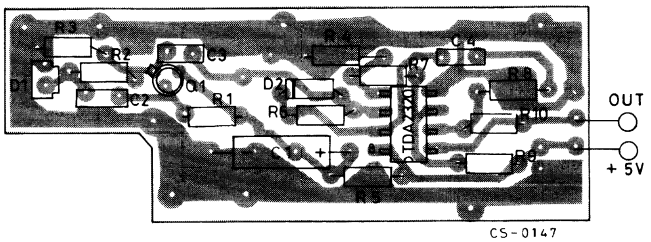


Fig. 4 - IR transmitter using M709 or M710

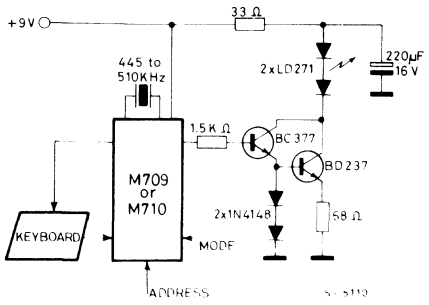
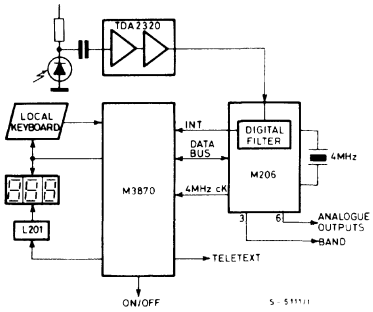
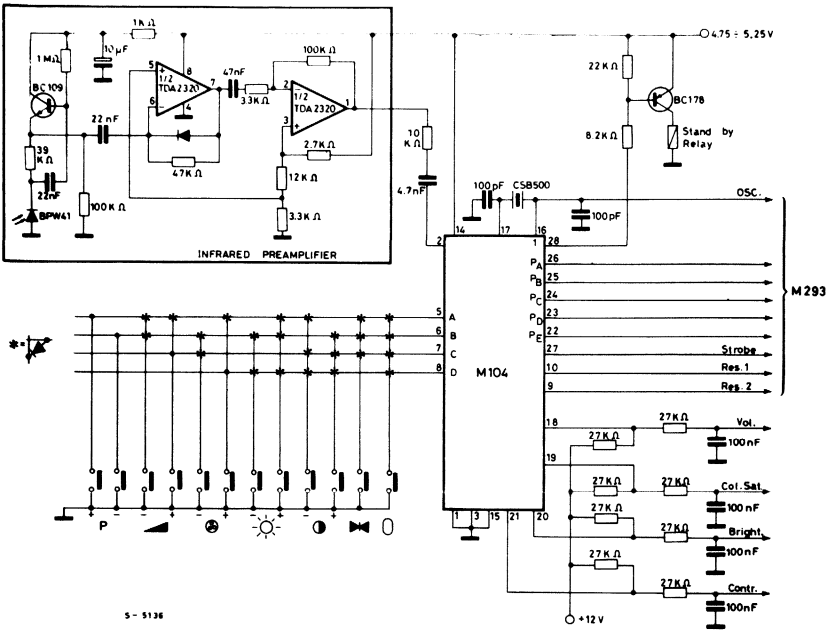


Fig. 5 - MMC II - PLL TV Frequency synthesizer



APPLICATION INFORMATION (continued)

Fig. 6 - IR Preamplifier and Remote Control receiver for 32 channel voltage synthesizer (EPM - M293)



TDA2320A

MINIDIP STEREO PREAMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3 TO 36V)
- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW CURRENT CONSUMPTION (0.8mA)
- VERY LOW DISTORTION
- NO POP-NOISE
- SHORT CIRCUIT PROTECTION

The TDA2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.

The TDA2320A is a monolithic integrated circuit a 8 lead minidip.

Minidip Plastic

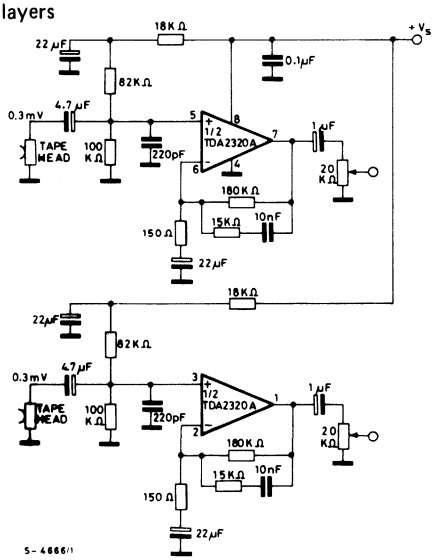
ORDERING NUMBER: TDA 2320A

ABSOLUTE MAXIMUM RATINGS

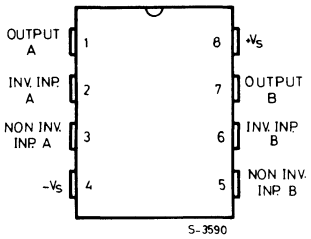
V_s	Supply voltage	36	V
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

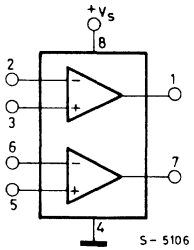
TYPICAL APPLICATION:

Stereo preamplifier for cassette players

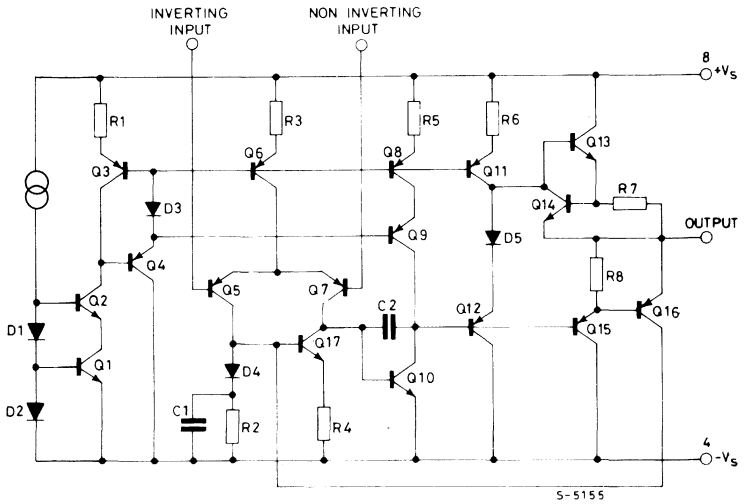


CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM
(one section)



TEST CIRCUITS

Fig. 1

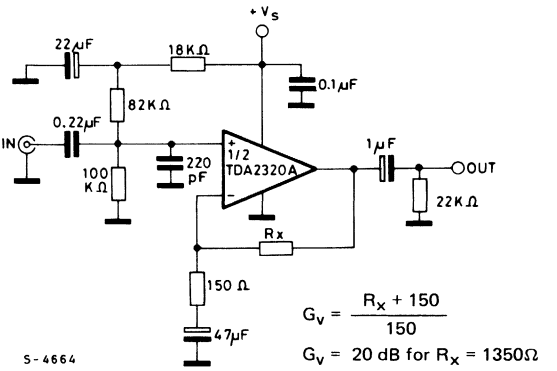
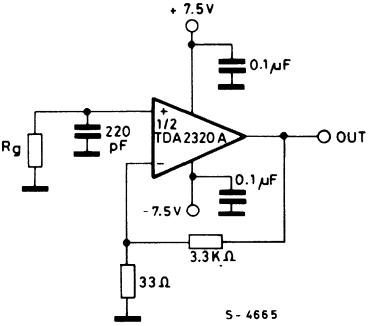


Fig. 2



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage (*)			3		36	V
I_s	Supply current (*)				0.8	2	mA
I_b	Input bias current				150	500	nA
V_{os}	Input offset voltage	R_g < 10 KΩ			1	5	mV
I_{os}	Input offset current				10	50	nA
G_v	Open loop voltage gain	V_s = 15V	f = 333 Hz		80		dB
			f = 1 KHz		70		
			f = 10 KHz		50		
		V_s = 4.5V	f = 1 KHz		70		
V_o	Output voltage swing (*)	f = 1 KHz	V_s = 15V		13		Vpp
		R_L = 600Ω	V_s = 4.5V		2.5		
B	Gain-bandwidth product	f = 20 KHz		1.5	2.5		MHz
BW	Power bandwidth (*)	V_o = 5 Vpp d = 1%		40	70		KHz
SR	Slew rate (*)			1	1.6		V/μS
d	Distortion (*)	V_o = 2V	f = 1 KHz		0.03		%
		G_v = 20 dB	f = 10 KHz		0.08		
e_N	Total input noise voltage (**)	Curve A	R_g = 50Ω		1		μV
			R_g = 600Ω		1.1	1.4	
			R_g = 5 KΩ		1.5		
		B = 22 Hz to 22 KHz	R_g = 50Ω		1.3		μV
			R_g = 600Ω		1.5		
			R_g = 5 KΩ		2		
		f = 1 KHz	R_g = 600Ω		9		$nV/\sqrt{Hz}$
Cs	Channel separation (**)		f = 1 KHz		100		dB
SVR	Supply voltage (**) rejection		f = 100 Hz		80		dB

(*) Test circuit of fig. 1.
(**) Test circuit of fig. 2.

Fig. 3 - Supply current vs. supply voltage

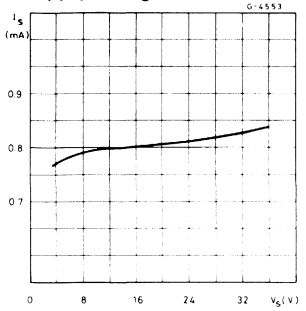


Fig. 4 - Supply current vs. ambient temperature

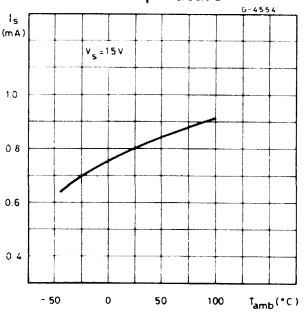


Fig. 5 - Output voltage swing vs. load resistance

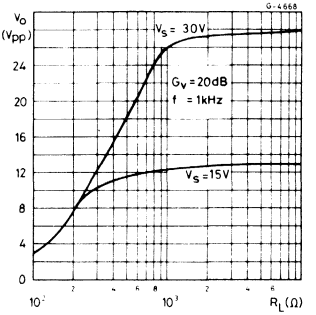


Fig. 6 - Power bandwidth

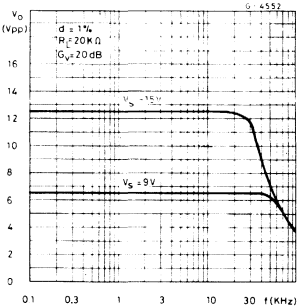


Fig. 7 - Total harmonic distortion vs. output voltage

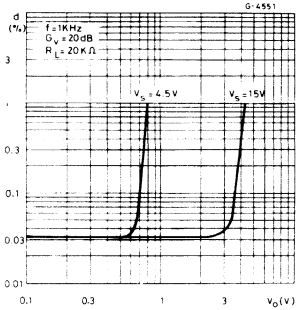


Fig. 8 - Total input noise vs. source resistance

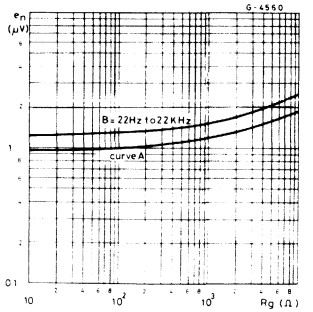


Fig. 9 - Noise density vs. frequency

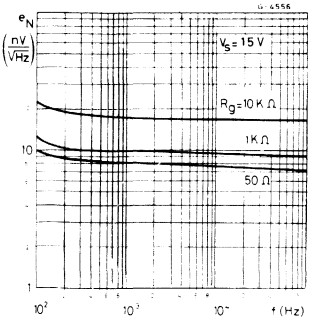


Fig. 10 - RIAA preamplifier response (circuit of fig. 12)

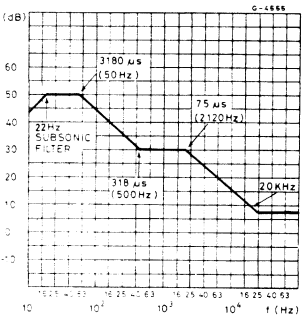
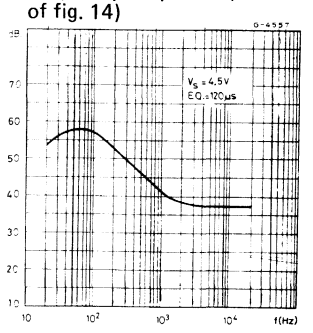


Fig. 11 - Tape preamplifier frequency response (circuit of fig. 14)



APPLICATION INFORMATION

Fig. 12 - Stereo RIAA preamplifier

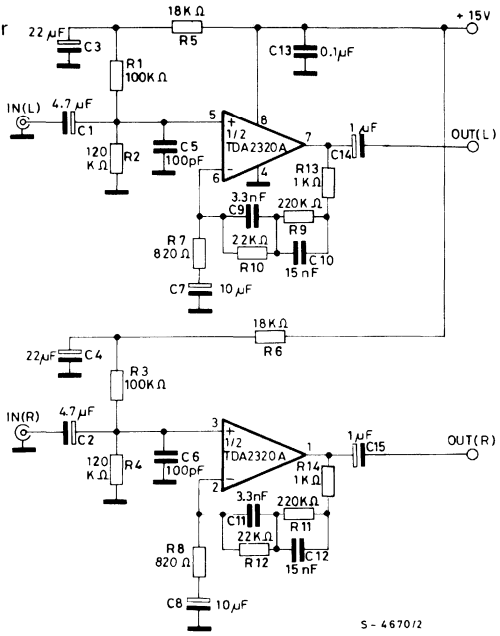
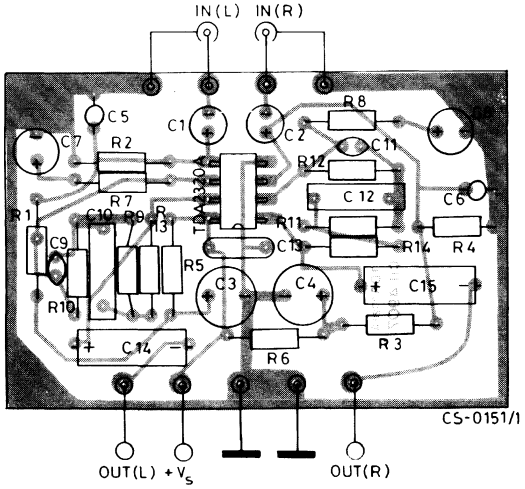


Fig. 13 - P.C. board and components layout of the circuit of fig. 12



APPLICATION INFORMATION (continued)

Fig. 14 - Stereo preamplifier for Walkman cassette players

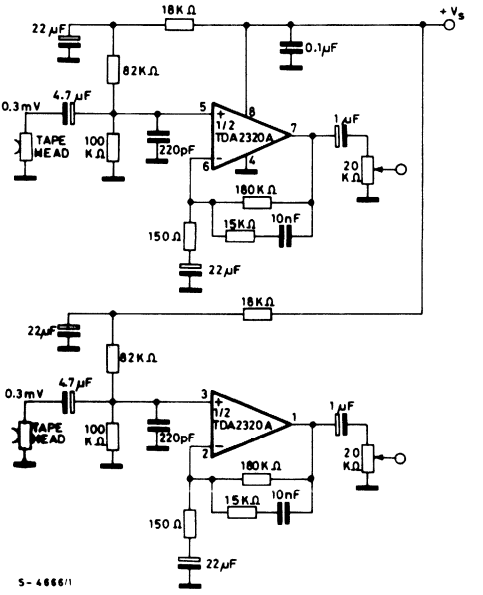


Fig. 15 - Second order 2 KHz Butterworth crossover filter for Hi-Fi active boxes

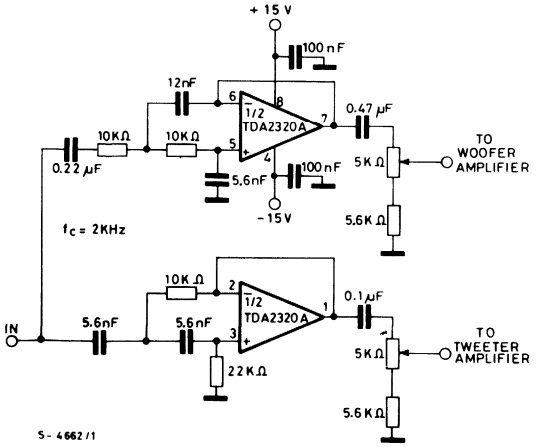
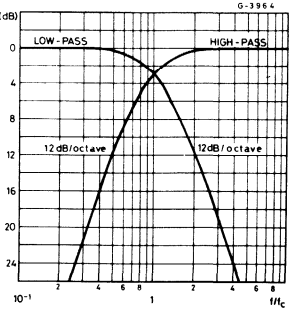


Fig. 16 - Frequency response (circuit of fig. 15)



APPLICATION INFORMATION (continued)

Fig. 17 - Third order 2.8 KHz Bessel crossover filter for Hi-Fi active boxes

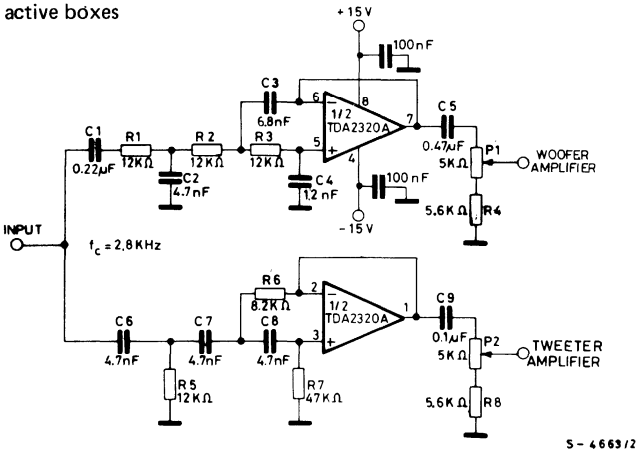


Fig. 18 - Frequency response (circuit of fig. 17)

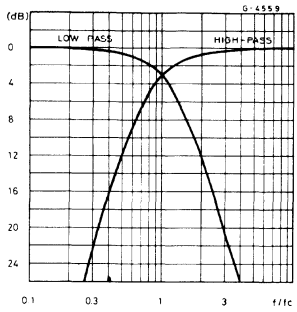


Fig. 19 - 200 Hz to 2 KHz Active Bandpass Filter for midrange speakers

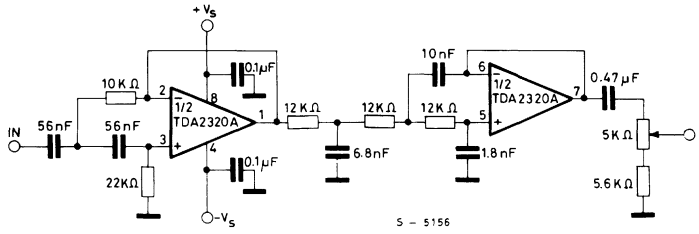
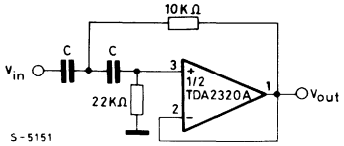
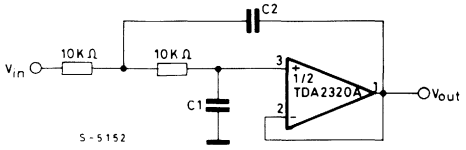


Fig. 20 - Subsonic filter



f_c (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

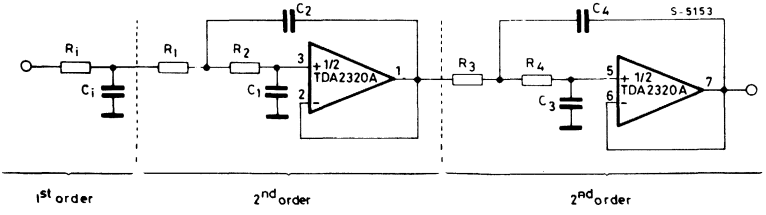
Fig. 21 - High-cut filter



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 22 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33$ nF

$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97$ nF

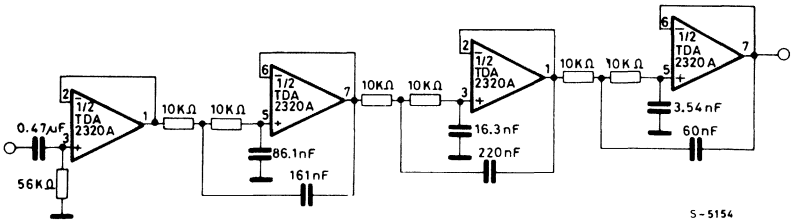
$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20$ nF

$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45$ nF

$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14$ nF

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 23 - Sixth-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

APPLICATION INFORMATION (continued)

Fig. 24 - Three band tone control

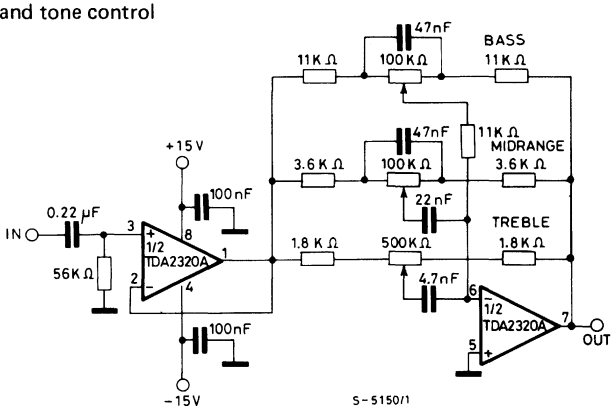
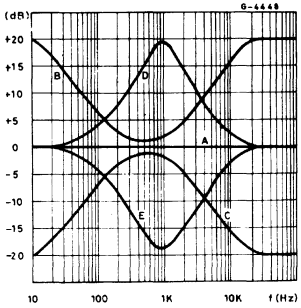


Fig. 25 - Frequency response of the circuit of fig. 24.



A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat

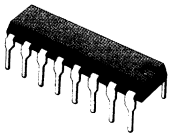
TDA2822

PRELIMINARY DATA

DUAL POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 3V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2822 is a monolithic integrated circuit in 12+2+2 powerdip, intended for use as dual audio power amplifier in portable radios and TV sets.



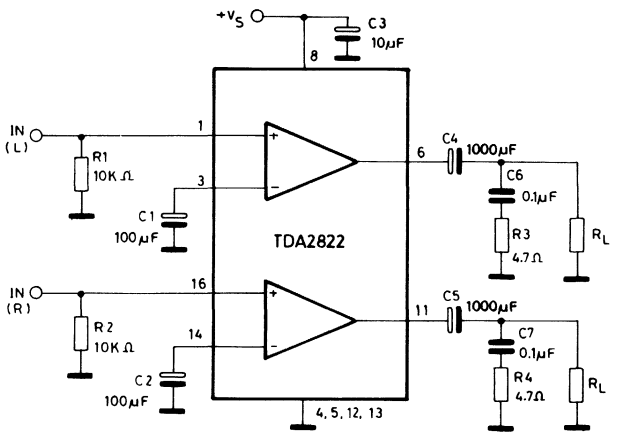
Powerdip (12+2+2)

ORDERING NUMBER: TDA2822

ABSOLUTE MAXIMUM RATINGS

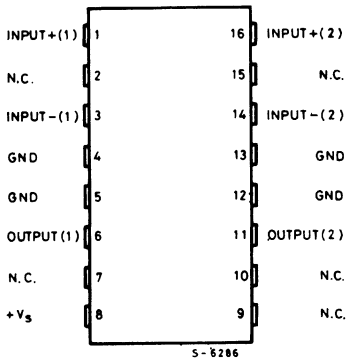
V_s	Supply voltage	15	V
I_o	Output peak current	1.5	A
P_{tot}	Total power dissipation at T_{amb} = 50°C	1.25	W
	at T_{case} = 70°C	4	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TYPICAL APPLICATION CIRCUIT (STEREO)

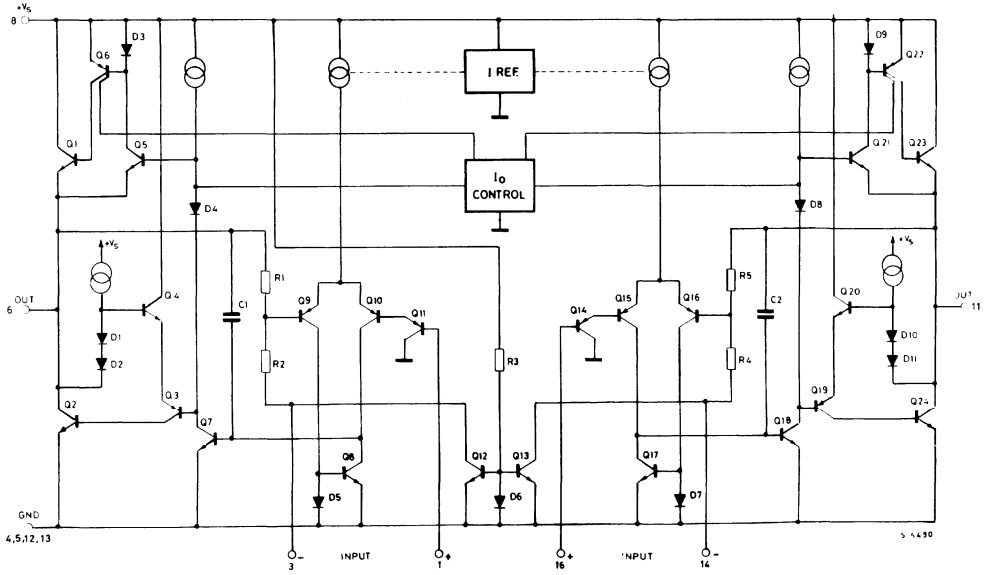


CONNECTION DIAGRAM

(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max 80 °C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max 20 °C/W

ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
STEREO (Test circuit of Fig. 1)						
V_s	Supply voltage		3		15	V
V_c	Quiescent output voltage	V_s = 9V V_s = 6V		4 2.7		V V
I_d	Quiescent drain current			6	12	mA
I_b	Input bias current			100		nA
P_o	Output current (each channel)	d = 10% f = 1KHz V_s = 9V R_L = 4Ω V_s = 6V R_L = 4Ω V_s = 4.5V R_L = 4Ω	 1.3 0.45	 1.7 0.65 0.32		 W W W
G_v	Closed loop voltage gain	f = 1KHz	36	39	41	dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_s = 10KΩ B = 22Hz to 22KHz		2.5		μV
		R_s = 10KΩ Curve A		2		μV
SVR	Supply voltage rejection	f = 100Hz	24	30		dB
CS	Channel separation	R_g = 10KΩ f = 1KHz		50		dB
BRIDGE (Test circuit of Fig. 2)						
V_s	Supply voltage		3		15	V
I_d	Quiescent drain current	R_L = ∞		6	12	mA
V_{os}	Output offset voltage	R_L = 8Ω		10	60	mV
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 8Ω V_s = 6V R_L = 8Ω V_s = 4.5V R_L = 4Ω	 2.7 0.9	 3.2 1.35 1		 W W W
d	Distortion (f = 1KHz)	R_L = 8Ω P_o = 0.5W		0.2		%
G_v	Closed loop voltage gain	f = 1KHz		39		dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_s = 10KΩ B = 22Hz to 22KHz		3		μV
		R_s = 10KΩ curve A		2.5		μV
SVR	Supply voltage rejection	f = 100Hz		40		dB

Fig. 1 - Test circuit (STEREO)

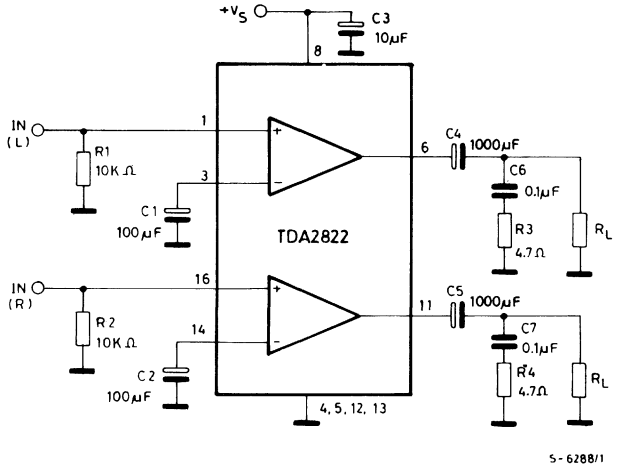


Fig. 2 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)

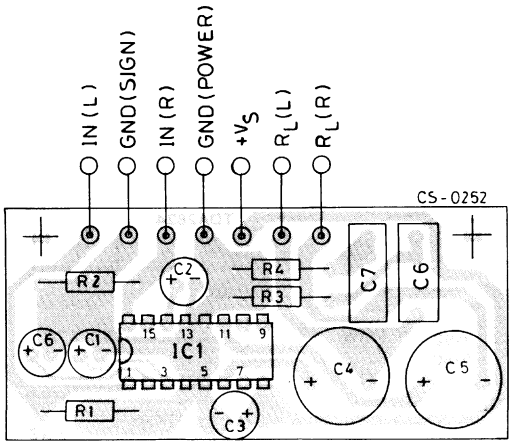


Fig. 3 - Test circuit (BRIDGE)

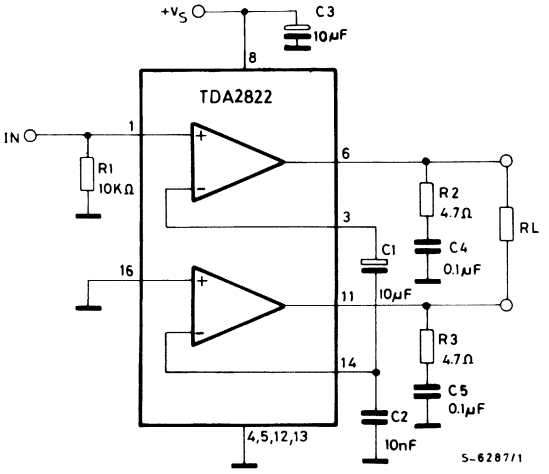


Fig. 4 - P.C. board and components layout of the circuit of Fig. 3 (1 : 1 scale)

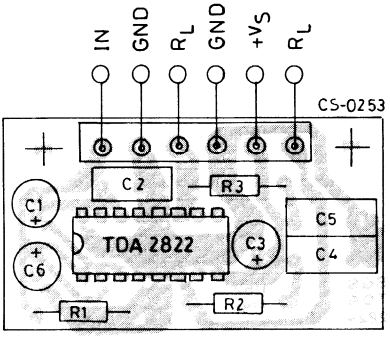


Fig. 5 - Output power vs. supply voltage (Stereo)

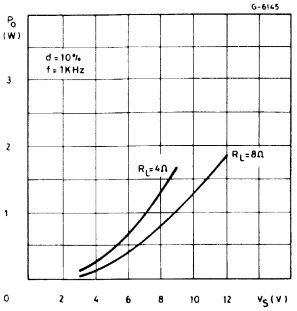


Fig. 6 - Output power vs. supply voltage (Bridge)

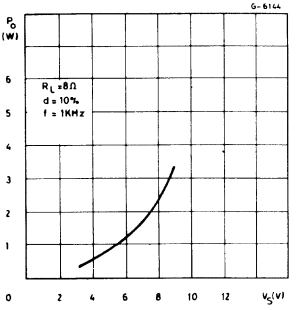


Fig. 7 - Distortion vs. output power (Bridge)

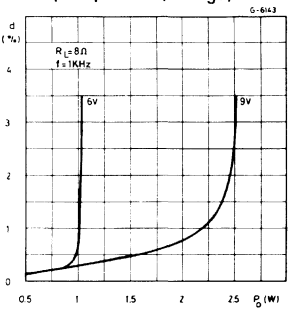


Fig. 8 - Distortion vs. output power (Bridge)

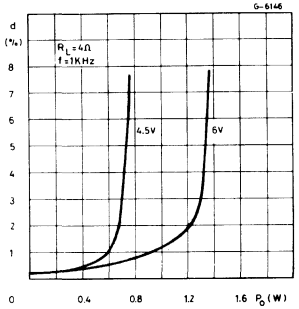


Fig. 9 - Supply voltage rejection vs. frequency

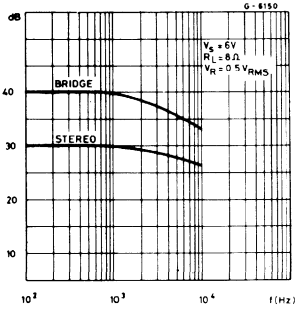


Fig. 10 - Quiescent current vs. supply voltage

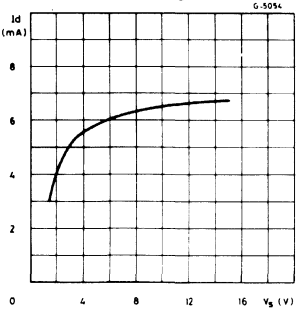


Fig. 11 - Total power dissipation vs. output power (Stereo)

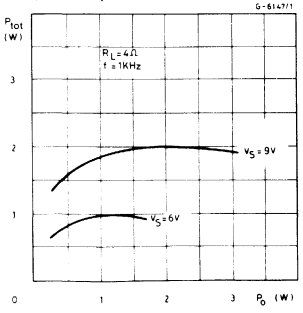


Fig. 12 - Total power dissipation vs. output power (Bridge)

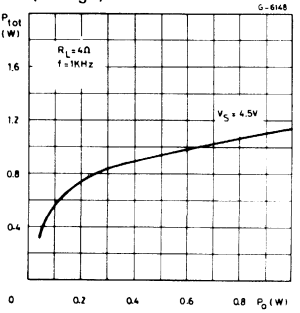


Fig. 13 - Total power dissipation vs. output power (Bridge)

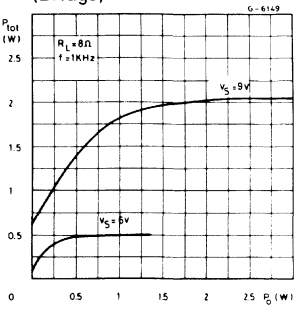
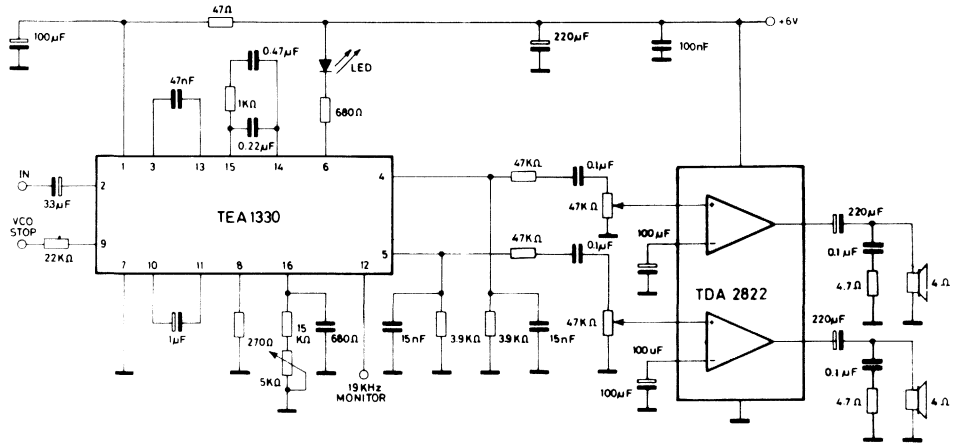


Fig. 14 - Application circuit for portable radios



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA2822 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 15 or to an external heatsink (Fig. 16).

The diagram of figure 17 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35µ (1.4mils).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 15 - Example of P.C. board copper area which is used as heatsink.

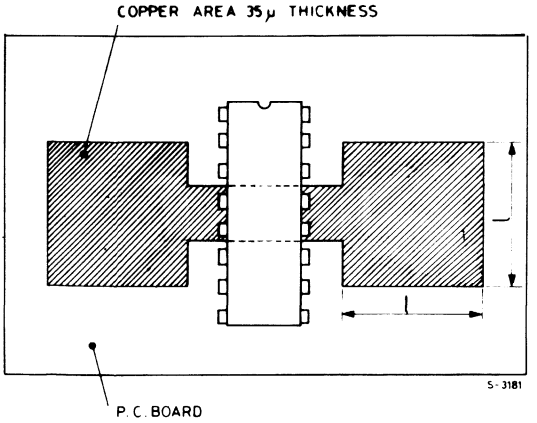
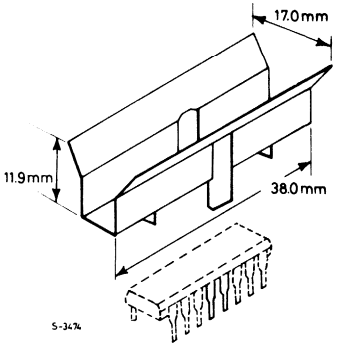


Fig. 16 - External heatsink mounting example



MOUNTING INSTRUCTION (continued)

Fig. 6 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

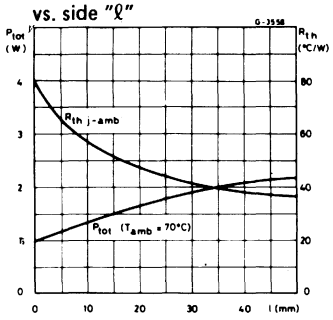
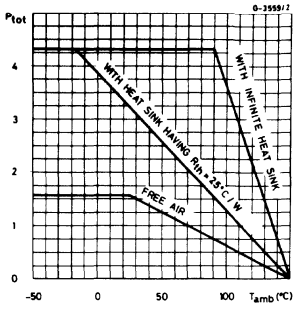


Fig. 7 - Maximum allowable power dissipation vs. ambient temperature



TDA2822M

PRELIMINARY DATA

DUAL LOW-VOLTAGE POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 1.8V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2822M is a monolithic integrated circuit in 8 lead Minidip package. It is intended for use as dual audio power amplifier in portable cassette players and radios.

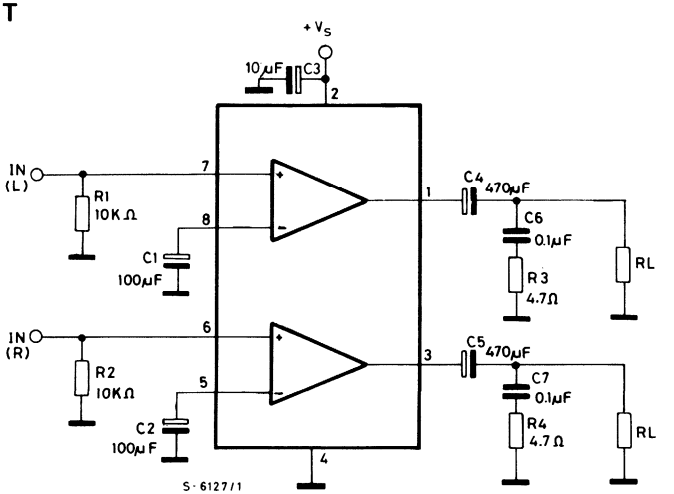
Minidip Plastic

ORDERING NUMBER: TDA2822M

ABSOLUTE MAXIMUM RATINGS

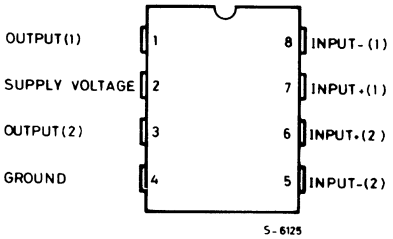
V_s	Supply voltage	15	V
I_o	Peak output current	1	A
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1	W
	at $T_{case} = 50°C$	1.4	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST CIRCUIT

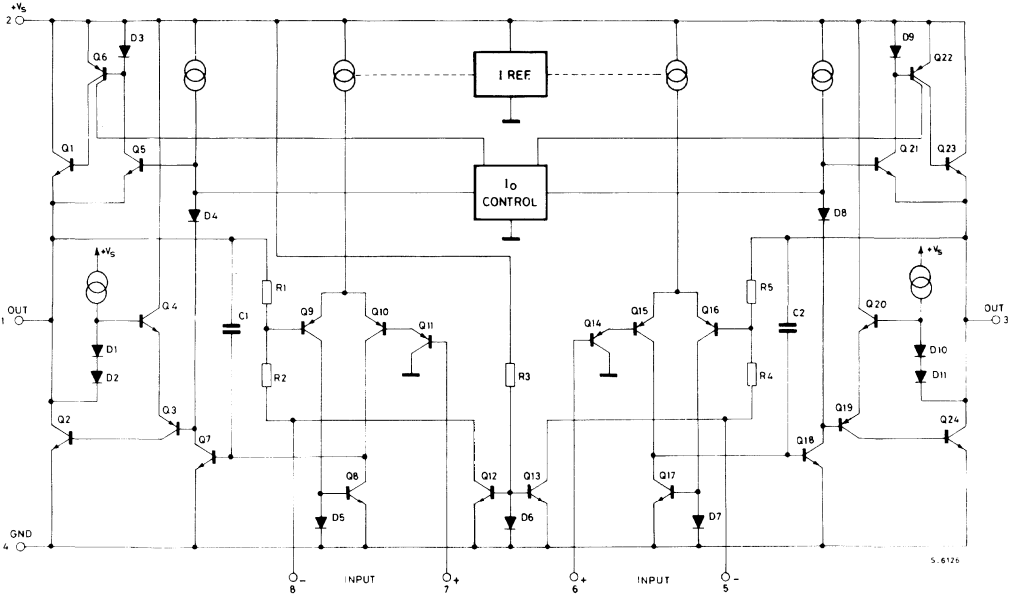


CONNECTION DIAGRAM

(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-pin (4)	max	70	°C/W

STEREO APPLICATION

Fig. 1 - Test circuit

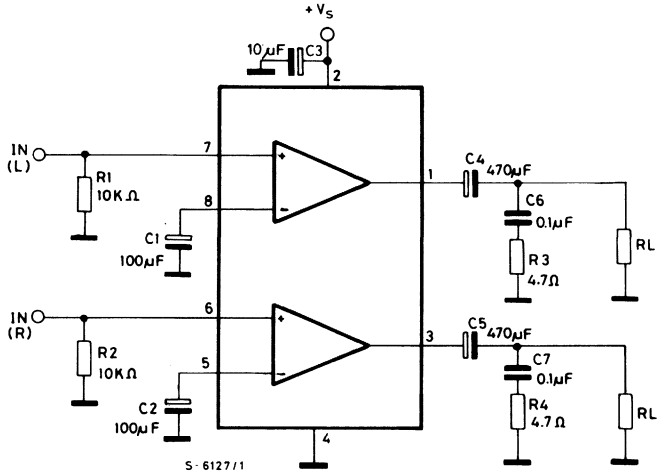
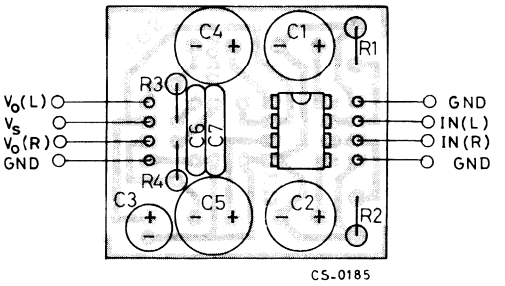


Fig. 2 - P.C. board and component layout of the circuit of Fig. 1 (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
STEREO (Test circuit of Fig. 1)							
V_s	Supply voltage			1.8		15	V
V_o	Quiescent output voltage				2.7		V
		V_s = 3V			1.2		V
I_d	Quiescent drain current				6	9	mA
I_b	Input bias current				100		nA
P_o	Output power (each channel) (f = 1KHz, d = 10%)	R_L = 32Ω	V_s = 9V V_s = 6V V_s = 4.5V V_s = 3V V_s = 2V	90 15	300 120 60 20 5		mW
		R_L = 16Ω	V_s = 6V	170	220		mW
		R_L = 8Ω	V_s = 9V V_s = 6V	 300	1000 380		mW
		R_L = 4Ω	V_s = 6V V_s = 4.5V V_s = 3V	450	650 320 110		mW
d	Distortion (f = 1KHz)	R_L = 32Ω	P_o = 40mW		0.2		%
		R_L = 16Ω	P_o = 75mW		0.2		%
		R_L = 8Ω	P_o = 150mW		0.2		%
G_v	Closed loop voltage gain	f = 1KHz		36	39	41	dB
ΔG_v	Channel balance					± 1	dB
R_i	Input resistance	f = 1KHz		100			KΩ
e_N	Total input noise	R_s = 10KΩ	B = Curve A		2		μV
			B = 22Hz to KHz		2.5		
SVR	Supply voltage rejection	f = 100Hz	C1 = C2 = 100μF	24	30		dB
C_s	Channel separation	f = 1KHz			50		dB

BRIDGE APPLICATION

Fig. 3 - Test circuit

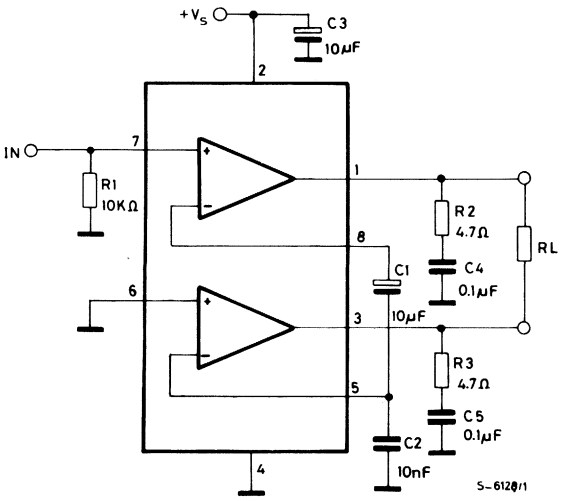
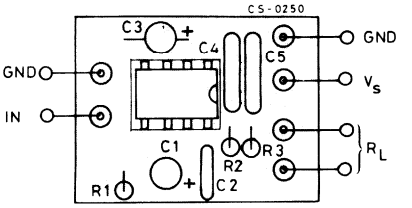


Fig. 4 - P.C. board and components layout of the circuit of Fig. 3 (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
BRIDGE (Test circuit of Fig. 3)							
V_s	Supply voltage			1.8		15	V
I_d	Quiescent drain current	R_L = ∞			6	9	mA
V_{os}	Output offset voltage (between the outputs)	R_L = 8Ω				± 50	mV
I_b	Input bias current				100		nA
P_o	Output power (f = 1KHz, d = 10%)	R_L = 32Ω	V_s = 9V V_s = 6V V_s = 4.5V V_s = 3V V_s = 2V	320 50	1000 400 200 65 8		mW
		R_L = 16Ω	V_s = 9V V_s = 6V V_s = 3V		2000 120		mW
		R_L = 8Ω	V_s = 6V V_s = 4.5V V_s = 3V	900	1350 700 220		mW
		R_L = 4Ω	V_s = 4.5V V_s = 3V V_s = 2V	200	1000 350 80		mW
d	Distortion	P_o = 0.5W f = 1KHz	R_L = 8Ω		0.2		%
G_v	Closed loop voltage gain	f = 1KHz			39		dB
R_i	Input resistance	f = 1KHz		100			KΩ
e_N	Total input noise	R_s = 10KΩ	B = Curve A		2.5		μV
			B = 22Hz to 22KHz		3		
SVR	Supply voltage rejection	f = 100Hz			40		dB
B	Power bandwidth (-3dB)	R_L = 8Ω	P_o = 1W		120		KHz

Fig. 5 - Quiescent current vs. supply voltage

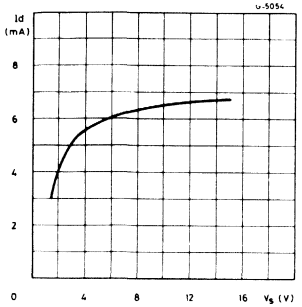


Fig. 6 - Supply voltage rejection vs. frequency

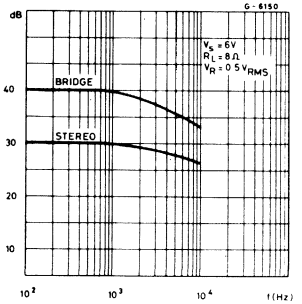


Fig. 7 - Output power vs. supply voltage (THD= 10%, f = 1KHz Stereo)

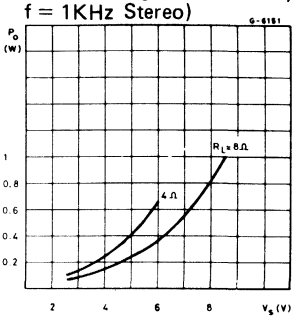


Fig. 8 - Distortion vs. output power (Stereo)

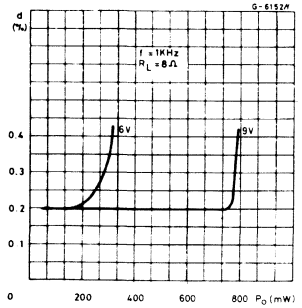


Fig. 9 - Distortion vs. output power (Stereo)

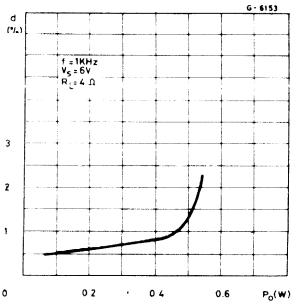


Fig. 10 - Output power vs. supply voltage (Bridge)

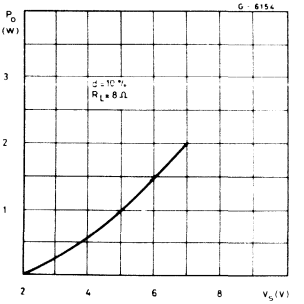


Fig. 11 - Distortion vs. output power (Bridge)

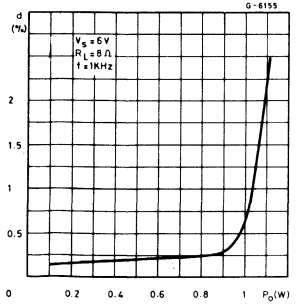


Fig. 12 - Total power dissipation vs. output power (Bridge)

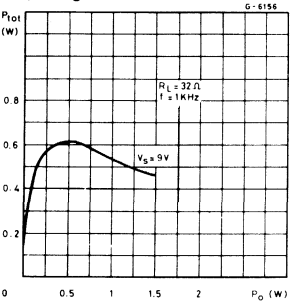


Fig. 13 - Total power dissipation vs. output power (Bridge)

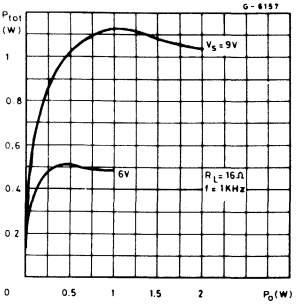


Fig. 14 - Total power dissipation vs. output power (Bridge)

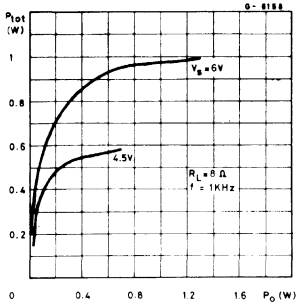


Fig. 15 - Total power dissipation vs. output power (Bridge)

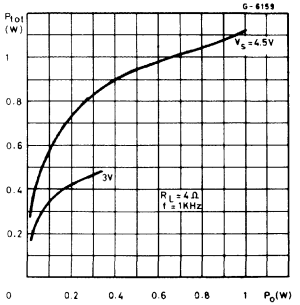


Fig. 16 - Typical application in portable players

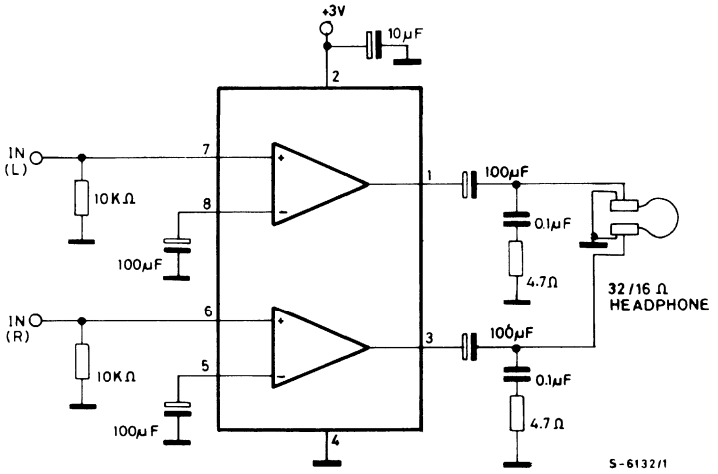


Fig. 17 - Application circuit for portable radio receivers

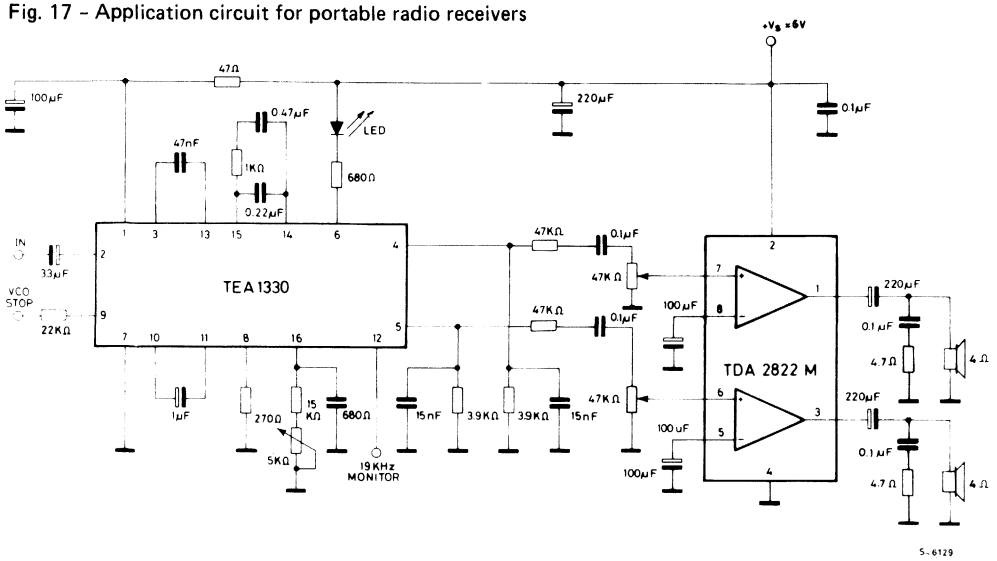
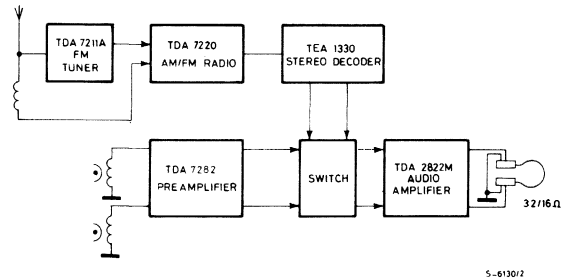
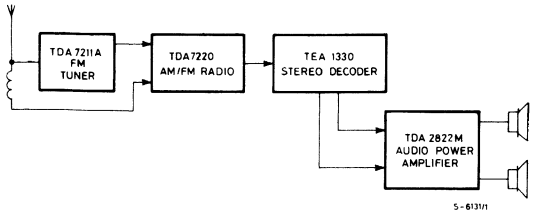


Fig. 18 - Portable radio cassette palyers



TYPE	SUPPLY VOLTAGE
TDA 7220	1.5V to 6V
TDA 7211A	1.2V to 6V
TEA 1330	3V to 15V
TDA 7282	1.5V to 6V
TDA 2822M	1.8V to 15V

Fig. 19 - Portable stereo radios



TYPE	SUPPLY VOLTAGE
TDA 7220	1.5V to 6V
TDA 7211A	1.2V to 6V
TEA 1330	3V to 15V
TDA 2822M	1.8V to 15V

Fig. 20 Low cost application for portable players (using only one 100μF output capacitor)

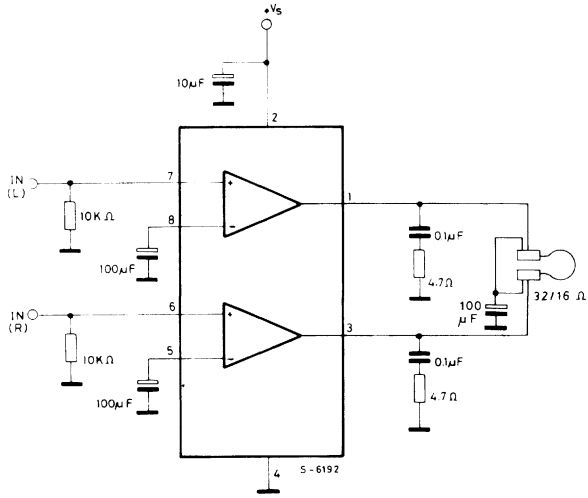
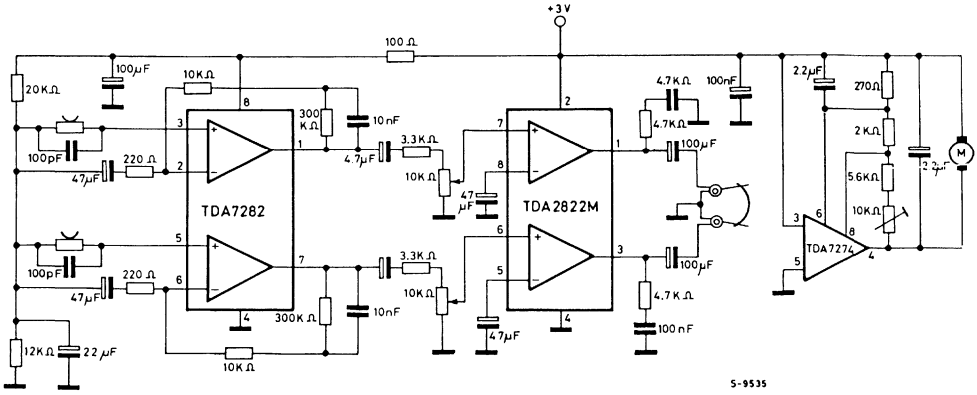


Fig. 21 - 3V Stereo cassette player with motor speed control



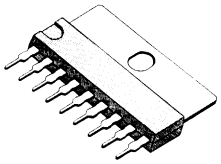
TDA2824S

ADVANCE DATA

DUAL POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 3V
- HIGH SVR
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2824S is a monolithic integrated circuit assembled in single line 9 pins package (SIP. 9), intended for use as dual audio power amplifier in portable radios and TV sets.



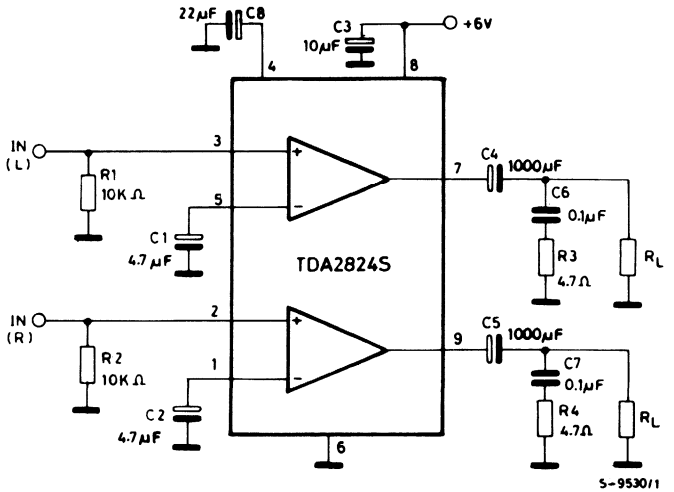
SIP. 9

ORDERING NUMBER: TDA2824S

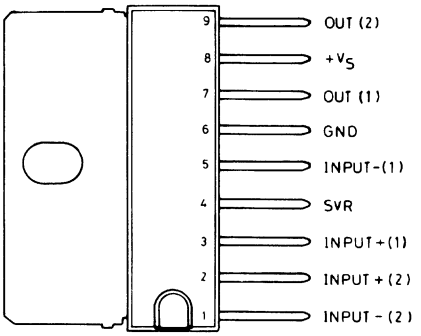
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output peak current	1.5	A
P_{tot}	Total power dissipation at $T_{amb} = 60°C$	1.3	W
	at $T_{case} = 70°C$	8	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TYPICAL APPLICATION CIRCUIT (Stereo)

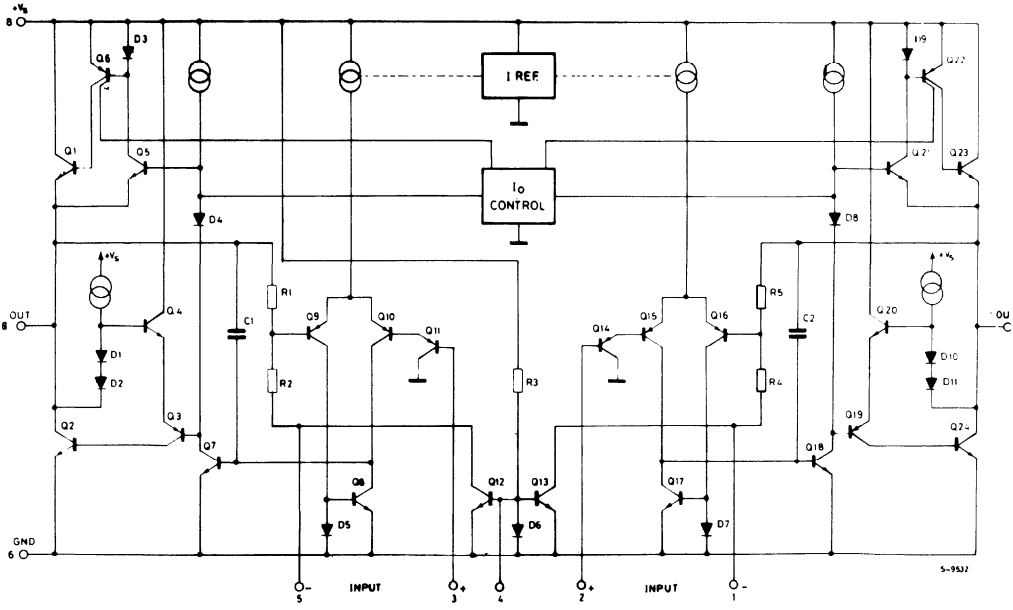


CONNECTION DIAGRAM
(Top view)



S-9531

SCHEMATIC DIAGRAM



S-9532

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	10	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
STEREO (Test circuit of Fig. 1)						
V_s	Supply voltage		3		15	V
V_c	Quiescent output voltage	V_s = 9V V_s = 6V		4 2.7		V V
I_d	Quiescent drain current			6	12	mA
I_b	Input bias current			100		nA
P_o	Output power (each channel)	d = 10% f = 1KHz V_s = 9V R_L = 4Ω V_s = 6V R_L = 4Ω V_s = 4.5V R_L = 4Ω	1.3 0.45	1.7 0.65 0.32		W W W
G_v	Closed loop voltage gain	f = 1KHz	36	39	41	dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_g = 10KΩ B = 22Hz to 22KHz		2.5		μV
		R_g = 10KΩ Curve A		2		μV
SVR	Supply voltage rejection	f = 100Hz	40	50		dB
CS	Channel separation	R_g = 10KΩ f = 1KHz		50		dB
BRIDGE (Test circuit of Fig. 3)						
V_s	Supply voltage		3		15	V
I_d	Quiescent drain current	R_L = ∞		6	12	mA
V_{os}	Output offset voltage	R_L = 8Ω		10	60	mV
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 8Ω V_s = 6V R_L = 8Ω V_s = 4.5V R_L = 4Ω	2.5 0.9	3.2 1.35 1		W W W
d	Distortion	f = 1KHz; R_L = 8Ω; P_o = 0.5W		0.2		%
G_v	Closed loop voltage gain	f = 1KHz		39		dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_g = 10KΩ B = 22Hz to 22KHz		3		μV
		R_g = 10KΩ Curve A		2.5		μV
SVR	Supply voltage rejection	f = 100Hz	50	60		dB

Fig. 1 - Test circuit (STEREO)

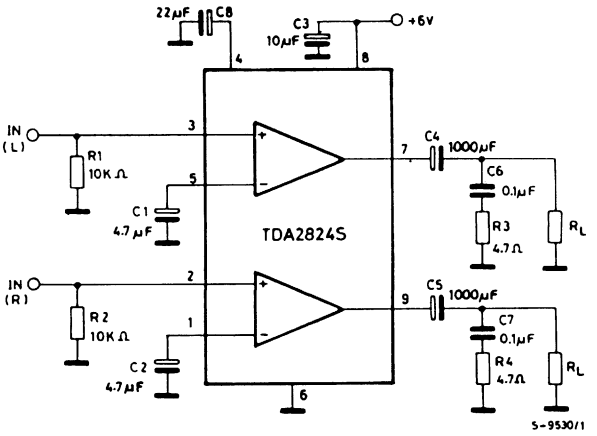


Fig. 2 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)

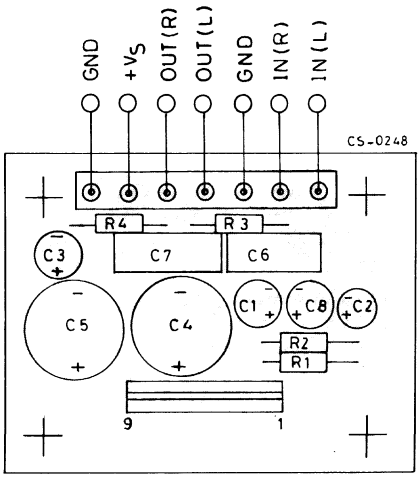


Fig. 3 - Test circuit (BRIDGE)

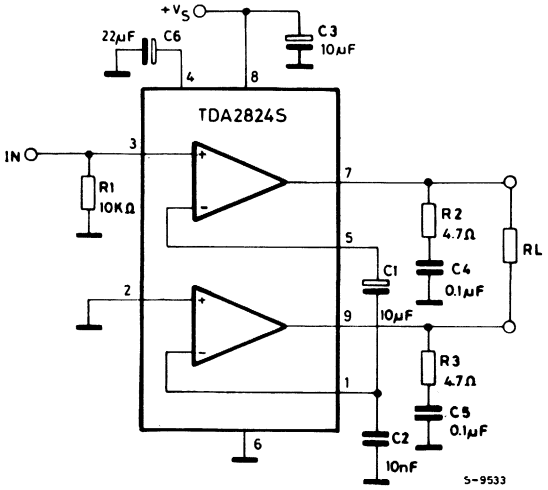


Fig. 4 - P.C. board and components layout of the circuit of the Fig. 3 (1 : 1 scale)

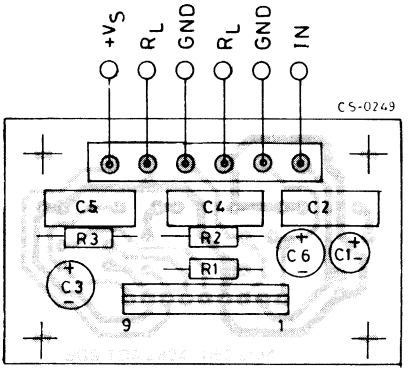


Fig. 5 - Output power vs. supply voltage (Stereo)

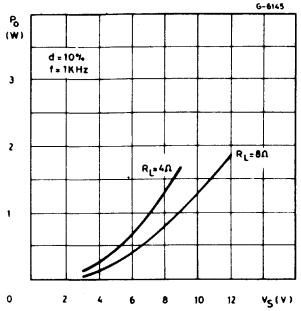


Fig. 6 - Output power vs. supply voltage (Bridge)

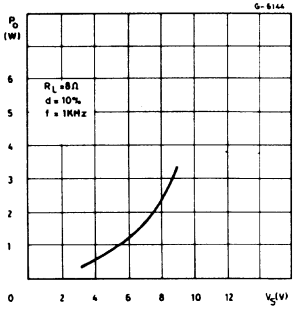


Fig. 7 - Distortion vs. output power (Bridge)

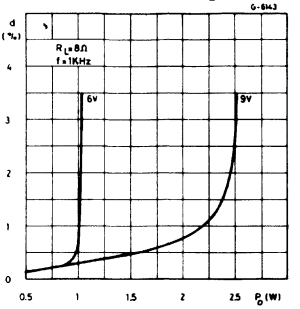


Fig. 8 - Distortion vs. output power (Bridge)

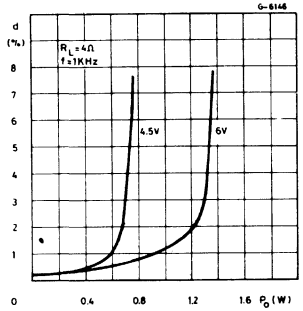


Fig. 9 - Supply voltage rejection vs. supply voltage (Stereo)

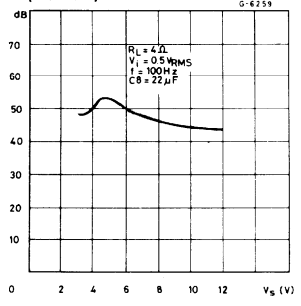


Fig. 10 - Supply voltage rejection vs. frequency (Stereo)

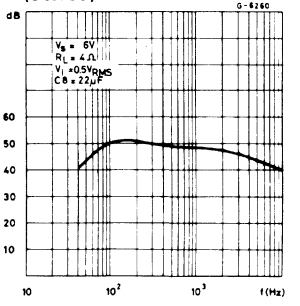


Fig. 11 - Quiescent current vs. supply voltage

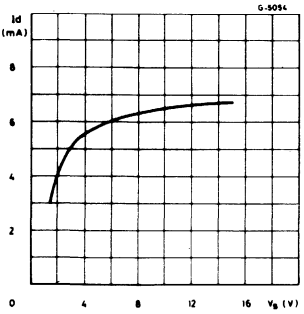


Fig. 12 - Total power dissipation vs. output power (Stereo)

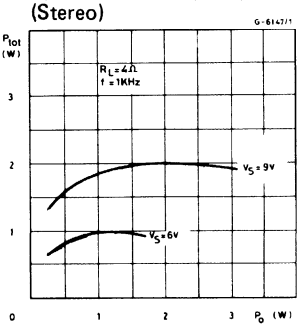
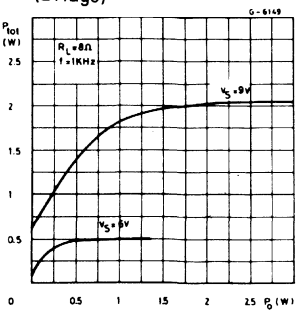


Fig. 13 - Total power dissipation vs. output power (Bridge)



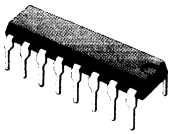
TDA3410

DUAL LOW NOISE TAPE PREAMPLIFIER WITH AUTOREVERSE

The TDA3410 is a dual preamplifier with tape autoreverse facility for the amplification of low level signals in applications requiring very low noise performance, as stereo cassette players. Each channel consists of two independent amplifiers. The first has a fixed gain of 30dB while the second one is an operational amplifier optimized for high quality audio application.

The TDA3410 is a monolithic integrated circuit in a 16-lead dual in-line plastic package and its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Wide supply range
- SVR = 120dB
- Large output voltage swing
- Tape autoreverse facility
- Short circuit protection



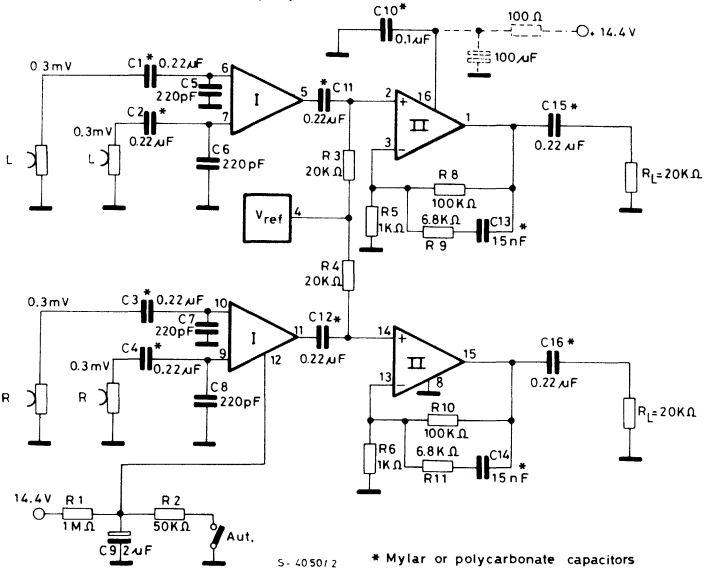
DIP-16 Plastic (0.4)

ORDERING NUMBER: TDA3410

ABSOLUTE MAXIMUM RATINGS

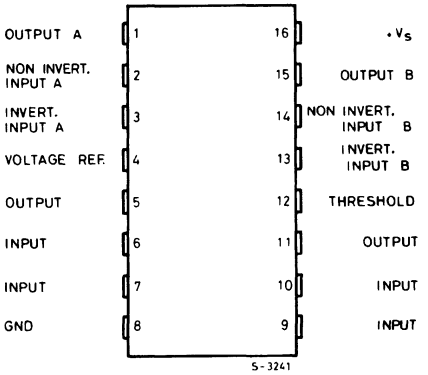
V_s	Supply voltage	36	V
P_{tot}	Total power dissipation at $T_{amb} = 60°C$	600	mW
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

Stereo preamplifier for autoreverse cassette players

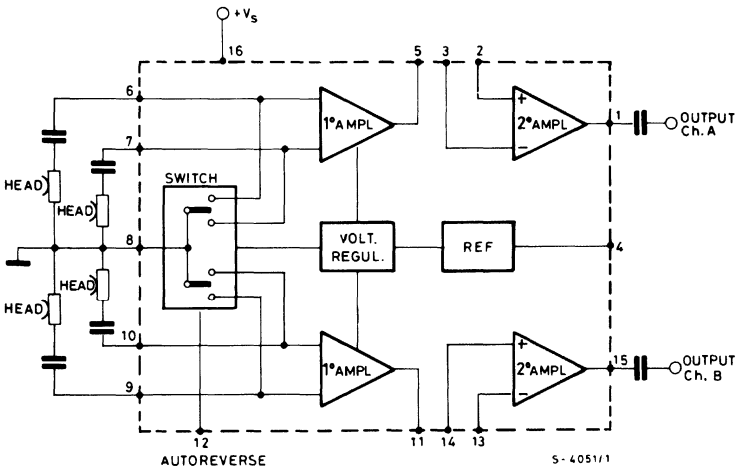


* Mylar or polycarbonate capacitors

CONNECTION DIAGRAM (top view)



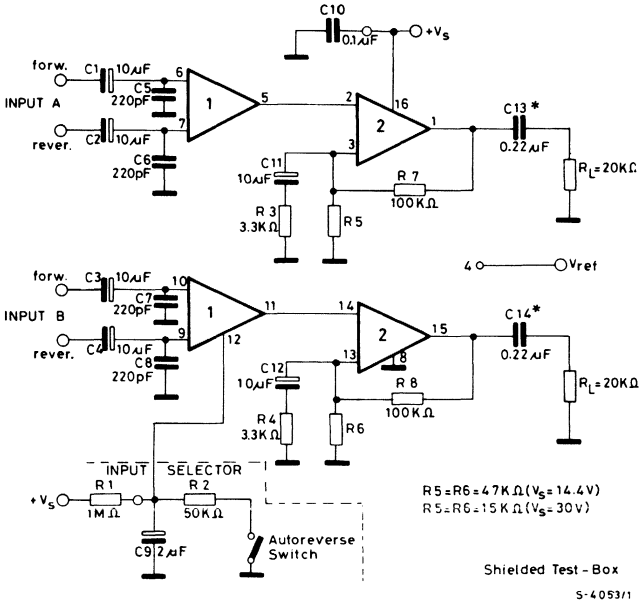
BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150	°C/W

TEST CIRCUIT (Flat Gain - G_v= 60 dB)



* Mylar or polycarbonate capacitors.

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s= 14.4V, G_v= 60 dB, refer to the test circuit, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current	V_s= 8V to 30V		10		mA
I_o	Output current (pins 1-15)	Source V_s= 8V to 30V		10		mA
		Sink		1		mA
G_v	Closed loop gain	f = 20 Hz to 20 KHz		60		dB
R_i	Input resistance	f = 1 KHz	50	80		KΩ
R_o	Output resistance (pins 1-15)	f = 1 KHz		50		Ω
THD	Total harmonic distortion	V_o= 300 mV f = 1 KHz		0.05		%
		f = 10 KHz		0.05		%

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_o	Output voltage swing (pins 1-15)	Peak to Peak	V_s= 14.4V V_s= 30V		12 28		.V V
V_o	Output voltage (pins 1-15)	d = 0.5% f = 1 KHz	V_s= 14.4V V_s= 30V		4 8		V_{rms} V_{rms}
e_n	Total input noise (°)	R_g= 50Ω R_g= 600Ω R_g= 5KΩ			0.25 0.4 1.3	 0.6 	μV μV μV
S/N	Signal to noise ratio (°)	V_{in}= 0.3 mV V_{in}= 1 mV	R_g= 600Ω R_g= 0		57 73		dB dB
CS	Channel separation	f = 1 KHz			60		dB
CT(°°°)	Cross-talk (differential input)	f = 1 KHz			80		dB
SVR	Supply voltage rejection (°°)	f = 1 KHz	R_g= 600Ω		120		dB
SVR (°°)	Of reference voltage (Pin 4)	f = 1 KHz R_g= 600Ω			100		dB
V_{ref}	Reference voltage (pin 4)				55		mV
R_{ref}	Ref. voltage output resistance (pin 4)				100		Ω
$\frac{\Delta V_{ref}}{\Delta T}$	Voltage temperature coefficient				10		μV/°C

(°) The weighting filter used for the noise measurement has a curve A frequency response.
(°°) Referred to the input.
(°°°) Between a disabled input and an input ON.

ELECTRICAL CHARACTERISTICS (Refer test circuit, V_s= 30V)

AMPLIFIER N° 1

Parameter		Test conditions	Min.	Typ.	Max.	Unit
G_v	Gain (pins 6 to 5)		29	30	30.5	dB
d	Distortion	V_o= 300 mV f = 1 KHz f = 10 KHz		0.05 0.05		%
e_n	Total input noise (°)	R_g= 600Ω		0.4		μV
Z_o	Output impedance (pin 5)	f = 1 KHz		100		Ω
I_o	Output current (pin 5)			1		mA
V_5	DC output voltage (pin 5)	V_s = 10V	1.3	2	2.7	V

AMPLIFIER N° 2

G_v	Open loop voltage gain (pins 2 to 1)			100		dB
I_B	Input bias current			0.2		μA
V_{os}	Input offset voltage			2		mV
I_{os}	Input offset current			0.05		μA
BW	Small signal bandwidth	G_v= 30 dB		150		KHz
e_n	Total input noise (°)	R_g= 600Ω		2		μV
R_i	Input impedance	f = 1 KHz (open loop)	150	500		KΩ

AUTOREVERSE

P_{in}	$V_{12} < 2V$	$V_{12} > 4.5V$
6 – 10	OFF	ON
7 – 9	ON	OFF

(°) The weighting filter used for the noise measurement has a curve A frequency response.

Fig. 1 - Total input noise vs. source resistance (curve A)

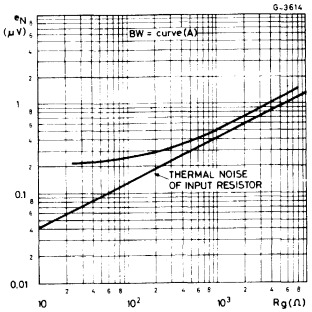


Fig. 2 - Total input noise vs. source resistance (BW= 22 Hz to 22 KHz)

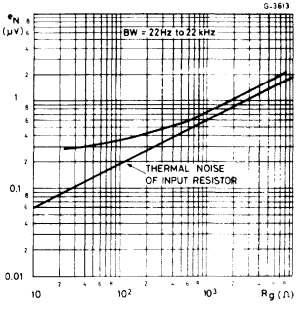


Fig. 3 - Total harmonic distortion vs. output voltage

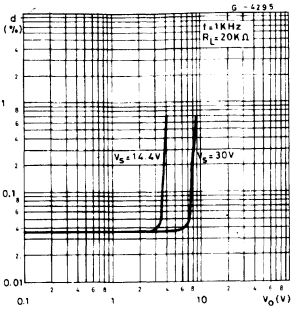


Fig. 4 - Very low noise stereo preamplifier for car cassette players (with Gap Loss Correction and autoreverse function)

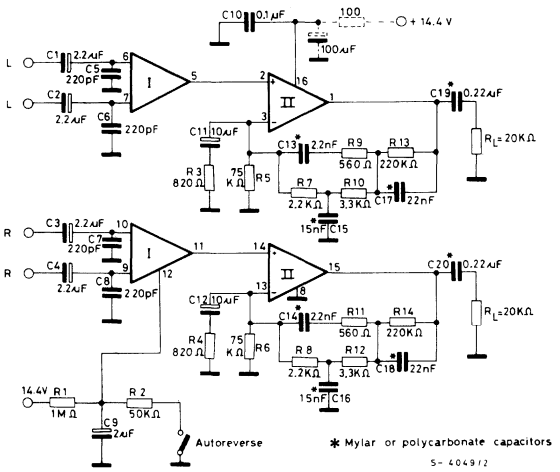


Fig. 5 - Frequency response

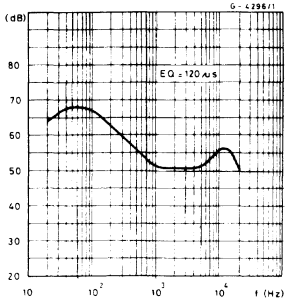


Fig. 6 - P.C. board and component lay-out (1:1 scale) for the circuit of fig. 4

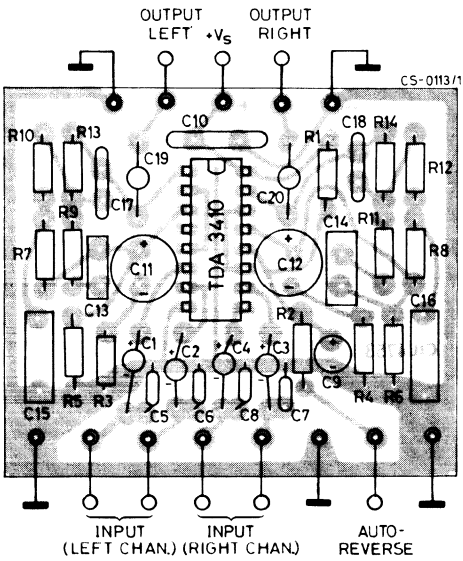


Fig. 7 - Stereo preamplifier for car cassette players, with low value capacitors (Autoreverse function)

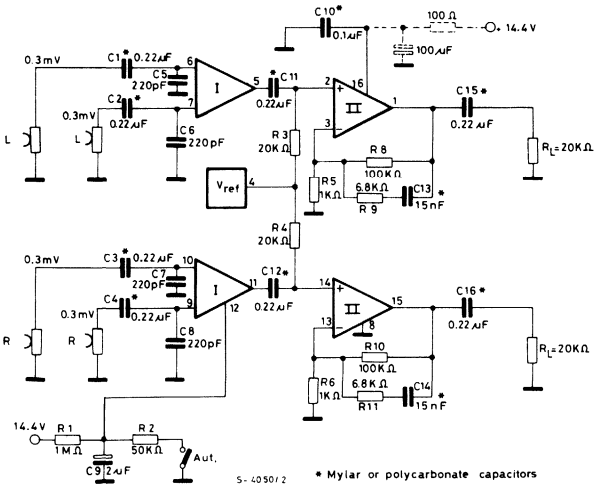
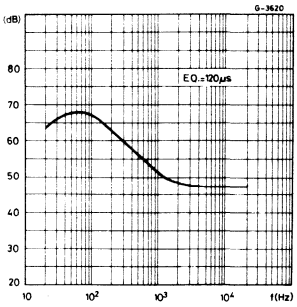


Fig. 8 - Frequency response

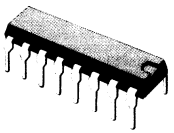


TDA3420

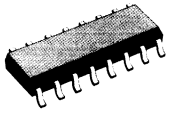
DUAL VERY LOW NOISE PREAMPLIFIER

The TDA 3420 is a dual preamplifier for applications requiring very low noise performance, **as stereo cassette players** and quality audio systems. Each channel consists of two independent amplifiers.
The first one has a fixed gain while the second one is an operational amplifier for audio application.
The TDA 3420 is available in two packages: 16-lead dual in-line plastic and 16 lead micropackage.
Its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Large output voltage swing
- Short circuit protection



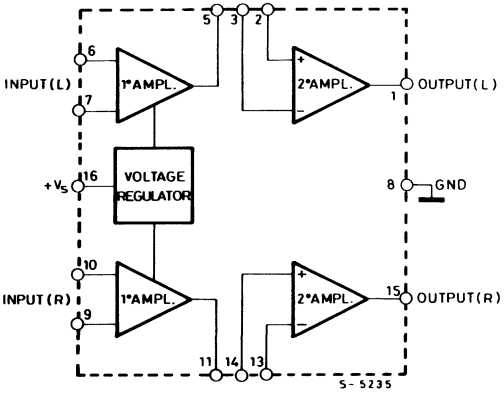
DIP-16 Plastic
(0.4)



SO-16J

ORDERING NUMBER: TDA3420 (DIP-16)
TDA3420D (SO-16)

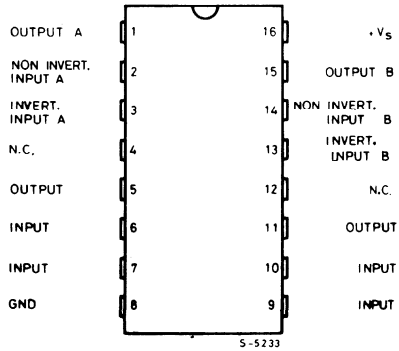
BLOCK DIAGRAM (Pin numbers refer to the DIP)



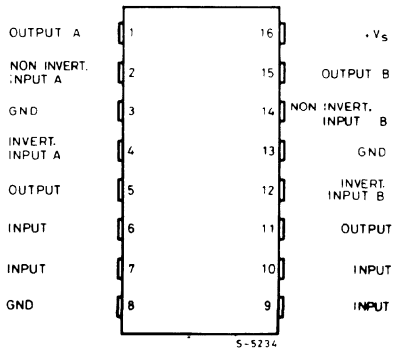
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 70°C Dip	550	mW
	SO-16	400	mW
T_j, T_{stg}.	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAMS



DIP



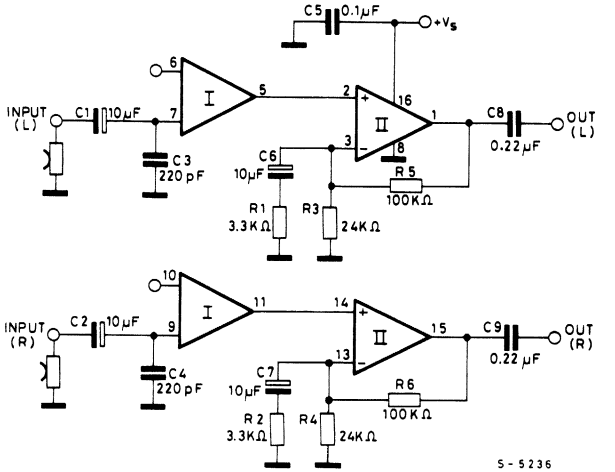
SO-16

THERMAL DATA

			DIP	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150 °C/W	200°C/W(*)

* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

Fig. 1 - Test circuit



Note: Pin numbers refer to DIP.

Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1:1 scale)

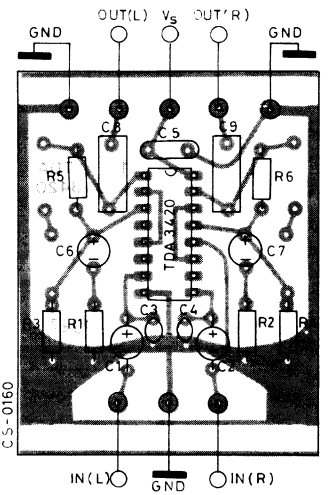
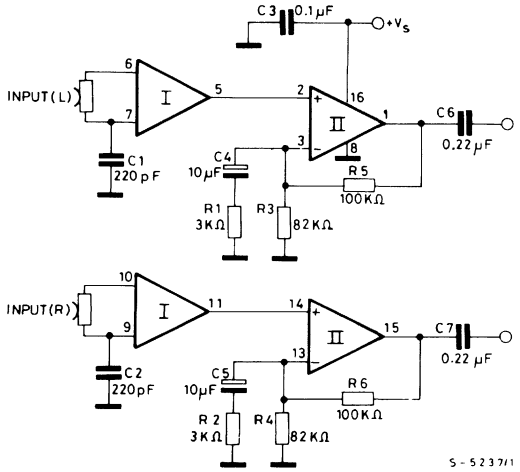


Fig. 3 - Test circuit without input capacitors



Note: Pin numbers refer to the DIP.

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s= 14.4V, G_v= 60 dB refer to the test circuit of fig. 1, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_s	Supply current	V_s= 8V to 20V			8		mA
I_o	Output current	Source	V_s= 8V to 20V		10		mA
		Sink			1		mA
G_v	Gain	f = 1 KHz			60		dB
R_i	Input resistance			50	100		KΩ
R_o	Output resistance				50		Ω
THD	Total harmonic distortion without noise	V_o= 300 mV	f = 1 KHz		0.05		%
			f = 10 KHz		0.05		%
V_o	Peak to peak output voltage	f = 40 Hz to 15 KHz			12		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
e_n	Total input noise (°)	R_s= 50 Ω R_s= 600 Ω R_s= 5 KΩ		0.25 0.4 1.3	0.7	μV μV μV
S/N	Signal to noise ratio (°)	V_{in}= 0.3 mV R_s= 600 Ω V_{in}= 1 mV R_s= 0		57 73		dB
	(°°)	V_{in}= 0.3 mV R_s= 600 Ω V_{in}= 1 mV R_s= 0		55 71		dB
CS	Channel separation	f = 1 KHz		60		dB
SVR	Supply voltage rejection (°°°)	f = 1 KHz R_s= 600 Ω		110		dB

AMPLIFIER N° 1

G_v	Gain (pin 6 to pin 5)		27.5	28.5	29	dB
d	Distortion	V_o= 300 mV f = 1 KHz f = 10 KHz		0.05 0.05		%
e_n	Total input noise (°)	R_s= 600Ω		0.4		μV
Z_o	Output impedance (pin 5)	f = 1 KHz		100		Ω
I_o	Output current (pin 5)			1		mA
V5	DC output voltage (pin 5)	Test circuit fig. 3		2.8		V
		Test circuit fig. 1	1.0	1.5		

AMPLIFIER N° 2

G_v	Open loop voltage gain			100		dB
I_B	Input bias current			0.2		μA
V_{os}	Input offset voltage			2		mV
I_{os}	Input offset current			50		nA
e_n	Total input noise (°)	R_s= 600Ω		2		μV
R_i	Input impedance	f = 1 KHz (open loop)	150	500		KΩ

(°) Weighting filter : curve A.
(°°) Weighting filter : Dolby CCIR/ARM.
(°°°) Referred to the input.

Fig. 4 - Total input noise vs. source resistance (curve A)

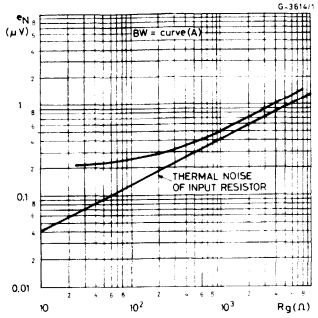


Fig. 5 - Total input noise vs. source resistance(BW=22Hz to 22 KHz)

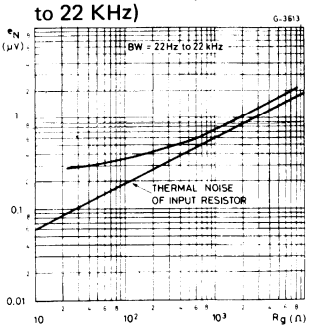


Fig. 6 - Total harmonic distortion vs. output voltage

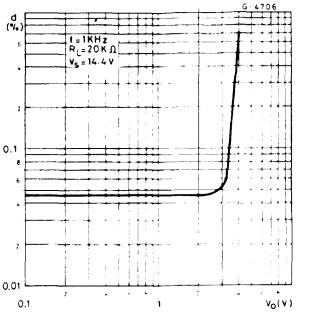


Fig. 7 - Output voltage vs. frequency

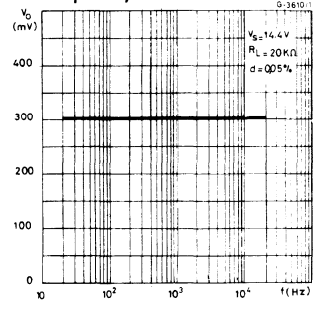


Fig. 8 - Distortion vs. input level (test circuit of fig. 1)

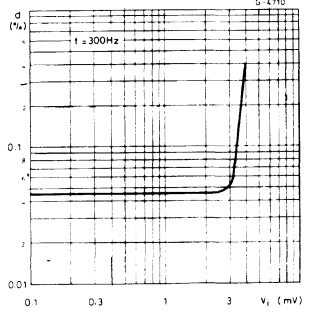


Fig. 9 - Frequency response of the circuit of fig. 10

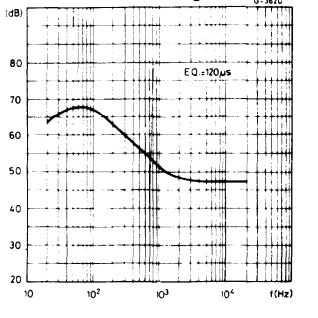
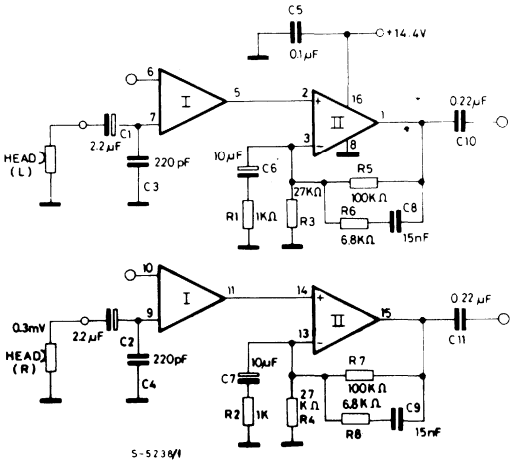


Fig. 10 - Very low noise stereo preamplifier for cassette players



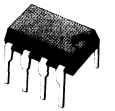
TDA7211A

ADVANCE DATA

LOW VOLTAGE FM FRONT END

- LOW OSCILLATOR RADIATION
- OPERATING SUPPLY VOLTAGE: 1.3V TO 6V
- EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE
- HIGH SIGNAL HANDLING
- FEW EXTERNAL COMPONENTS
- BUILT-IN VARICAP FOR AFC
- MINIDIP PACKAGE PERMITS RATIONAL LAYOUT AND LOW PROFILE
- COVERS JAPANESE, US AND EUROPEAN BANDS

The TDA7211A is a monolithic FM turner suitable for portable radio and radio/cassette player applications where a very low supply voltage is used and compactness is an important design consideration. It contains an RF amplifier, balanced mixer, one-pin local oscillator and a varicap diode for AFC. Very few external components are required. Mounted in a Minidip or SO-8 package, the TDA7211A is particularly suitable for slimline cassette-type radios.

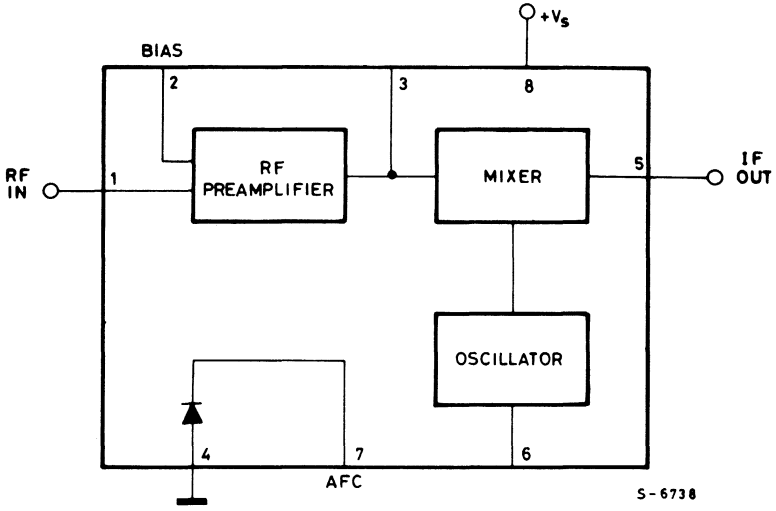


Minidip Plastic

SO-8

ORDERING NUMBER: TDA7211A (Minidip)
TDA7211D (SO-8)

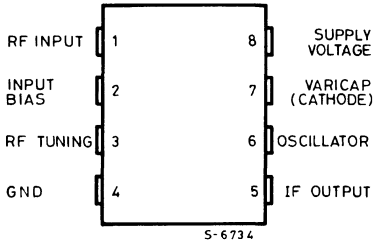
BLOCK DIAGRAM



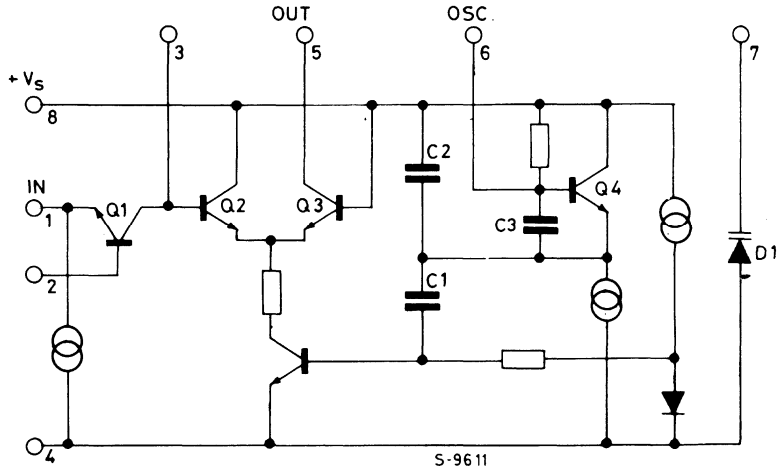
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	7	V
P_{tot}	Total power dissipation at $T_{amb} < 70°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 3V, test circuit of fig. 1, T_{amb}= 25°C, unless otherwise specified)

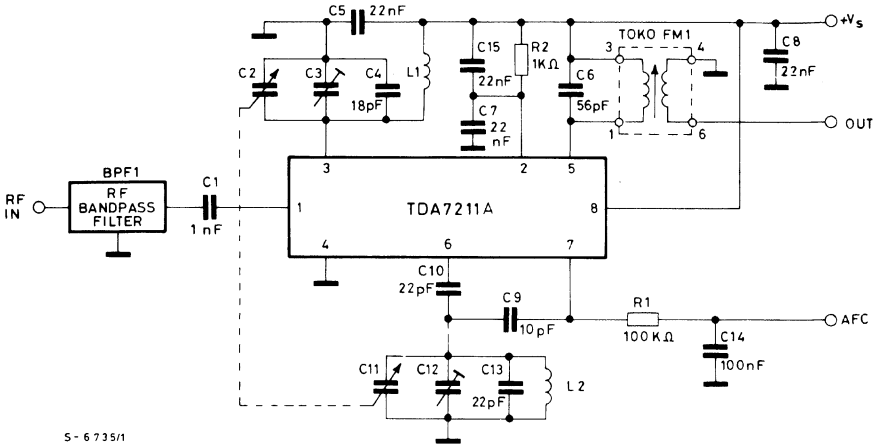
Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			1.3	3	6	V
V_{osc}	Local oscillator voltage					330	mV_{rms}
I_s	Supply current	V_s = 1.5 to 4.5V		2	3	4.5	mA
C_{AFC}	AFC diode capacitance	V_{AFC}= 1V			4		pF
K(*)	AFC diode variation	V_{AFC}= 1 to 3V			0.24		
G_c(**)	Conversion gain	V_s = 3V	f = 83 MHz f = 98 MHz	25 25	34 34		dB
		V_s = 1.6V	f = 83 MHz f = 98 MHz		32 32		dB
V_{STP}	Local oscillator stop voltage				1.2		V

(*) $K = \frac{C\,(1V) - C\,(3V)}{C\,(3V)}$ (**) R_i = 75Ω; R_L = 300Ω

TYPICAL DC VOLTAGES (test circuit)

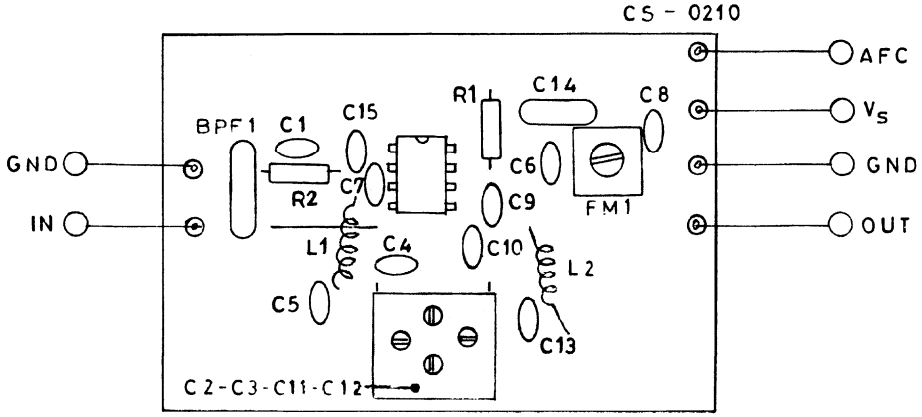
Pin	1	2	3	4	5	6	7	8
(V)	2.3	3	3	0	3	2.9	0	3

Fig. 1 - Test circuit



BPF1 = TAIYO YUDEN - B10861
C_V = C2, C3, C11, C12 = 20 + 20 pF
L1 = RF coil - 5 turns - 0.6 mm/4 mm.
L2 = OSC. coil - 4 turns - 0.6 mm/4 mm.

Fig. 2 - P.C. board and components layout of the test circuit (1:1 scale)



APPLICATION INFORMATION

Fig. 3 - Typical application for portable AM/FM radio

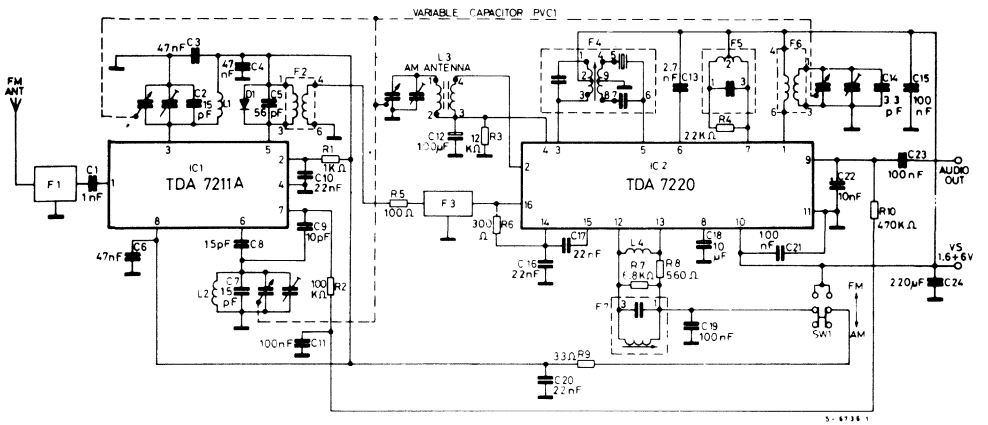
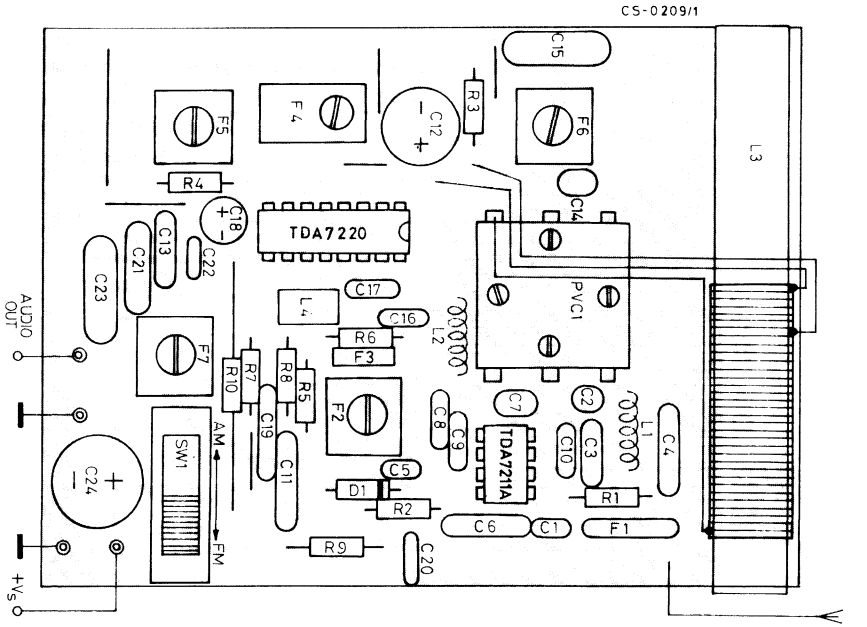


Fig. 4 - P.C. board and components layout of the circuit of fig. 3 (1:1 scale)



APPLICATION INFORMATION (continued)

PARTS LIST (Radioreceiver of fig. 3)

Code number	Value	Description
PVC 1	FM 20 pF x 2 AM 140/82 pF	TOKO POLYVARICON QT 22124
L1	ϕ 4 mm. - 5 T # 0.6 mm.	FM RF COIL
L2	ϕ 4 mm. - 4 T # 0.6 mm.	FM OSC. COIL
L3	600 μH PRIMARY SEC. - 7 TURNS	AM ANT. COIL with ferrite bar ϕ 10 mm. x 80 mm.
L4	22 μH INDUCTOR	TOKO 144LY - 220K
D1	AA 119	GE DIODE
F1	TAIYO YUDEN BPF10861K	FM BAND PASS FILTER
F2	TOKO FM1 - 154 AN - 7A5965R	FM IFT
F3	SFE 10.7 MA	CERAMIC FILTER
F4	TOKO CF2 455C	AM IFT WITH CERAMIC FILTER
F5	TOKO AM2 RLC - 4A7524EK	AM DET. COIL
F6	TOKO RWO - 6A6574N	AM OSC. COIL
F7	TOKO KACS - K586HM	FM DIS. COIL

Typical performance of the radio receiver of fig. 3

Parameter		Test conditions		V_s = 3V	V_s = 1.6V
WAVEBANDS	FM			87 to 109 MHz	
	AM			523 to 1620 KHz	
SENSITIVITY	FM	S/N = 26 dB	$\Delta f = \pm$ 22.5 KHz	1.8 μV	2 μV
	AM	S/N = 20 dB	m = 0.3	400 μV	400 μV
AUDIO SIGNAL OUT	FM	$\Delta f = \pm$ 22.5 KHz		70 mV	55 mV
	AM	V_i = 1 mV/m	m = 0.3	80 mV	75 mV
DISTORTION (f_m= 1 KHz)	FM	V_i = 1 mV	$\Delta f = \pm$ 22.5 KHz	0.35%	0.5%
			Δf = 75 KHz	0.7%	0.75%
	AM	5 mV/m	m = 0.3	0.8%	0.8%
		100 mV/m	m = 0.8	2%	1.9%
SIGNAL TO NOISE (f_m= 1 KHz)	FM	V_i = 1 mV	$\Delta f = \pm$ 22.5 KHz	50 dB	50 dB
	AM	V_i = 1 mV/m	m = 0.3	33 dB	32 dB
AMPLITUDE MODULATION REJECTION	FM	V_i = 1 mV	Δf = 22.5 KHz m = 0.3	32 dB	31 dB
TWEET	2nd H.	f = 911 KHz		1%	1%
	3rd H.	f = 1370 KHz		0.2%	0.2%
QUIESCENT CURRENT				13.5 mA	12.5 mA

APPLICATION INFORMATION (continued)

Inversion of "S" shaped curve in quadrature discriminators

In FM receivers, the frequency used for the local oscillator is usually greater than the receiving frequency.

Anyway, in some cases it may be required to work with a local oscillator showing a frequency lower than the frequency of the received signal. According to this choice, the "S" shaped curve of the discriminator is therefore either positive or negative (the output d.c. voltage either increases or decreases as the input frequency increases) and the varicap diode of the AFC will have to be referred either to ground or to a reference voltage. The additional reference voltage may be circuitally unsuitable, besides increasing the costs. In the case of circuits using the monolithic tuner TDA7211 (internal varicap diode, with a side already connected to ground) the things would get still more complicated.

To overcome the problem, figure 5 shows a simple circuit solution to perform the inversion. The traditional diagram is shown in figure 6 for comparision.

This solution may be used with all the SGS radio circuits (TDA7220, TDA1220B, etc.) with performance equal to that achieved through the conventional circuitry.

In the diagram shown, the inversion of the curve is obtained through the replacement of the inductive reactance (normally 22 μH) with a capacitance (12 pF) and the recovery of the d.c. voltages through L3.

L3, which is forced to resonance and strongly smoothed by R1, also performs the function of resistive load across the collector of the output transistor in IF limiter.

The described circuit doesn't modify the ease of calibration of the quadrature discriminators, makes the amplitude modulation rejection (AMR) more continuous and significantly reduces the harmonic radiation from the last limiter stage.

Fig. 5

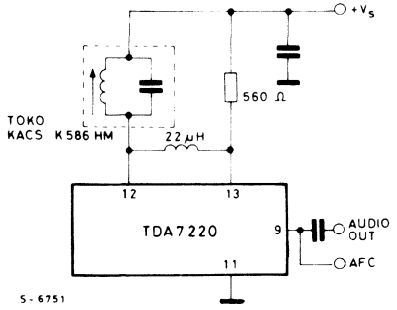
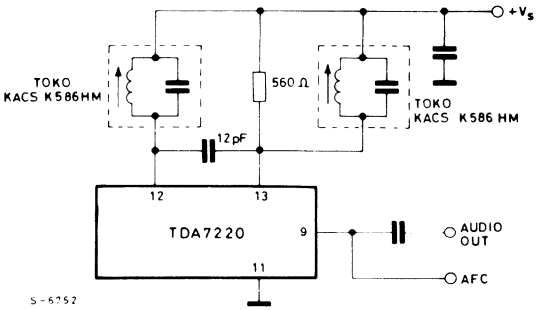


Fig. 6



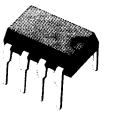
TDA7212

PRELIMINARY DATA

LOW VOLTAGE FM XTAL CONTROLLED FRONT-END

The TDA 7212 is a monolithic integrated circuit in a 8 pin minidip package designed for general purpose xtal controlled FM front-end up to 140 MHz.
The TDA 7212 main features are:

- 1.3V min supply voltage
- RF preamplifier
- Balanced mixer
- Xtal controlled oscillator (fundamental and overtone)
- Low oscillator radiation
- High signal handling

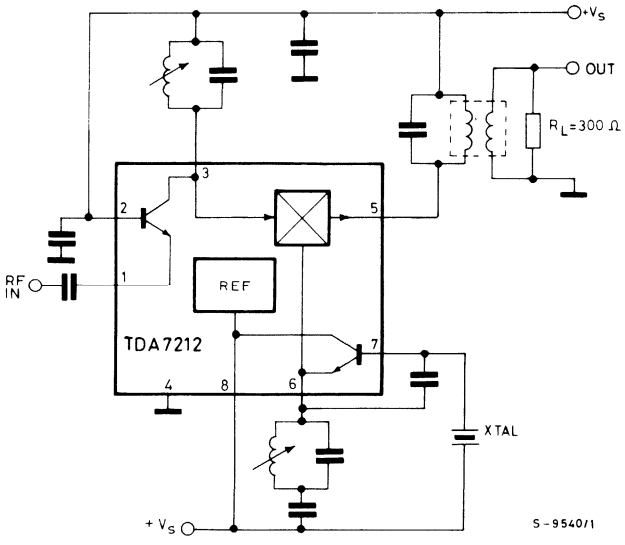


Plastic Minidip

SO-8

ORDERING NUMBERS: TDA7212 (MINIDIP)
TDA7212D (SO-8)

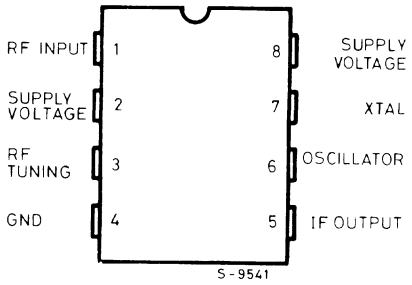
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	7	V
P_{tot}	Total power dissipation at $T_{amb} < 70°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(top view)



ELECTRICAL CHARACTERISTICS (V_s = 3V, T_{amb} = 25°C unless otherwise specified Refer to Test circuit)

Parameter		Test Condition	Min.	Typ.	Max.	Unit
V_s	Supply votage			3	6	V
I_s	Supply current			3		mA
V_{osc}	Local oscillator voltage (pin 6)			200		mVrms
G_v	Voltage gain	f = 49MHz, R_{in}= 75Ω, R_{out}= 300Ω		40		dB
V_{off}	Local oscillator stop voltage			1.2		V

Typical DC voltages (refer to the test circuit)

pins	1	2	3	4	5	6	7	8
(V)	2.3	3	3	0	3	2.1	2.9	3

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

Fig. 1 - Test circuit

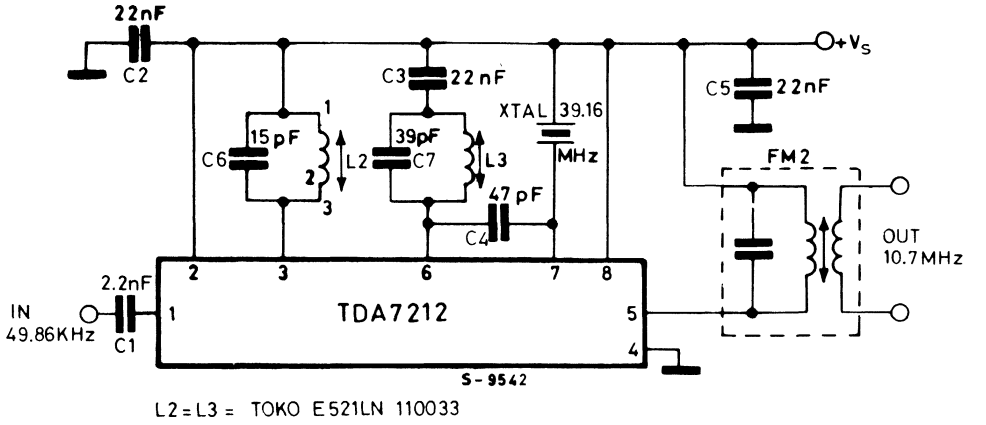
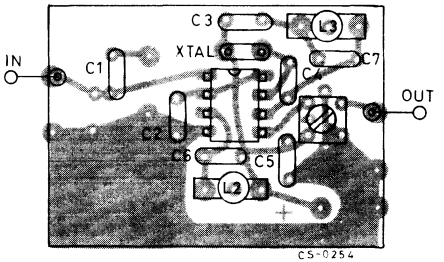


Fig. 2 - P.C. board and component layout of the test circuit of fig. 1 (1:1 scale)



APPLICATION INFORMATION

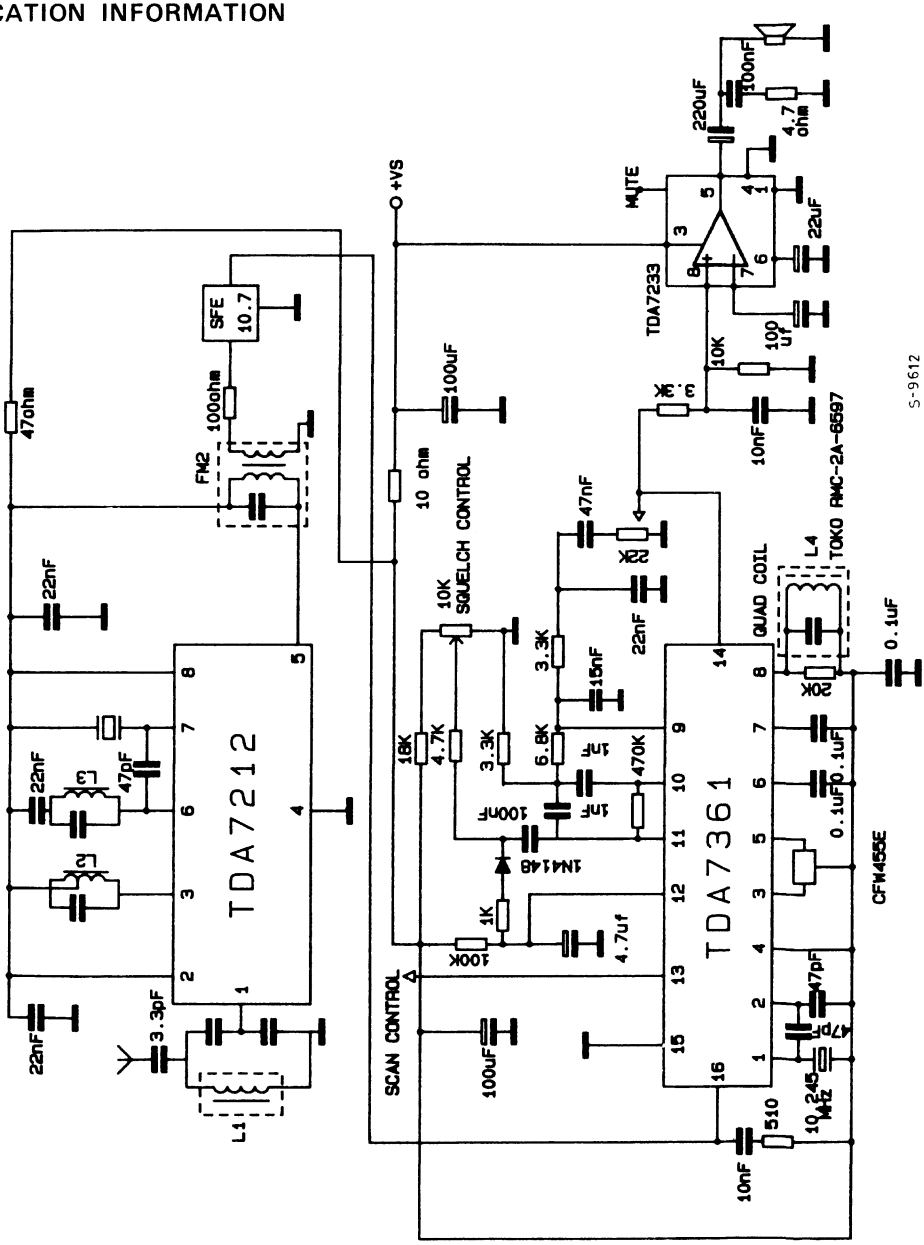
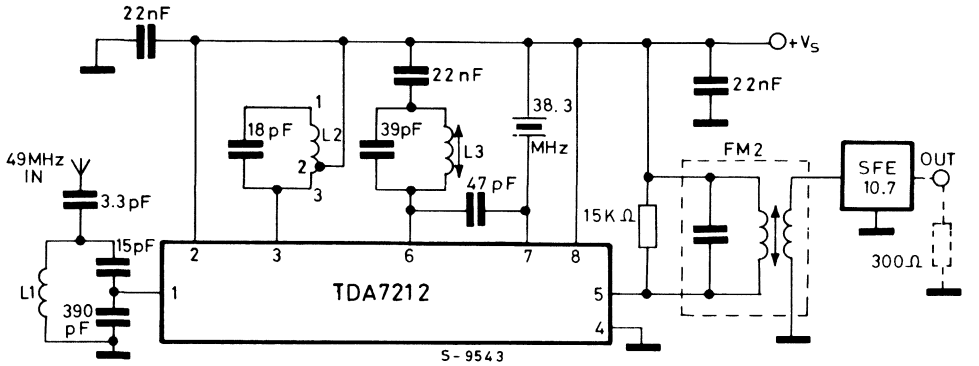


Fig. 3 – 49 MHz double conversion receiver.

APPLICATION INFORMATION (continued)

Fig. 4 - Front-end for cordless



L1 = L3 = TOKO E521LN 110033

N.B.: In this application it is advisable to decrease the gain of the front-end through a tapping on the L2 coil (3 turns of 12). So it can be obtained: better selectivity, improved intermodulation performance, better metching with the following block that are IC's designed for double conversion radio receivers.

TDA7220

PRELIMINARY DATA

VERY LOW VOLTAGE AM-FM RADIO

- OPERATING SUPPLY VOLTAGE: 1.5 to 6V
- HIGH SENSITIVITY AND LOW NOISE
- LOW BATTERY DRAIN
- VERY LOW TWEET
- HIGH SIGNAL HANDLING
- VERY SIMPLE DC SWITCHING OF AM-FM
- AM SECTION OPERATES UP TO 30 MHz

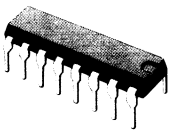
The TDA 7220 is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in 3V, 4.5V and 6V portable AM-FM radio receivers.
The functions incorporated are:

AM SECTION

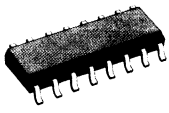
- Preamplifier and double balanced mixer with AGC
- On pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

FM SECTION

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier



DIP-16 Plastic (0.25)



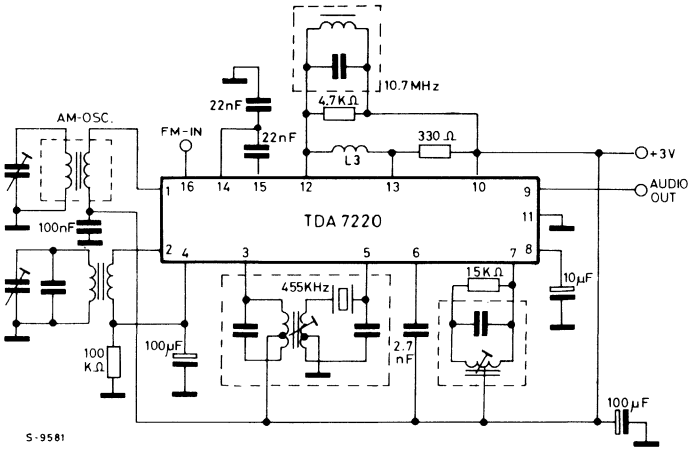
SO-16J

ORDERING NUMBERS: TDA7220 (DIP-16)
TDA7220D (SO-16)

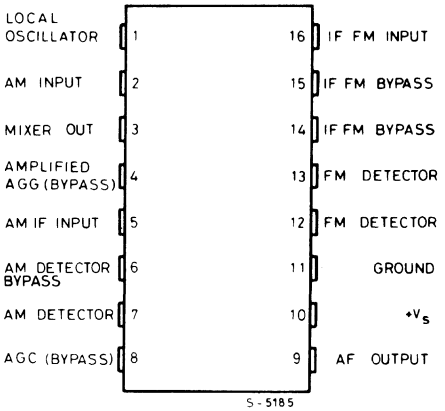
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	6.5	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$ (DIP-16)	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

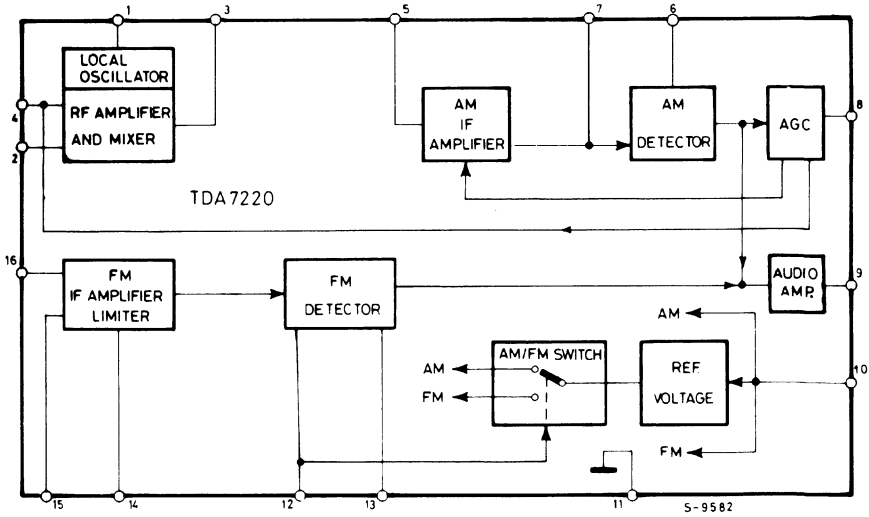
TYPICAL APPLICATION



CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA			DIP-16	SO-16	
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	200	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 3V unless otherwise specified, refer to test circuit)

	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_d	Drain current	AM section			11	18	mA
		FM section			10	15	mA
AM SECTION (f_o = 1 MHz; f_m = 1 KHz)							
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		12	25	μV
S/N	Signal to noise	V_i = 1 mV	m = 0.3	40	50		dB
ΔV_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	90			dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	40	80	110	mV
d	Distortion				0.6		%
V_H	Max input signal handling capability	m = 0.8	d < 10%	0.5			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)				4.5		KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB
FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)							
V_i	Input limiting voltage	-3 dB limiting point			33	80	μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3		40		dB
S/N	Signal to noise	Δf = ± 22.5 KHz	V_i = 1 mV	50	65		dB
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.3		%
		Δf = ± 75 KHz			1.1	1.5	%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV	40	70	90	mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)				4.5		KΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 1.6V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_d	Drain current	AM section			8	15	mA
		FM section			7	13	mA
AM SECTION (f_o = 1 MHz; f_m = 1 KHz)							
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		15	25	μV
S/N	Signal to noise	V_i = 1 mV	m = 0.3	40	48		dB
V_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	90			dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	40	75		mV
d	Distortion				0.5		%
V_H	Max input signal handling capability	m = 0.8	d < 10%	0.5			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)				4.5		KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB
FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)							
V_i	Input limiting voltage	-3 dB limiting point			50		μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3		34		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz	V_i = 1 mV		55		dB
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.6		%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV		55		mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)				4.5		KΩ

Fig. 1 - Test circuit

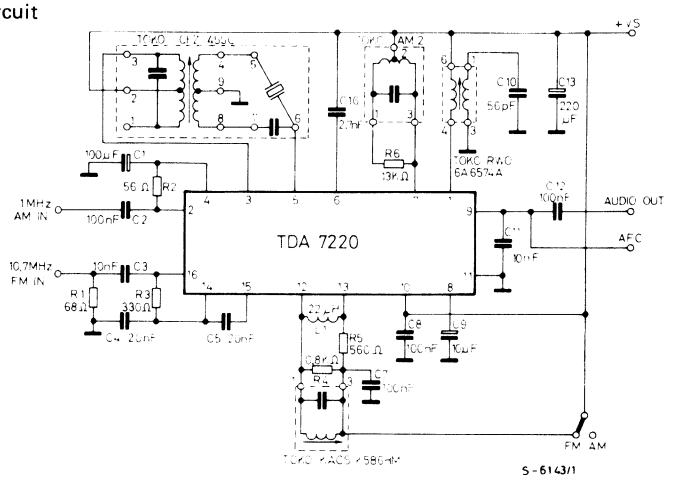
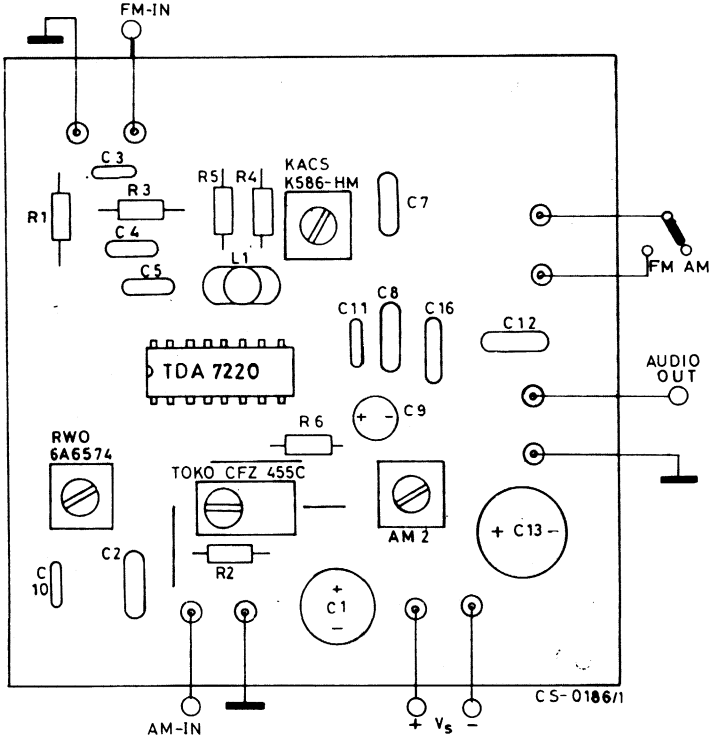


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit



AM-FM SWITCHING

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

Typical DC voltage (refer to the test circuit)

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Unit
AM	3	1.1	3	1.1	1.1	2.5	3	0.7	1.2	3	0	2.1	2.1	2.9	3	2.9	V
FM	3	0	3	0	0	2.4	3	0	0.9	3	0	3	3	2.7	2.7	2.7	V

APPLICATION SUGGESTION

Recommended values referred to the test circuit of Fig. 1

Part number	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C1	100 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C2 (*)	100 nF	AM input DC cut		
C3 (*)	10 nF	FM input DC cut		
C4 C5	20 nF 20 nF	FM amplifier bypass	Reduction of sensitivity	– Bandwidth increase – Higher noise
C7	100 nF	FM detector decoupling	Danger of RF irradiation	
C8	100 nF	Power supply bypass	Noise increase of the audio output	
C9	10 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C10 (*)	56 pF	Tuning of the AM oscillator at 1455 KHz		
C11	10 nF	50 μs FM de-enphasis		
C12	100 nF	Output DC decoupling	Low audio frequency cut	
C13	220 μF	Power supply decoupling	Increase of the distortion at low frequency	
C16	2.7 nF	AM detector capacitor	Low suppression of the IF frequency and harmonics	Increase of the audio distortion
R1 (*)	68 ohm	FM input matching		
R2 (*)	56 ohm	AM input matching		
R3	330 ohm	Ceramic filter matching		
R4	6.8 Kohm	FM detector coil Q setting	Audio output decrease and lower distortion	Audio output increase and higher distortion
R5	560 ohm	FM detector load resistor	Audio output decrease and higher AMR	
R6	13 Kohm	AM detector coil Q setting	Lower IF gain and Lower AGC range	Higher IF gain and lower AGC range

(*) Only for test circuit.

Fig. 3 - Audio output and noise vs. input signal (AM section) $V_s = 3V$

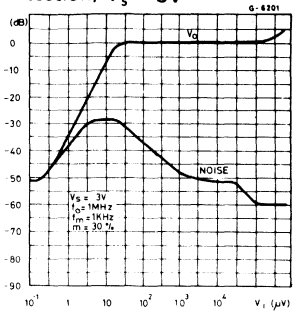


Fig. 4 - Audio output and noise vs. input signal (AM section) $V_s = 1.6V$

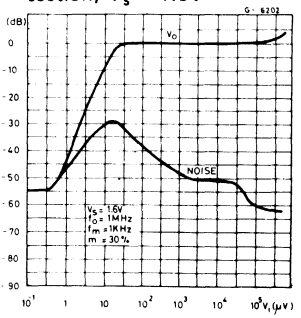


Fig. 5 - Distortion vs. input signal (AM section) $V_s = 3V$

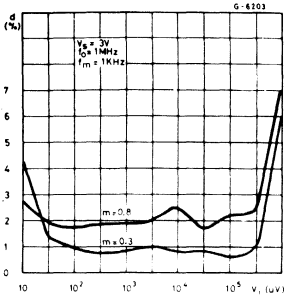


Fig. 6 - Distortion vs. input signal (AM section) $V_s = 1.6V$

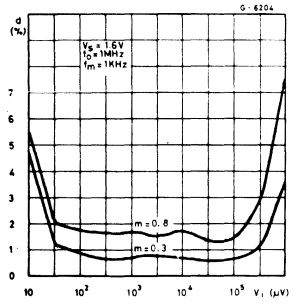


Fig. 7 - Audio output vs. supply voltage (AM section)

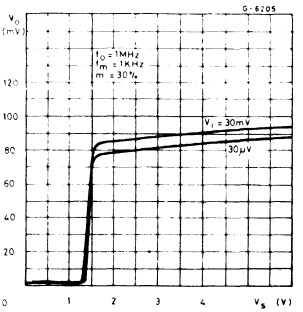


Fig. 8 - Amplified AGC voltage (pin 4) vs. input signal (AM section)

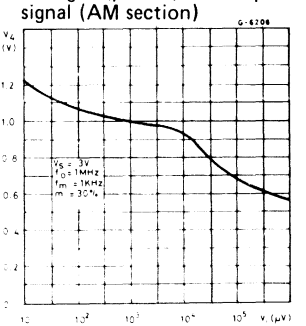


Fig. 9 - Audio output and noise vs. input signal (FM section) $V_s = 3V$

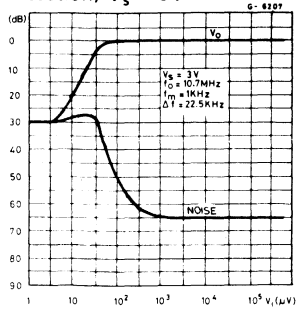


Fig. 10 - Audio output and noise vs. input signal (FM section) $V_s = 1.6V$

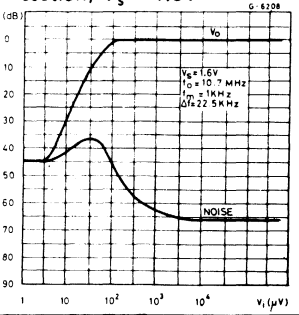


Fig. 11 - Distortion vs. input signal (FM section) $V_s = 3V$

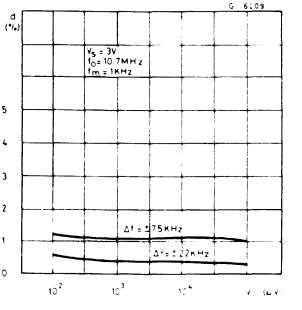


Fig. 12 - Distortion vs. input signal (FM section) $V_s = 1.6V$

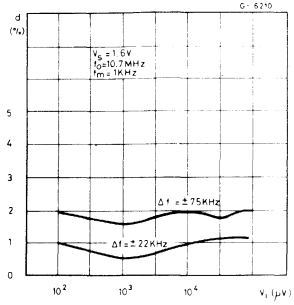


Fig. 13 - Audio output vs. supply voltage (FM section)

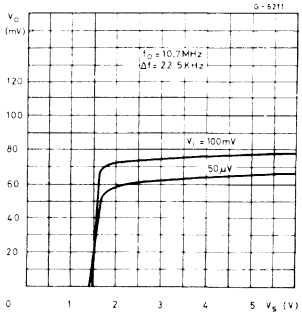


Fig. 14 - Amplitude modulation rejection vs. input signal (FM section)

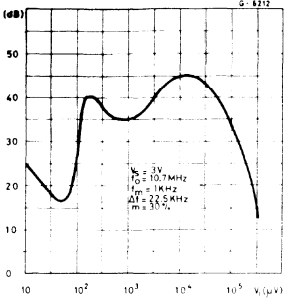


Fig. 15 - DC output voltage (pin 9) vs. supply voltage (FM section)

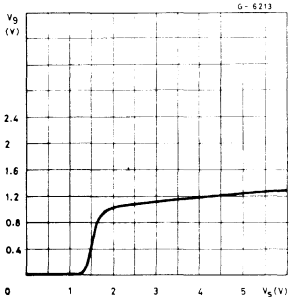


Fig. 16 - AFC output voltage (pin 9) vs. frequency deviation (FM section)

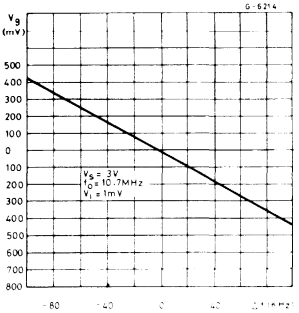
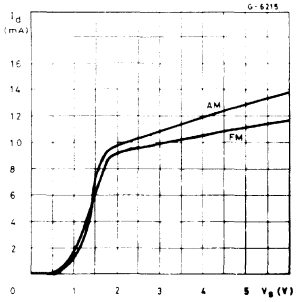
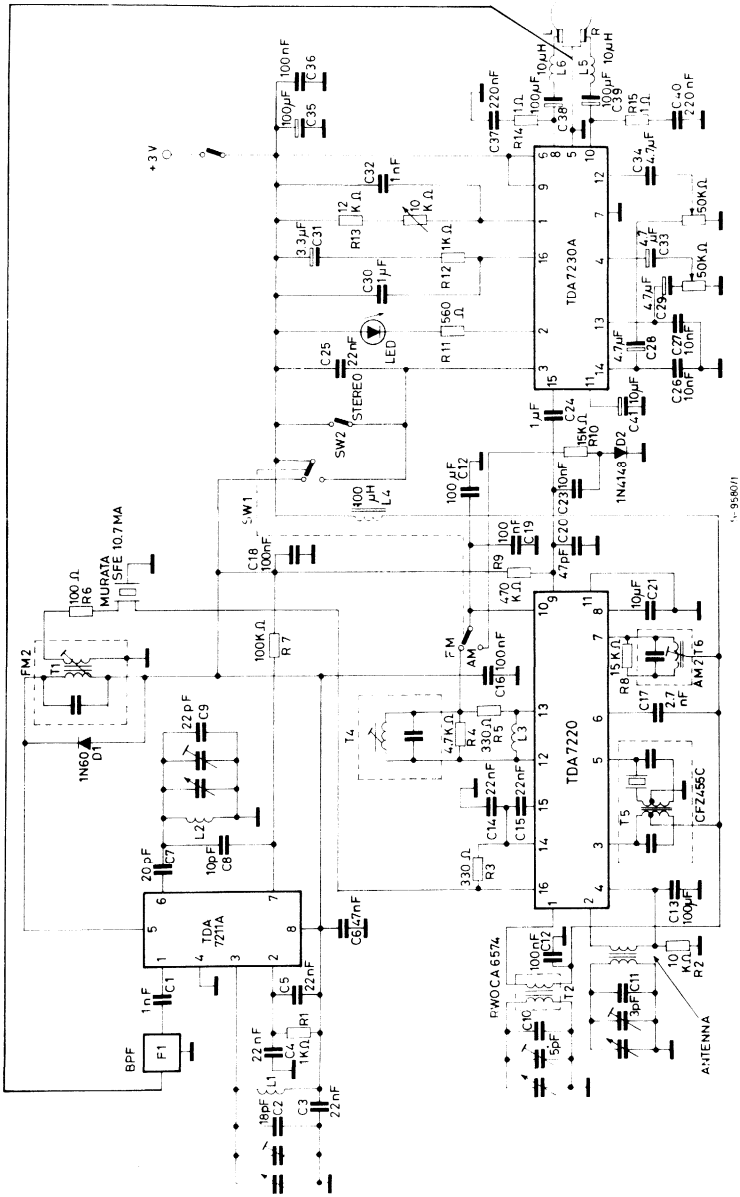


Fig. 17 - Drain current vs. supply voltage



APPLICATION INFORMATION

Fig. 18 - Stereo AM/FM miniradio



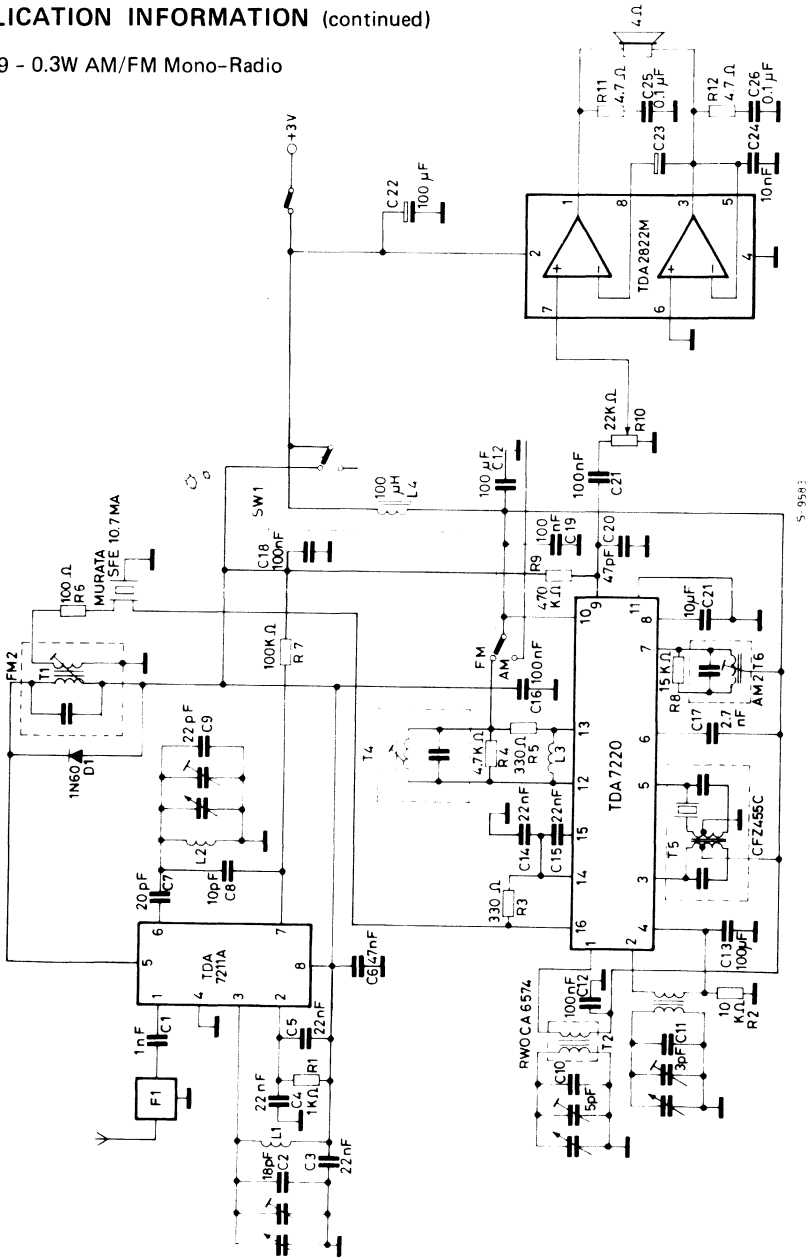
APPLICATION INFORMATION (continued)

Typical performance of the radio receiver of fig. 18 (V_s = 3V, R_L = 32Ω)

Parameter		Test Conditions		Value
WAVEBANDS	FM			87.5 to 108 MHz
	AM			510 to 1620 KHz
SENSITIVITY	FM	S/N = 26 dB	Δf = 22.5 KHz	3 μV
	AM	S/N = 6 dB	m = 0.3	2 μV
	AM	S/N = 26 dB	m = 0.3	10 μV
DISTORTION (fm = 1 KHz)	FM	P_o = 20 mW	Δf = 22.5 KHz	0.5%
			Δf = 75 KHz	1.8%
	AM	V_i = 100 μV	m = 0.8	1.1%
SIGNAL TO NOISE (fm = 1 KHz)	FM	P_o = 20 mW V_i = 100 μV	Δf = 22.5 KHz	60 dB
	AM	P_o = 20 mW V_i = 1 mV	m = 0.3	45 dB
AMPLITUDE MODULATION REJECTION	FM	V_i = 100 μV	Δf = 22.5 KHz m = 0.3	40 dB
QUIESCENT CURRENT				16 mA
SUPPLY VOLTAGE RANGE				1.6 to 3V

APPLICATION INFORMATION (continued)

Fig. 19 - 0.3W AM/FM Mono-Radio



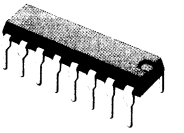
TDA7230A

ADVANCE DATA

STEREO DECODER AND HEADPHONE AMPLIFIER

- OPERATING SUPPLY VOLTAGE RANGE: 1.8 to 6V
- LED DRIVING FOR STEREO INDICATION
- STEREO/MONO SWITCH
- ONLY OSCILLATOR FREQUENCY ADJUSTMENT NECESSARY
- LOW DISTORTION AND LOW NOISE
- VERY LOW POP ON/OFF NOISE
- FEW EXTERNAL COMPONENTS
- SOFT CLIPPING

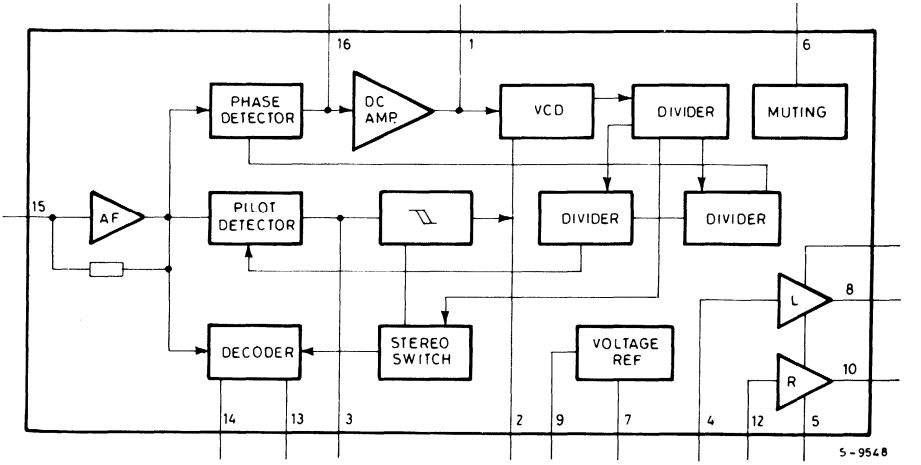
The TDA7230A is a monolithic integrated circuit in 16 pin plastic package designed for stereo decoder and headphone amplifier applications in portable radio.



DIP-16 Plastic (0.4)

ORDER CODE: TDA 7230A

BLOCK DIAGRAM

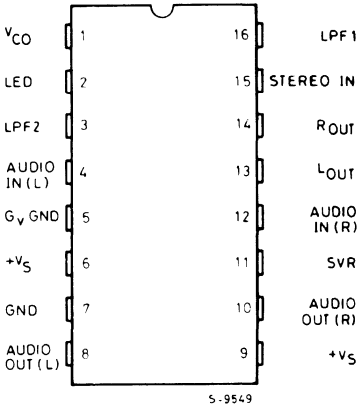


TDA7230A

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9	V
I_L	LED current	8	mA
I_O	Peak output current	200	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W

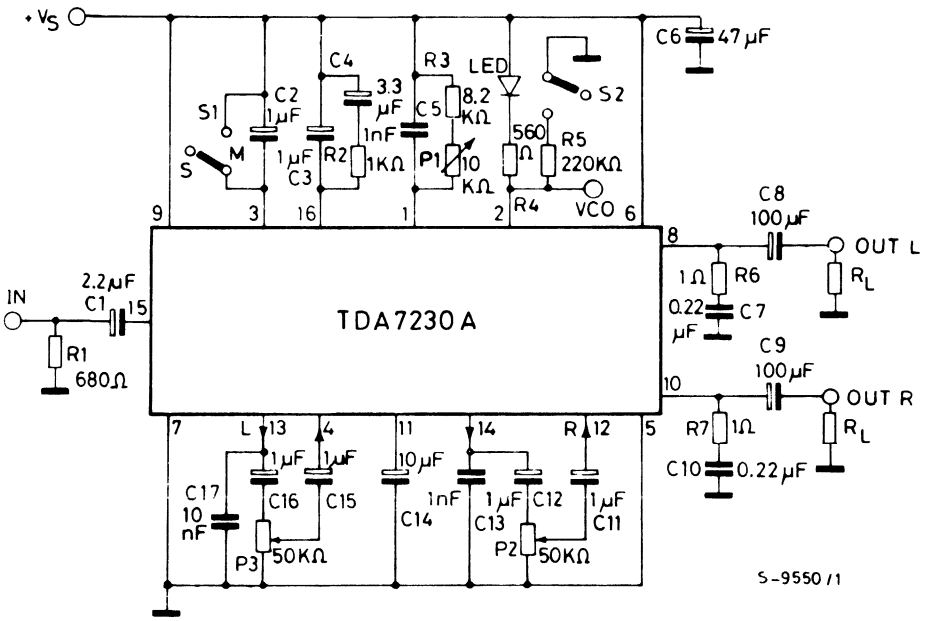
CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	max	80	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, T_{amb} = 25°C, V_s = 3V, f = 1KHz)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		1.8		6	V
I_s	Supply current	LED on		9.5		mA

AUDIO STEREO AMPLIFIER

P_o	Output power	V_s = 3V, R_L = 32Ω, d = 10% V_s = 3V, R_L = 16Ω, d = 10% V_s = 1.8V, R_L = 32Ω, d = 10%	27 45 6	30 48 7		mW mW mW
d	Distortion	P_o = 10 mW, f = 1 KHz, R_L = 32Ω		0.2	1	%

ELECTRICAL CHARACTERISTICS (continued)

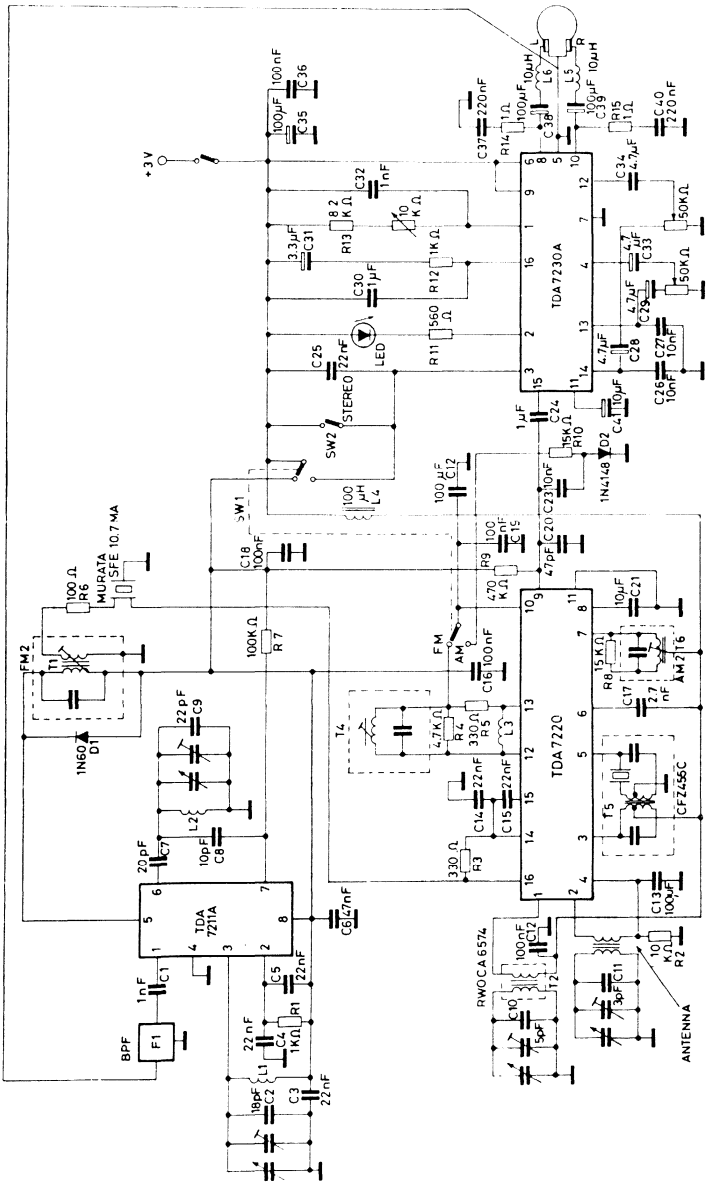
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
G_v	Voltage gain		28	30	32	dB
R_i	Input resistance		15	20		KΩ
	Cross talk	f = 1 KHz R_s = 10 KΩ	40			dB
SVR	Supply voltage rejection	C_{14} = 10μF, R_g = 10 KΩ, f = 100 Hz		40		dB
e_N	Total input noise voltage	R_G = 10 KΩ Bandwidth: 22 Hz - 22 KHz		2	5	μV

STEREO DECODER

R_i	Input resistance		6	10		KΩ
R_o	Output resistance			5		KΩ
V_i	Max. Input signal (composite)	L + R = 90% P = 10% f_m = 1 KHz THD = 5%	200			mVrms
S_c	Channel separation	L + R = 90 mVrms f_m = 1 KHz	25	35		dB
d	Total harmonic distortion (Out pin 13, pin 14)	Mono V_i = 100 mVrms Stereo L + R = 90 mVrms f_m = 1 KHz P = 10 mVrms		0.4 0.5	1 1	%
G_v	Voltage gain	V_i = 100 mVrms	-3		+3	dB
	Channel balance	V_i = 100 mVrms	-1	0	+1	dB
	LED on	Pilot input		8	11	mVrms
	LED off			6		mVrms
	LED Hysteresis	Turn OFF from Turn ON		3		mVrms
	Capture range	P = 10 mVrms		± 3		%
S/N	Carrier leak 19 KHz 38 KHz	P = 10 mVrms L + R = 90mVrms	-25 -40	-32 -48		dB dB
S/N	Signal to noise	V_i = 100 mVrms R_G = 600Ω		82		dB

TYPICAL APPLICATION

Fig. 1 - 3V stereo AM/FM mini-radio



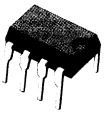
TDA7231

ADVANCE DATA

1.6W AUDIO AMPLIFIER

- OPERATING VOLTAGE 1.8 TO 15V
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION
- SOFT CLIPPING

The TDA7231 is a monolithic integrated circuit in 4+4 lead minidip package. It is intended for use as class AB power amplifier with wide range of supply voltage in portable radios, cassette recorders and players, etc.



Powerdip (4 + 4)

ORDERING NUMBER: TDA7231

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1.25	W
	at $T_{case} = 70°C$	4	W
I_o	Output peak current	1	A
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM

(Top view)

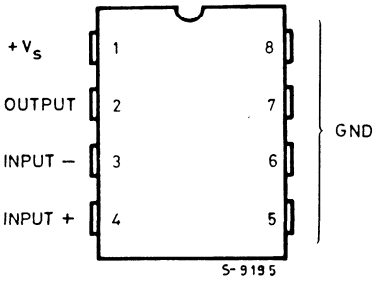


Fig. 1 - Test and application circuit

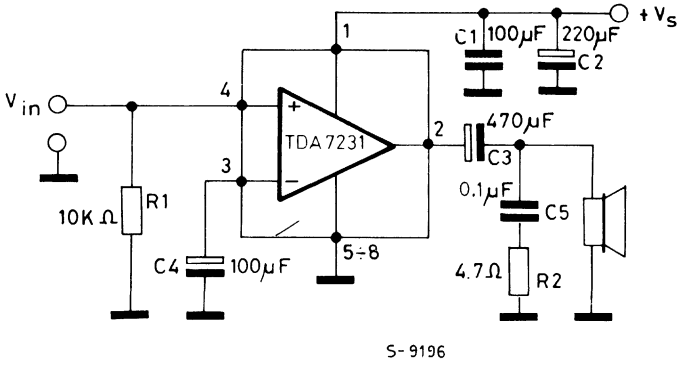
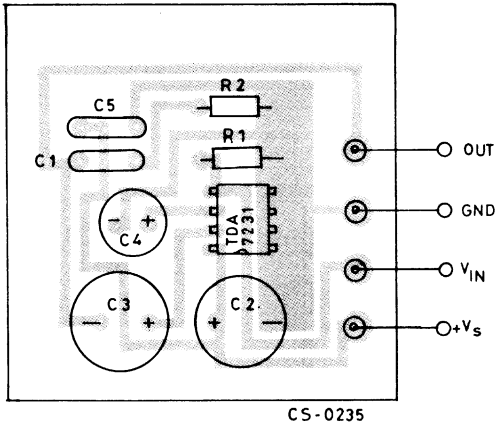


Fig. 2 - P.C. board and components layout



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance juction ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	15	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		1.8		15	V
Vo	Quiescent out voltage	V_s = 3V		2.7		V
				1.2		
I_d	Quiescent drain current			3.6	9	mA
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz				
		V_s = 12V R_L = 8Ω		2		W
		V_s = 9V R_L = 4Ω		1.6		W
		V_s = 6V R_L = 8Ω		0.4		W
		V_s = 6V R_L = 4Ω		0.7		W
		V_s = 3V R_L = 4Ω		110		mW
		V_s = 3V R_L = 8Ω		70		mW
d	Distortion	P_o = 0.2W R_L = 8Ω f = 1KHz		0.3		%
G_v	Closed loop voltage gain			38		dB
R_{in}	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_s = 10KΩ B = Curve A		2		μV
		B = 22Hz to 22KHz		3		
SVR	Supply voltage rejection		24	30		dB

Fig. 3 - Output power versus supply voltage

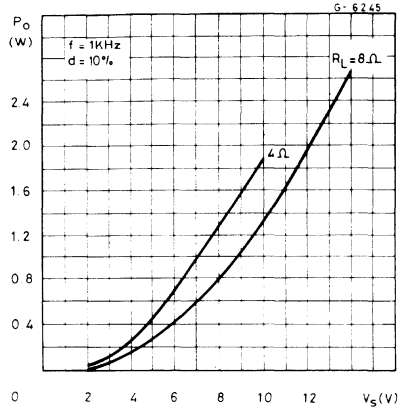


Fig. 4 - Quiescent current versus supply voltage

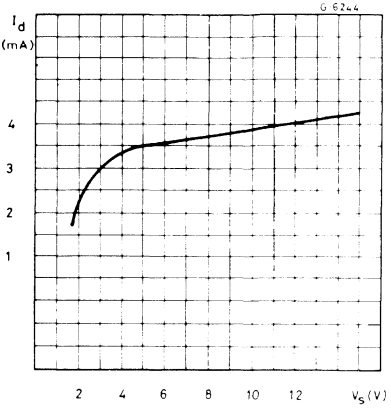


Fig. 5 - Quiescent output voltage versus supply voltage

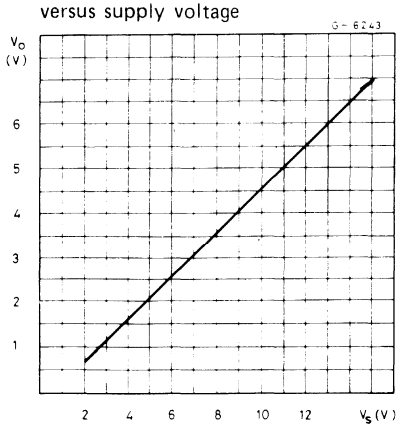
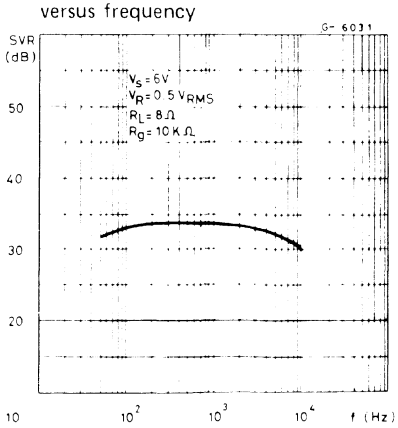


Fig. 6 - Supply voltage rejection versus frequency



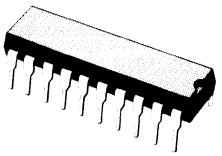
TDA7232

ADVANCE DATA

LOW NOISE PREAMPLIFIER COMPRESSOR

- SINGLE SUPPLY OPERATION (10 to 30V)
- HIGH SUPPLY VOLTAGE REJECTION
- COMPRESSOR FACILITY
- VERY LOW NOISE AND DISTORTION
- HIGH COMMON MODE REJECTION
- SHORT CIRCUIT PROTECTION

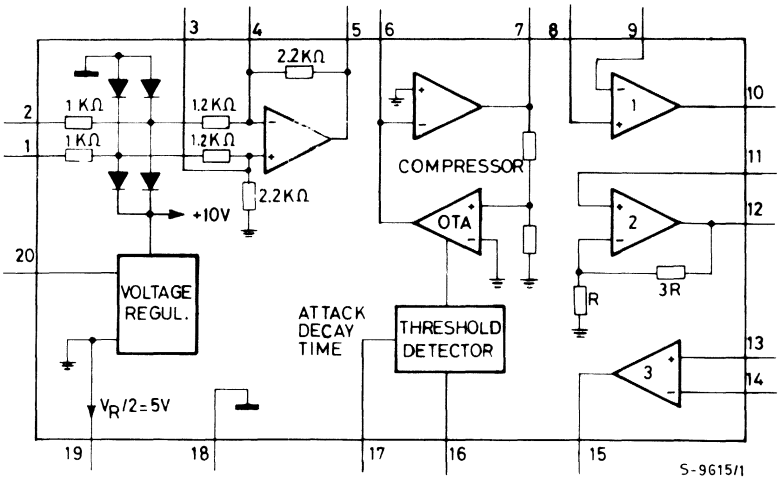
The TDA 7232 is a preamplifier mainly intended for car-radio applications, requiring very low noise and distortion performance.
It consists of a unity gain differential input amplifier with a very high common mode rejection, a compressor wich avoids the output clipping and three multipurpose operational amplifiers.
A high stability voltage regulator is also included.
The TDA 7232 is assembled in a 20 lead dual in line plastic package.



DIP-20 Plastic
(0.4)

ORDER CODE: TDA 7232

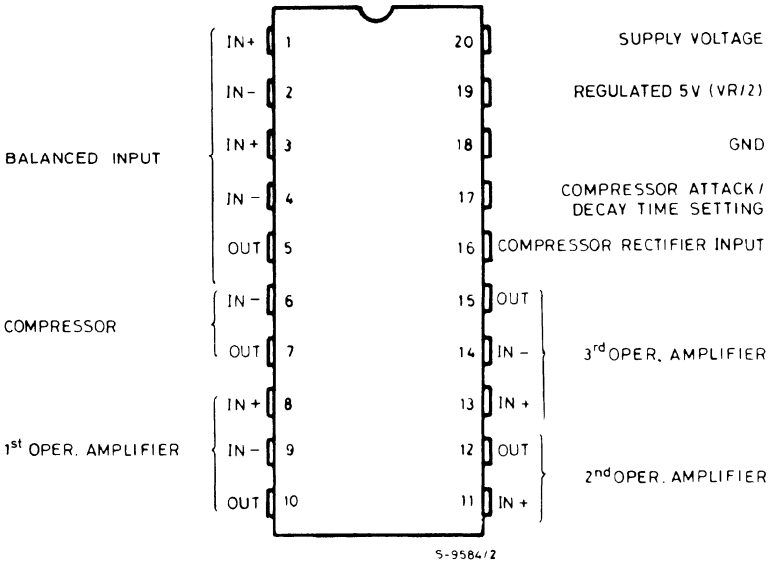
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	30	V
V_s	Peak supply voltage (for 50 ms)	40	V
V_i	Input voltage	$\pm V_s$	
T_{op}	Operating temperature	-25 to 85	°C
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	1	W

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s = 14.4V, G_v = 30 dB, refer to test circuit amplifier fig. 1)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		10		30	V
I_s	Supply current			10	16	mA
G_v	Closed loop gain	Pin 1-2 to pin 15	29	30	31	dB
d	Total harmonic distortion	f = 1 KHz out of compression V_o = 2 V_{RMS}		0.03	0.12	%
		in compression V_i = 0.7 V_{RMS}		0.15	0.5	%
V_o	Output volt. swing		7.5	8.4		V
e_N	Total output noise	B = 22 Hz to 22 KHz		160		μV
		R_g = 50Ω Curve A		120		μV
SVR	Supply volt. rejection (*)	R_g = 50Ω f = 100 Hz V_R = 1 V_{RMS}	90	110		dB

INPUT DIFFERENTIAL AMPLIFIER

V_{OS}	Input offset voltage			1	7	mV
G_v	Voltage gain	f = 20 Hz to 20 KHz	0.98	1	1.02	V/V
e_N	Total input noise voltage	R_g = 50Ω; B = 22 Hz to 22 KHz		1.5		μV
		R_g = 50Ω; curve A		1.1		μV
d	Distortion	R_L = 2 KΩ V_o = 1 V_{RMS} f = 1 KHz		0.01		%
V_o	Output swing	R_L = 2 KΩ	7.5	8.4		V_{pp}
SR	Slew rate			1		V/μS
CMR	Common mode reject.	f = 20 Hz to 20 KHz	36	50		dB

COMPRESSOR

I_b	Input bias current			60	300	nA
V_{os}	Input offset voltage	$R_g \leq$ 10 KΩ out of compression		1	3.5	mV
V_{os}	Output offset voltage	in compression $V_{pin.17}$= 0.7V			350	mV
e_N	Total input noise volt.	R_g = 50Ω; B = 22 Hz to 22 KHz		1.8		μV
		R_g = 50Ω; curve A		1.3		μV
d	Distortion	R_L = 2 KΩ V_o = 1 V_{RMS} f = 1 KHz G_v = 20 dB		0.01		%
SVR	Supply voltage rejection	V_R = 1V, f = 100 Hz, R_g = 50Ω	86			dB

(*) Referred to the input.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	DC output voltage swing	R_L = 2 KΩ	7.5	8.4		V
SR	Slew rate			0.7		V/μS

1st AND 3rd OPERATION AMPLIFIER

I_b	Input bias current			60	300	nA
I_{os}	Input offset current			20	50	nA
V_{os}	Input offset voltage	$R_g \leqslant$ 10 KΩ		1	3.5	mV
CMR	Common mode rejection		86			dB
SVR	Supply volt. rejection	V_R = 1V, f = 100 Hz, R_g = 50Ω	86			dB
e_N	Total inp. noise volt.	R_g = 50Ω; B = 22 Hz to 22 KHz		1.4		μV
		R_g = 50Ω; curve A		1.1		μV
V_o	Output volt. swing	R_L = 2 KΩ	7.5	8.4		V_{pp}
d	Total harmonic distortion	R_L = 2 KΩ, V_o = 1 V_{RMS}, f = 1 KHz, G_v = 20 dB		0.01		%
G_v	Open loop gain	R_L = 2 KΩ	86	100		dB
SR	Slew rate	R_L = 2 KΩ		1		V/μS

2nd OPERATIONAL AMPLIFIER (G_v = 12 dB internally set)

V_{os}	Output offset voltage			4	15	mV
SVR	Supply voltage rejection	V_R = 1V, f = 100 Hz	86			dB
e_N	Total input noise voltage	R_g = 50Ω; B = 22 Hz to 22 KHz		2.2		μV
		R_g = 50Ω; curve A		1.4		μV
V_o	DC output volt. swing	R_L = 2 KΩ	7.5	8.4		V
d	Total harmonic distortion	R_L = 2 KΩ, f = 1 KHz, V_o = 1 V_{RMS}		0.01		%
G_v	Voltage gain	f = 20 Hz to 20 KHz	11.5	12	12.5	dB
SR	Slew rate	R_L = 2 KΩ		1		V/μS

VOLTAGE REGULATOR

V_o	Output voltage	Pin 19, $I_{sink, source}$ from 0 to 12 mA	4.6	5	5.4	V
I_o	Output max. current	I_{source}		12		mA
		I_{sink}		12		mA

Fig. 1 - Test circuit

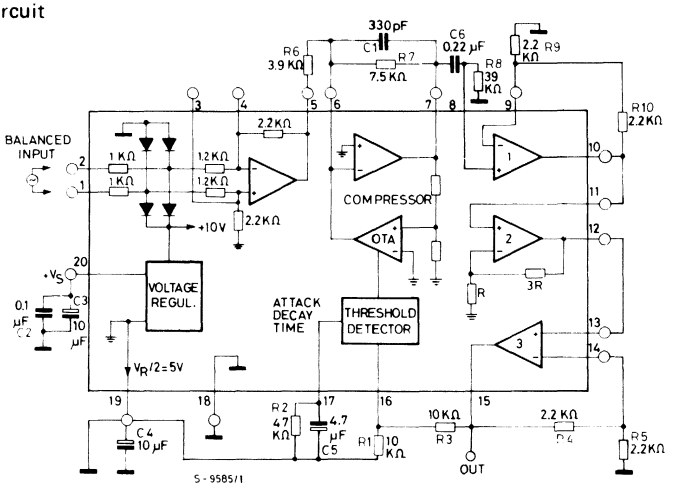


Fig. 2 - P.C. board and components layout of the test circuit of fig. 1 (1:1 scale)

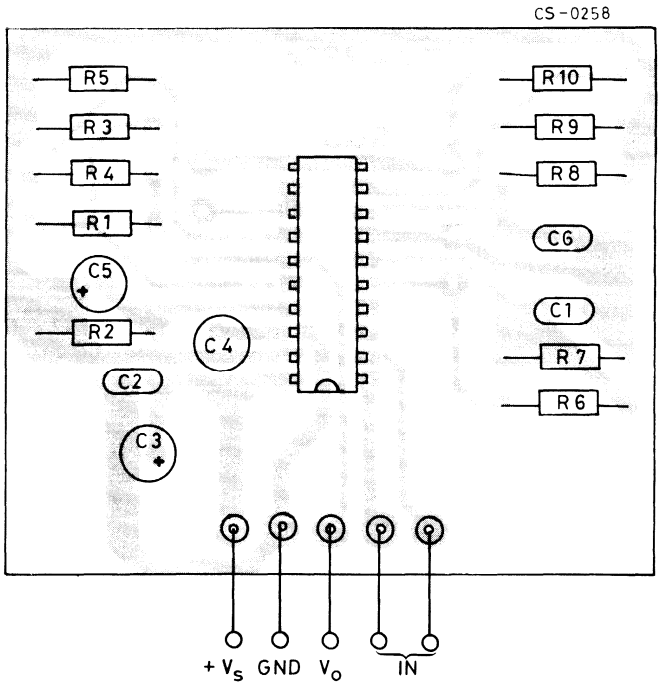


Fig. 3 - Supply current vs. supply voltage (complete test circuit)

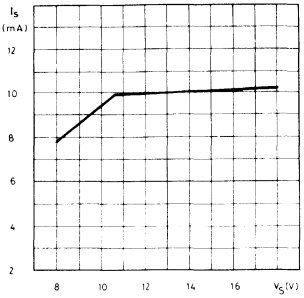


Fig. 4 - Compression characteristics

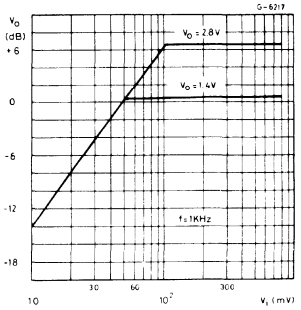


Fig. 5 - Distortion vs. frequency (complete test circuit)

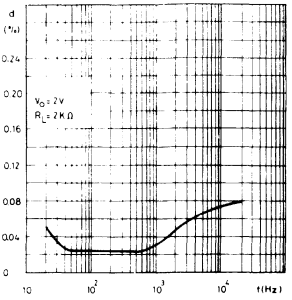


Fig. 6 - Distortion vs. input signal level (complete test circuit)

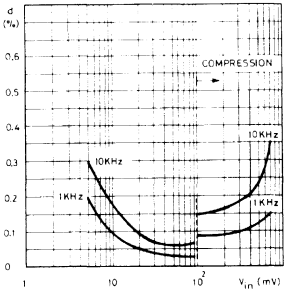


Fig. 7 - Supply voltage rejection vs. frequency (complete test circuit)

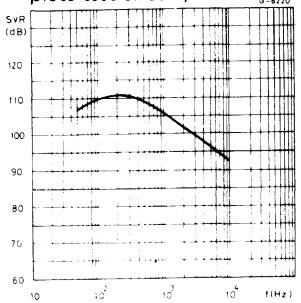


Fig. 8 - Distortion vs. output voltage (input differ. amplifier)

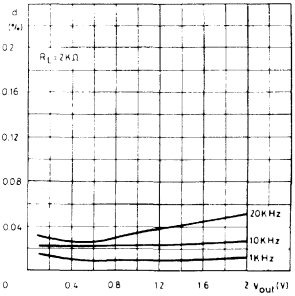


Fig. 9 - Distortion vs. frequency (input differ. amplifier)

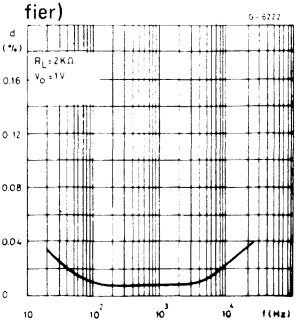
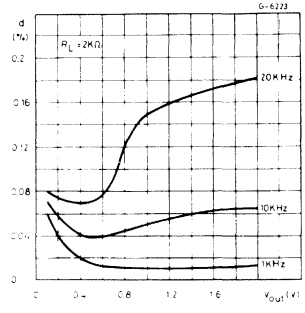


Fig. 10 - Distortion vs. output voltage (compressor)



Fi. 11 - Distortion vs. frequency (compressor)

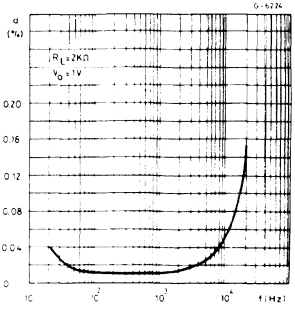


Fig. 12 - Distortion vs. output voltage (Op. Amp. 1&3)

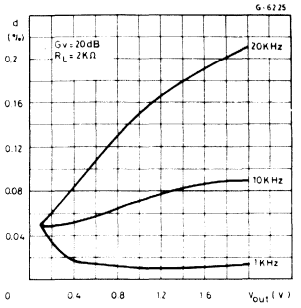


Fig. 13 - Distortion vs. frequency (Op. Amp. 1 & 3)

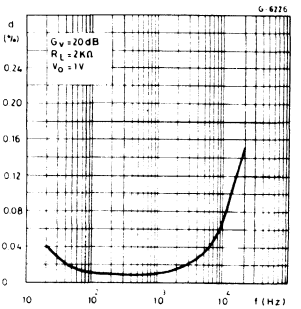


Fig. 14 - Open loop frequency and phase response (Op. Amp. 1 & 3)

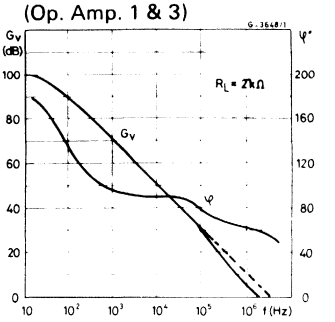


Fig. 15 - Distortion vs. output voltage (Op. Amp. 2)

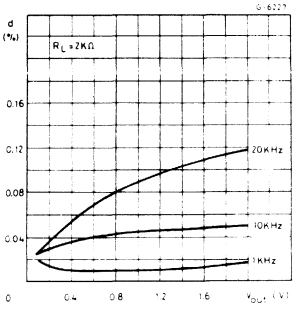
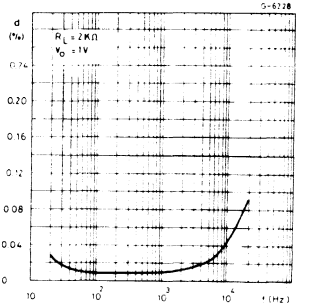


Fig. 16 - Distortion vs. frequency (Op. Amp. 2)



APPLICATION INFORMATION

The devices TDA 7232 and TDA 7260 realize with four external POWER MOS an exclusive audio system for car radio, thanks to their unique features as:

- 25W output power (d = 0.3%) without heatsink, thanks to the extra-high efficiency (85% typ. at rated output power) of the power stage, which operates in class "D" (pulse width modulation).
- In-car frequency response compensation, thanks to the availability of several operational amplifiers for the necessary equalization.
- High-quality sound at all listening levels, thanks to an appropriate compressor circuit that avoids clipping in the system.
- Low distortion, low noise, fully protected operation of the whole system.

Fig. 17 - Suggested application using the TDA 7260 audio PWM amplifier

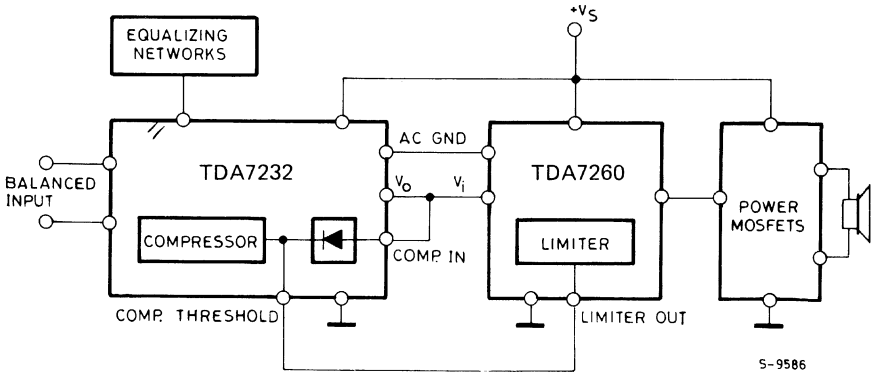
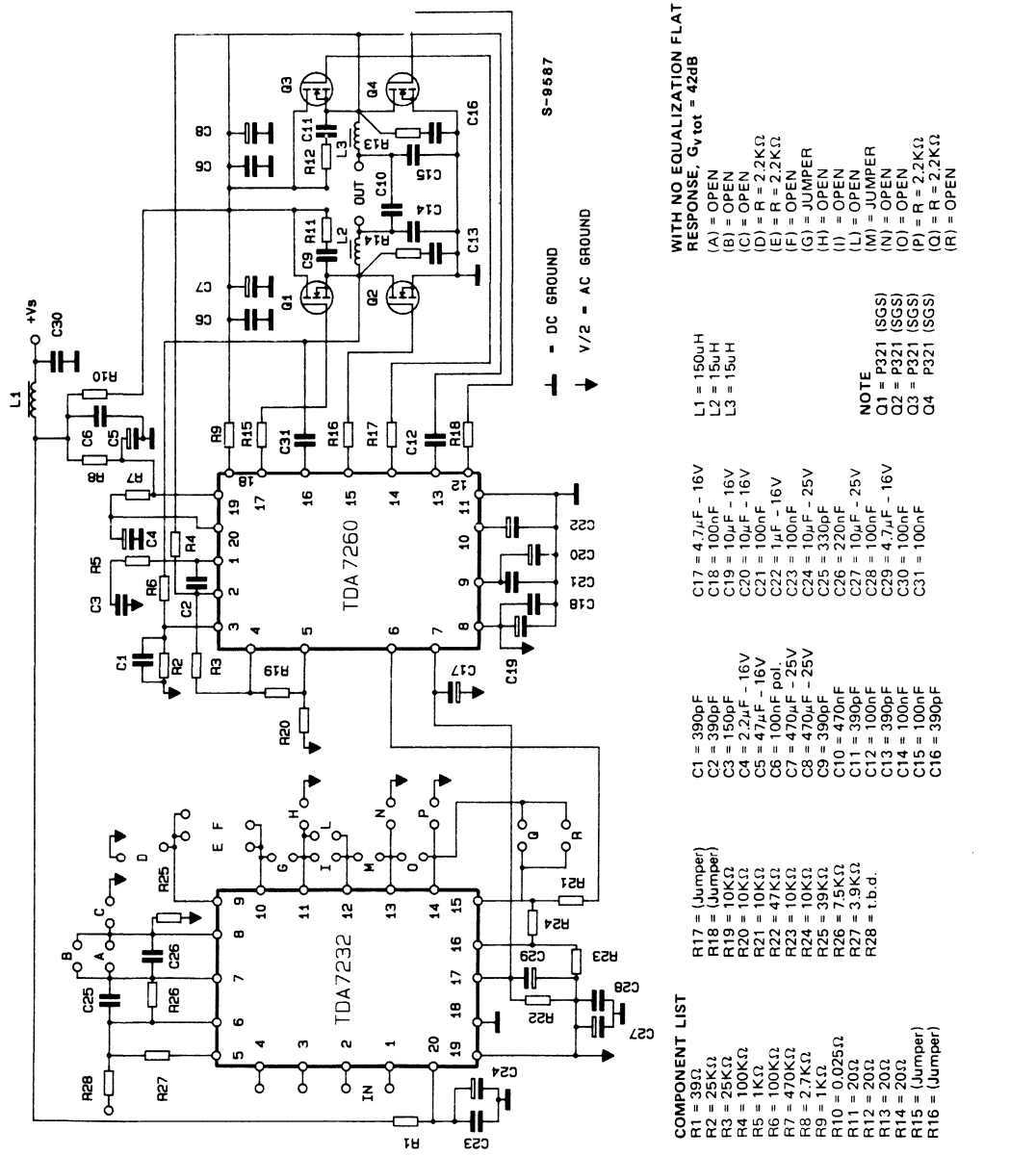


Fig. 18 - 25W application circuit using the TDA7260 audio PWM



COMPONENT LIST

R1 = 39Ω	R17 = (Jumper)	C1 = 390pF	C17 = 4.7μF - 16V
R2 = 25KΩ	R18 = (Jumper)	C2 = 390pF	C18 = 100nF
R3 = 25KΩ	R19 = 10KΩ	C3 = 150pF	C19 = 10μF - 16V
R4 = 100KΩ	R20 = 10KΩ	C4 = 2.2μF - 16V	C20 = 10μF - 16V
R5 = 1KΩ	R21 = 10KΩ	C5 = 47μF - 16V	C21 = 100nF
R6 = 100KΩ	R22 = 47KΩ	C6 = 100nF pol.	C22 = 1μF - 16V
R7 = 470KΩ	R23 = 10KΩ	C7 = 470μF - 25V	C23 = 100nF
R8 = 2.7KΩ	R24 = 10KΩ	C8 = 470μF - 25V	C24 = 10μF - 25V
R9 = 1KΩ	R25 = 39KΩ	C9 = 390pF	C25 = 330pF
R10 = 0.025Ω	R26 = 7.5KΩ	C10 = 470nF	C26 = 220nF
R11 = 20Ω	R27 = 3.9KΩ	C11 = 390pF	C27 = 10μF - 25V
R12 = 20Ω	R28 = t.b.d.	C12 = 100nF	C28 = 100nF
R13 = 20Ω		C13 = 390pF	C29 = 4.7μF - 16V
R14 = 20Ω		C14 = 100nF	C30 = 100nF
R15 = (Jumper)		C15 = 100nF	C31 = 100nF
R16 = (Jumper)		C16 = 390pF	

Fig. 19 - P.C. board and components layout of the circuit of fig. 18 (1 : 1 scale)

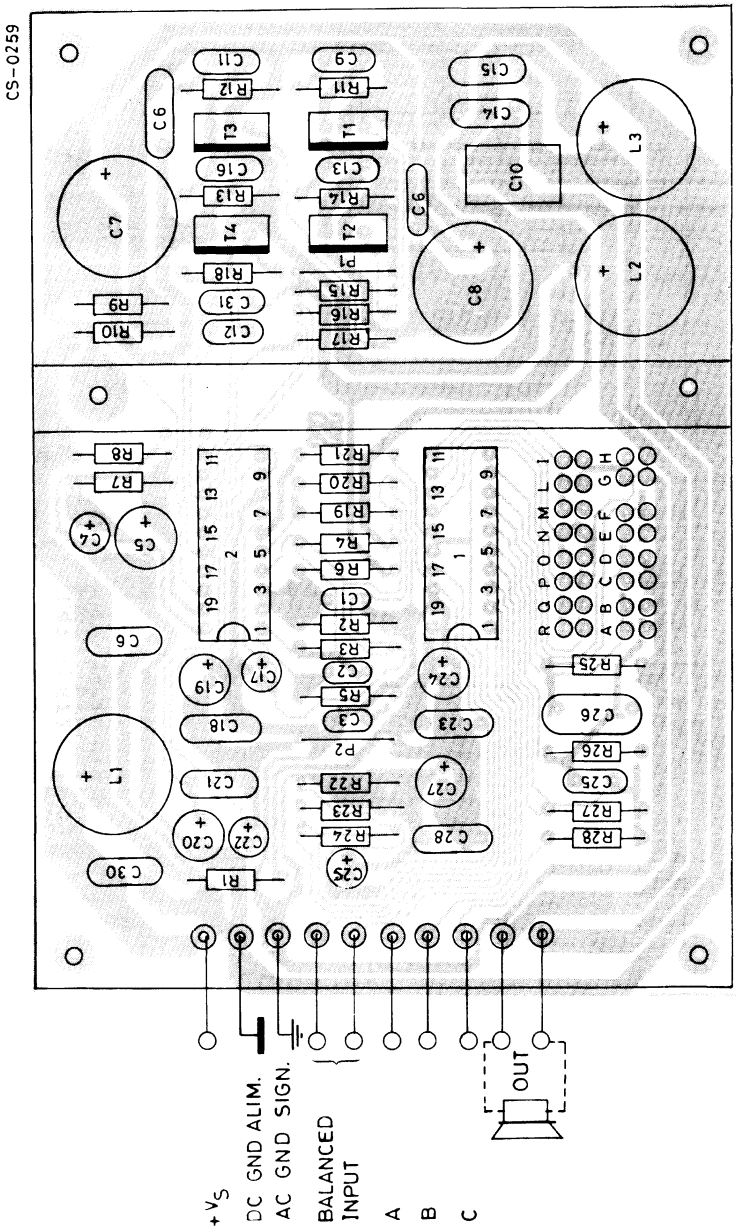


Fig. 20 - Five bands equalizer with compression indicator

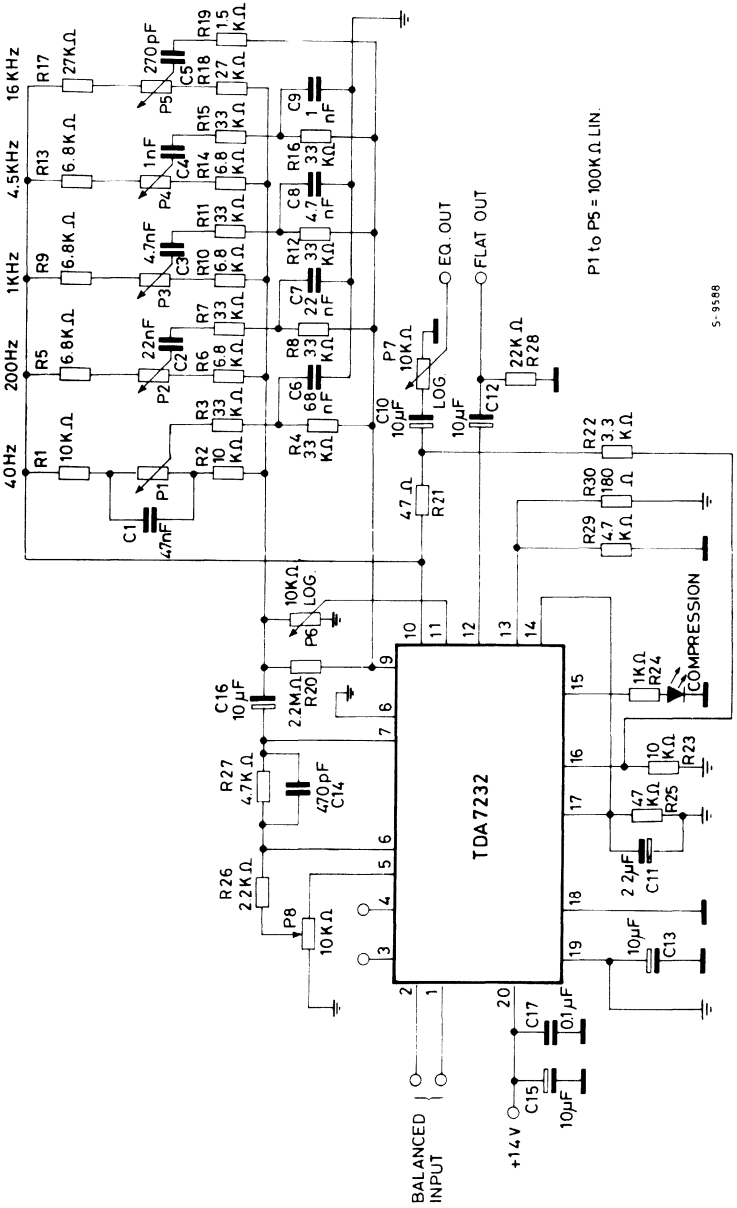


Fig. 21 - P.C. and components layout of the circuit of Fig. 20 (1 : 1 scale)

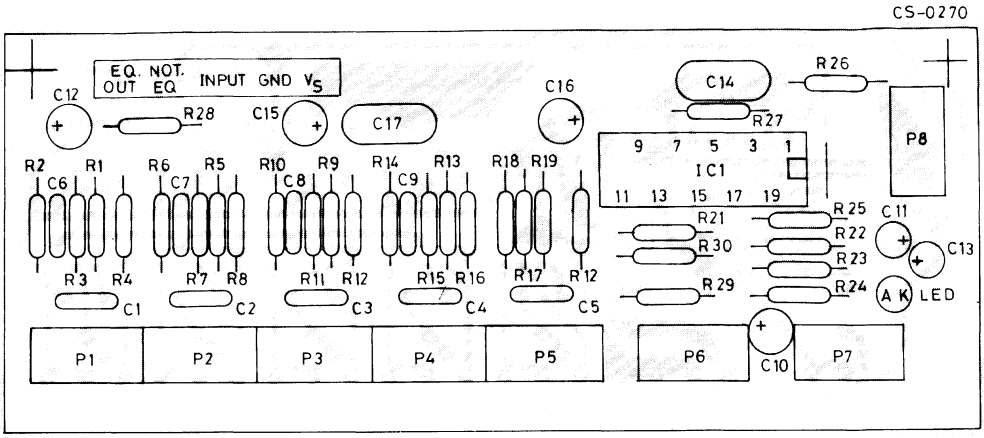
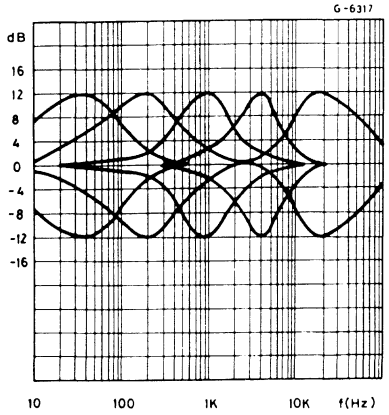


Fig. 22 - Frequency response of the five bands equalizer circuit



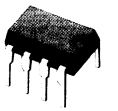
TDA7233

ADVANCE DATA

1W AUDIO AMPLIFIER WITH MUTE

- OPERATING VOLTAGE 1.8 TO 15V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION

The TDA7233 is a monolithic integrated circuit in 8 pin Minidip or SO-8 package, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable radios, cassette recorders and players.



Minidip Plastic

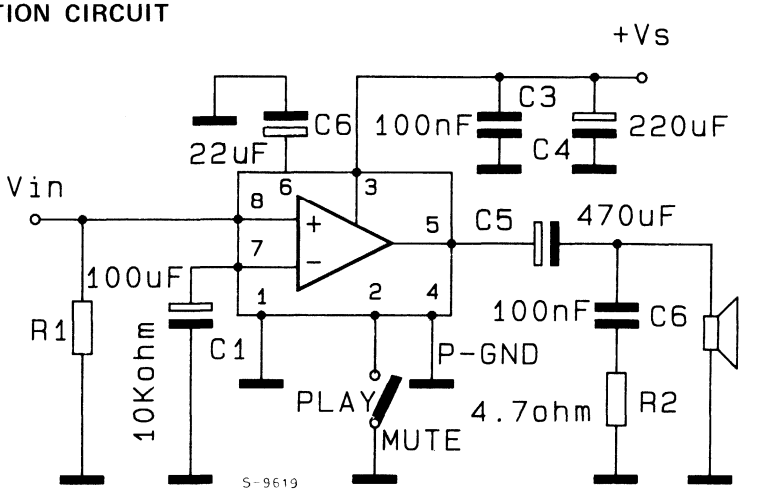
SO-8

ORDERING NUMBER: TDA7233 (Minidip)
TDA7233D (SO-8)

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output peak current	1	A
P_{tot}	Total power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT



CONNECTION DIAGRAM
(Top view)

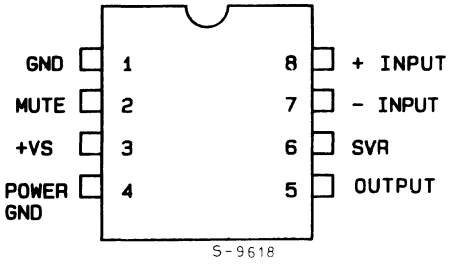
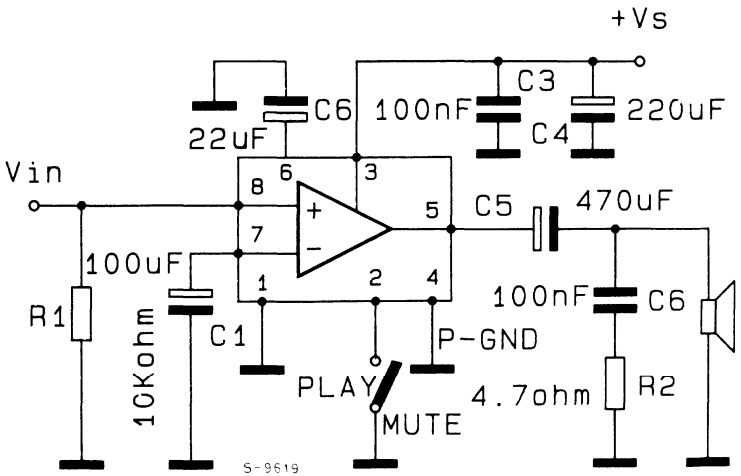


Fig. 1 - Test and application circuit



THERMAL DATA			SO-8	Minidip
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	100°C/W

ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise speficied)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		1.8		15	V
V_o	Quiescent out voltage			2.7		V
		V_s = 3V V_s = 9V		1.2 4.2		V V
I_d	Quiescent drain current	MUTE HIGH		3.6	9	mA
		MUTE LOW		0.4		
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz V_s = 12V R_L = 8Ω V_s = 9V R_L = 4Ω V_s = 9V R_L = 8Ω V_s = 6V R_L = 8Ω V_s = 6V R_L = 4Ω V_s = 3V R_L = 4Ω V_s = 3V R_L = 8Ω		 1.9 1.6 1 0.4 0 7 110 70		 W W W W W mW mW
d	Distribution	P_o = 0.5W R_L = 8Ω f = 1KHz V_s = 9V		0.3		%
G_v	Closed loop voltage gain			39		dB
R_{IN}	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise (R_s = 10KΩ)	B = Curve A		2		μV
		B = 22Hz to 22KHz		3		
SVR	Supply voltage rejection	f = 100Hz		45		dB
	MUTE attenuation	V_o = 1V f = 100Hz to 10KHz		70		dB
	MUTE threshold			0.6		V
I_M	MUTE current			0.4		mA

Fig. 2 - Output power vs. supply voltage

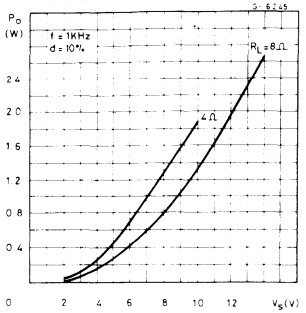


Fig. 3 - Supply voltage rejection vs. frequency

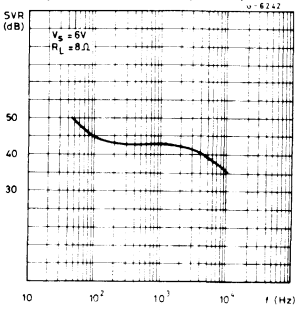


Fig. 4 - DC output voltage vs. supply voltage

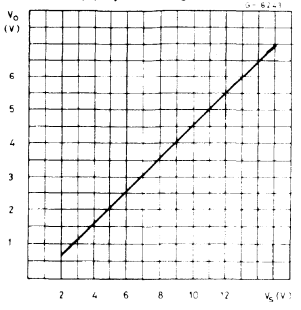


Fig. 5 - Quiescent current vs. supply voltage

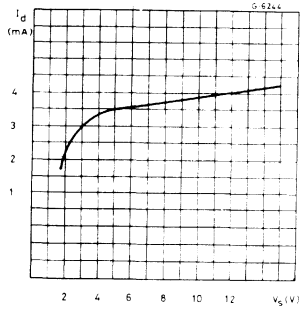
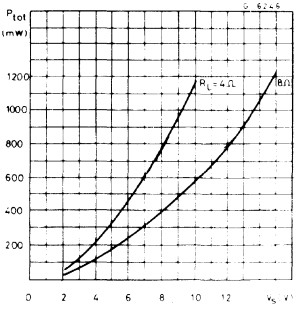


Fig. 6 - Total dissipated power vs. supply voltage



TDA7236

ADVANCE DATA

VERY LOW VOLTAGE AUDIO BRIDGE

The TDA7236 is a monolithic bridge audio amplifier in minidip and SO-8 package intended for use as audio power amplifier in telephone sets, mono radio receivers, etc. . Its main features are: minimum working supply voltage of 0.9V and low quiescent current.

Minidip Plastic

SO-8

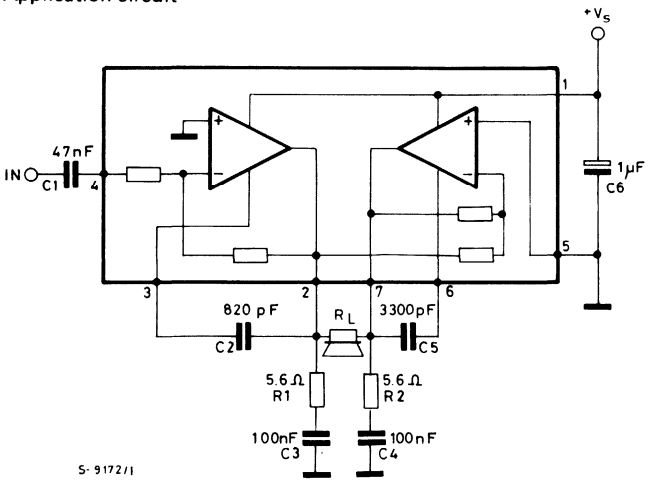
ORDERING NUMBER :

TDA7236 TDA7236D

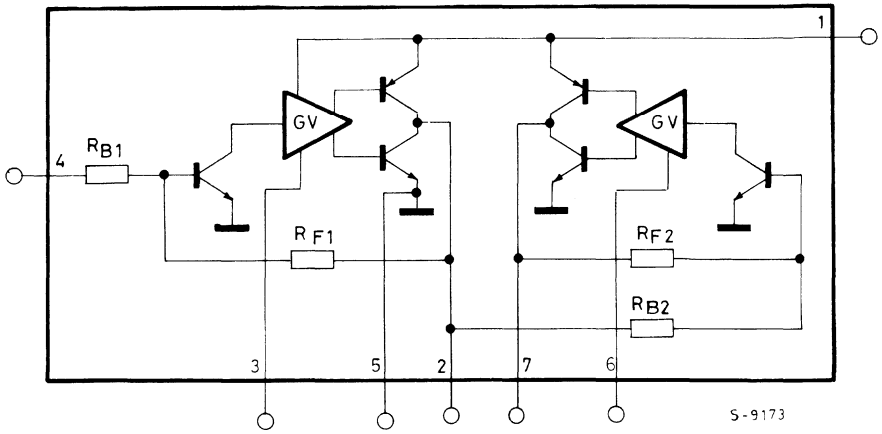
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	1.8	V
I_o	Output power current	50	mA
P_{tot}	Total power dissipation at T_{amb} = 50°C (Minidip)	0.5	W
T_{stg}, T_j	Storage and junction temperature	150	°C

Fig. 1 - Test and Application circuit

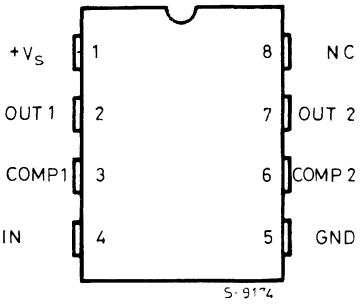


SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit V_s = 1.25V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltagerange		0.9		1.6	V
V_o	Quiescent output voltage			0.62		V
I_d	Total quiescent drain current			1	3	mA
G_v	Voltage gain			31		dB
R_i	Input resistance			10		KΩ
P_o	Output power	R_L = 32Ω; f = 1KHz; d = 5%	12	16		mW
d	Distortion	R_L = 32Ω; f = 1KHz; P_o = 5mW		1		%
B	Bandwidth		200Hz to 10KHz			
e_N	Total input noise voltage (curve A)			2		μV
V_{os}	Output DC offset			30		mV

Fig. 2 - Output power vs. supply voltage

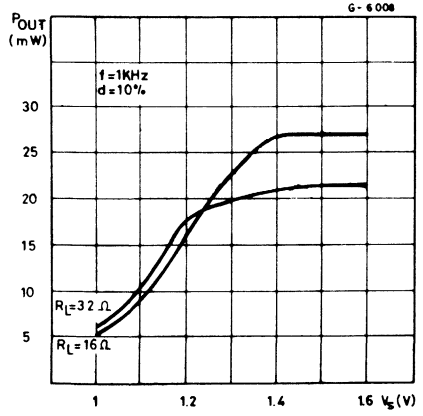


Fig. 3 - Drain current vs. supply voltage referred to Fig. 2

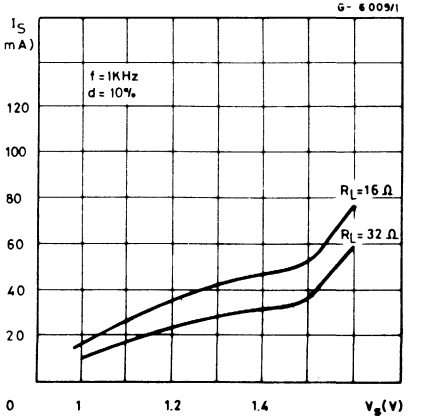
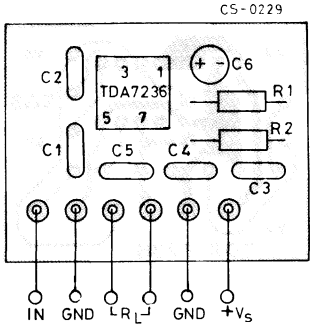
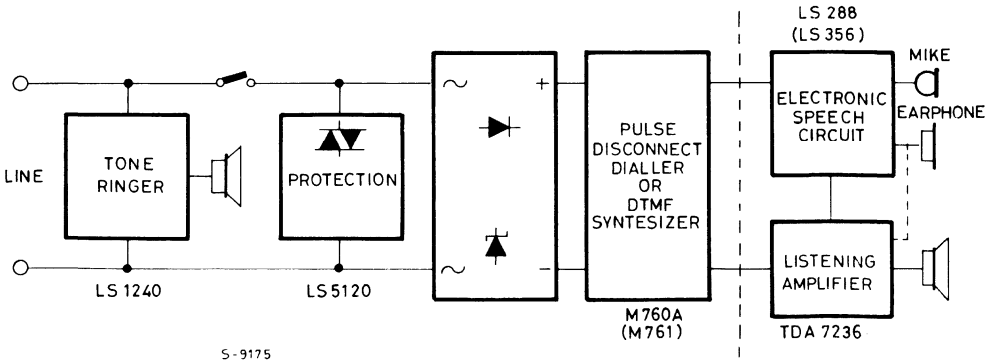


Fig. 4 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)



TYPICAL APPLICATION CIRCUIT

Fig. 5 - Telephone listening amplifier



TDA7240A

ADVANCE DATA

20W BRIDGE AMPLIFIER FOR CAR RADIO

- COMPACT HEPTAWATT PACKAGE
- FEW EXTERNAL COMPONENTS
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- DUMP TRANSIENT AND REVERSE POLARITY PROTECTION
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION / LOW NOISE

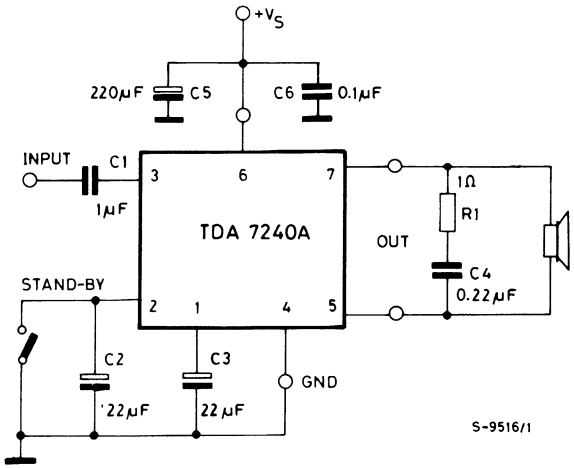
The TDA7240A is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7240A occupies little space on the printed circuit board.

Reliable operation is guaranteed by a comprehensive array of on-chip protection features. These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, polarity reversal, and junction overtemperature. Additionally, the TDA7240A protects the loudspeaker when one output is short-circuited to ground.

Heptawatt

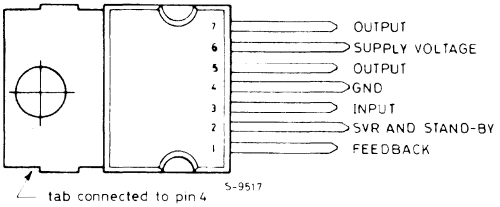
ORDERING NUMBER: TDA7240A

TYPICAL APPLICATION CIRCUIT



TDA7240A

CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Peak output current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Peak output current (repetitive f $\geqslant$ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 70°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

(*) Internally limited

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the circuit of Fig. 1, T_{amb} = 25°C, R_{th} (heatsink) = 4°C/W, V_s = 14.4V)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		18	V
V_{os}	Output offset voltage					150	mV
I_d	Total quiescent current	R_L = 4Ω			65	120	mA
P_o	Output power	f = 1KHz	R_L = 4Ω	16	20		W
		d = 10%	R_L = 8Ω	10	12		
d	Distortion	R_L = 4Ω f = 1KHz P_o = 50mW to 12W			0.1	0.5	%
		R_L = 8Ω f = 1KHz P_o = 50mW to 6W			0.05	0.5	
G_v	Voltage gain	f = 1KHz		39.5	40	40.5	dB
SVR	Supply voltage rejection	f = 100Hz		35	40		dB
E_n	Total input noise	(*)	R_s = 10KΩ		2	4	μV
		(**)			3		
η_l	Efficiency	R_L = 4Ω f = 1KHz P_o = 20W			65		%
I_{sb}	Stand-by current				200		μA
R_i	Input resistance	f = 1KHz		70			KΩ
V_i	Input sensitivity	f = 1KHz P_o = 2W	R_L = 4Ω		28		mV
f_L	Low frequency roll off (-3dB)	P_o = 15W	R_L = 4Ω			30	Hz
f_H	High frequency roll off (-3dB)	P_o = 15W	R_L = 4Ω	25			KHz
A_s	Stand-by attenuation	V_o = 2V_{rms}		70	90		dB
$V_{TH\ (pin\ 2)}$	Stand-by threshold					1	V

Bandwidth (*) B = Curve A (**) B = 22Hz to 22KHz

Fig. 1 - Test and application circuit

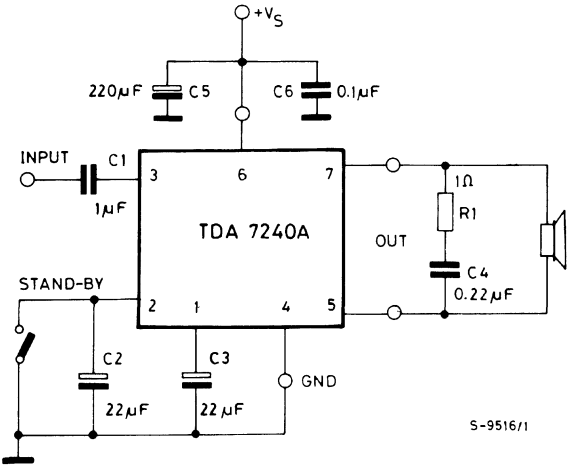
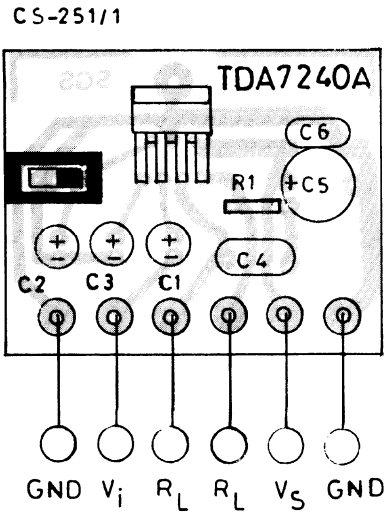


Fig. 2 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of Fig. 1. Different values can be used, the following table can help the designer.

Component	Recommended Value	Purpose	Larger than	Smaller than
R1	1Ω	Frequency stability.	Danger of high frequency oscillation.	
C1	1μF	Input DC decoupling.	Higher turn 'ON' and stand-by delay.	Higher turn 'ON' pop. Higher low frequency cutoff.
C2	22μF	Ripple rejection.	Increase of SVR. Increase of the turn 'ON' delay.	Degradation of SVR.
C3	22μF	Feedback low frequency cutoff		Higher low frequency cutoff
C4	0.22μF	Frequency stability.		Danger of oscillation.
C5	220μF	Supply filter.		Danger of oscillation.
C6	0.1μF	Supply by pass.		Danger of oscillation.

Fig. 3 - Output power vs. supply voltage

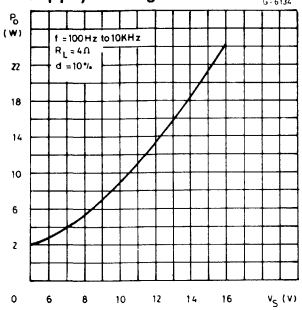


Fig. 4 - Distortion vs. output power

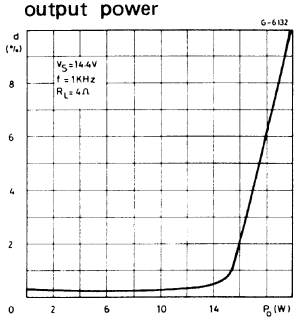


Fig. 5 - Output power vs. supply voltage

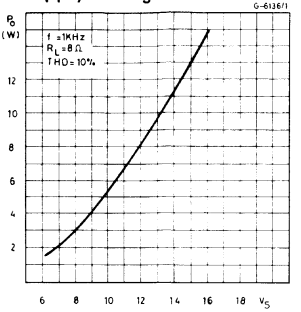


Fig. 6 - Distortion vs. output power

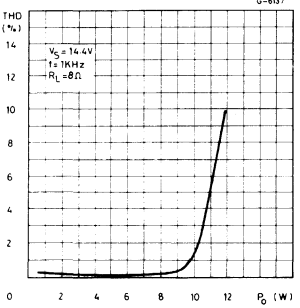


Fig. 7 - Distortion vs. frequency

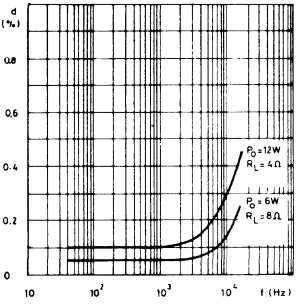


Fig. 8 - Supply voltage rejection vs. frequency

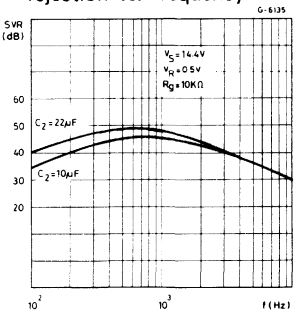


Fig. 9 - Output offset voltage vs. supply voltage

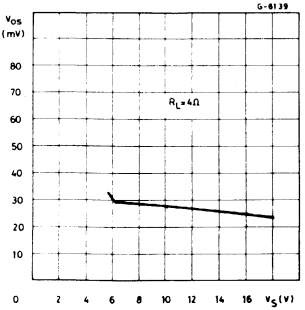


Fig. 10 - Power dissipation and efficiency vs. output power

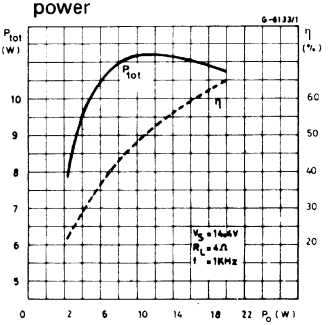


Fig. 11 - Power dissipation and efficiency vs. output power

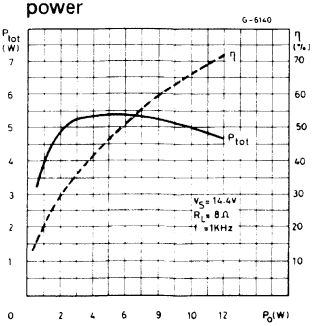
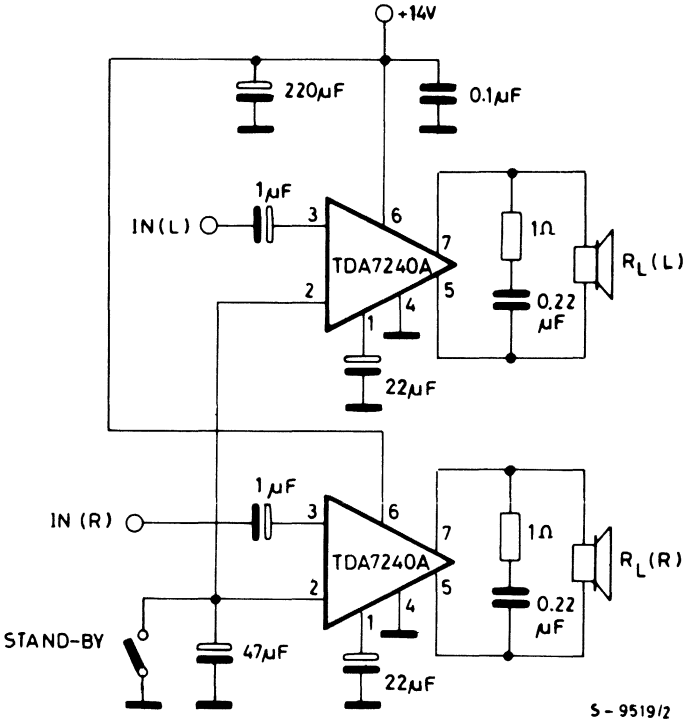


Fig. 12 - 20 + 20W Stereo amplifier for car-radio



TDA7241

ADVANCE DATA

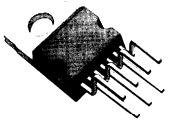
20W BRIDGE AMPLIFIER FOR CAR RADIO

- VERY LOW STAND-BY CURRENT
- GAIN = 26dB
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- COMPACT HEPTAWATT PACKAGE
- DUMP TRANSIENT AND REVERSE POLARITY PROTECTION
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION / LOW NOISE

The TDA7241 is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7241 occupies little space on the printed circuit board.

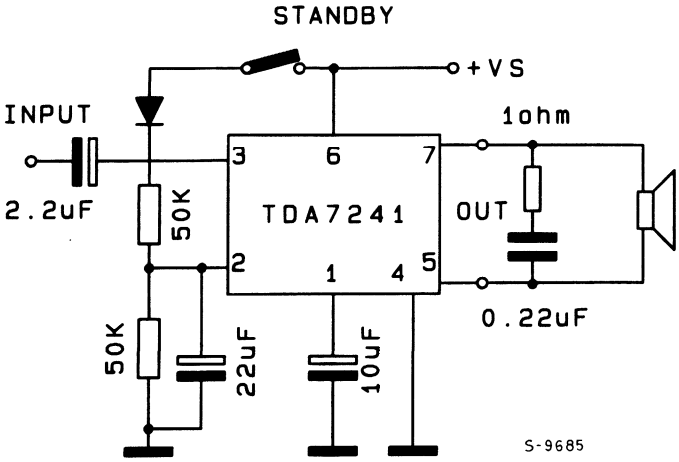
Reliable operation is guaranteed by a comprehensive array of on-chip protection features.

These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, polarity reversal, and junction overtemperature. Additionally, the TDA7241 protects the loudspeaker when one output is short-circuited to ground.



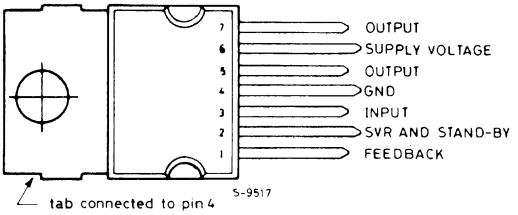
Heptawatt

ORDERING NUMBER: TDA 7241



TDA7241

CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Peak output current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Peak output current (repetitive f $\geqslant$ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 70°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

(*) Internally limited

THERMAL DATA

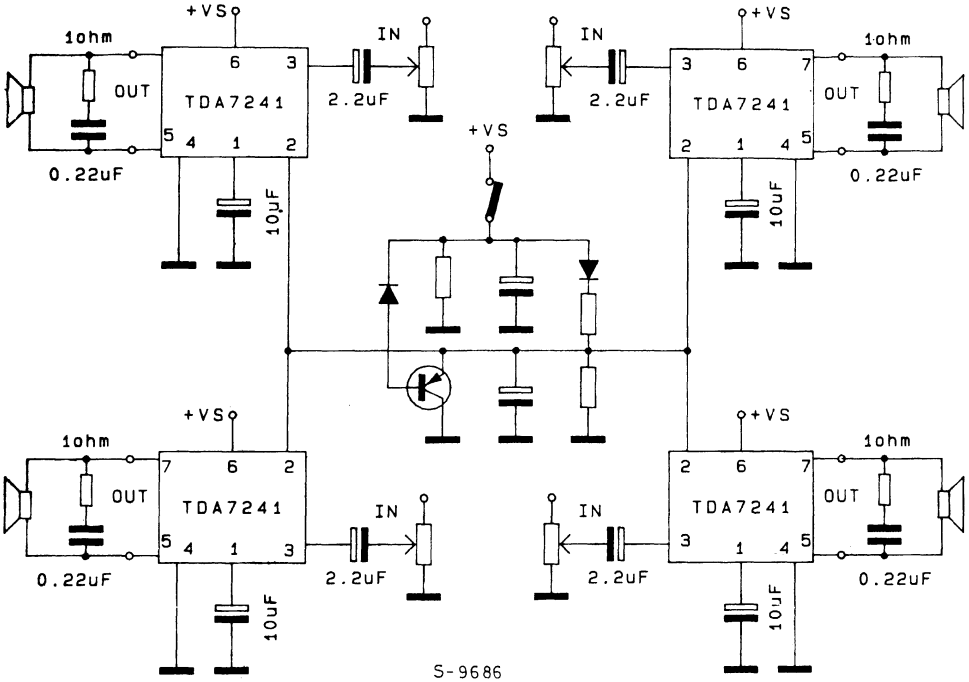
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the circuit of Fig. 1, T_{amb} = 25°C, R_{th} (heatsink)= 4°C/W, V_s = 14.4V)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		18	V
V_{os}	Output offset voltage					150	mV
I_d	Total quiescent current	R_L = 4Ω			65	120	mA
P_o	Output power	f = 1 KHz d = 10%	R_L = 4Ω	18	20		W
			R_L = 8Ω	10	12		
d	Distortion	R_L = 4Ω P_o = 50 mW to 12W	f = 1 KHz		0.1	0.5	%
		R_L = 8Ω P_o = 50 mW to 6W	f = 1 KHz		0.05	0.5	
G_v	Voltage gain	f = 1 KHz			26		dB
SVR	Supply voltage rejection	f = 100 Hz		45	52		dB
E_n	Total input noise	(*)	R_s = 10 KΩ		2	4	μV
		(**)			3		
η	Efficiency	R_L = 4Ω P_o = 20W	f = 1 KHz		65		%
I_{sb}	Stand-by current				1		μA
R_i	Input resistance	f = 1 KHz		70			KΩ
V_i	Input sensitivity	f = 1 KHz P_o = 2W	R_L = 4Ω		140		mV
f_L	Low frequency roll off (-3 dB)	P_o = 15W	R_L = 4Ω			30	Hz
f_H	High frequency roll off (-3 dB)	P_o = 15W	R_L = 4Ω	25			KHz
A_s	Stand-by attenuation	V_o = 2 V_{rms}		70	90		dB
V_{TH}(pin. 2)	Stand-by threshold					1	V

Bandwidth (*) B = Curve A (**) B = 22 Hz to 22 KHz

Fig. 1 - Application circuit: 4x20 W - Amplifier



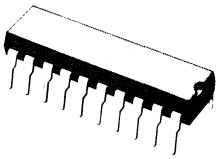
TDA7250

ADVANCE DATA

60W HI-FI DUAL AUDIO DRIVER

- WIDE SUPPLY VOLTAGE RANGE: 20 TO 90V (± 10 TO ± 45V)
- VERY LOW DISTORTION
- AUTOMATIC QUIESCENT CURRENT CONTROL FOR THE POWER TRANSISTORS WITHOUT TEMPERATURE SENSE ELEMENTS
- OVERLOAD CURRENT PROTECTION FOR THE POWER TRANSISTORS
- MUTE/STAND-BY FUNCTIONS
- LOW POWER CONSUMPTION
- OUTPUT POWER 60W/8Ω AND 100W/4Ω

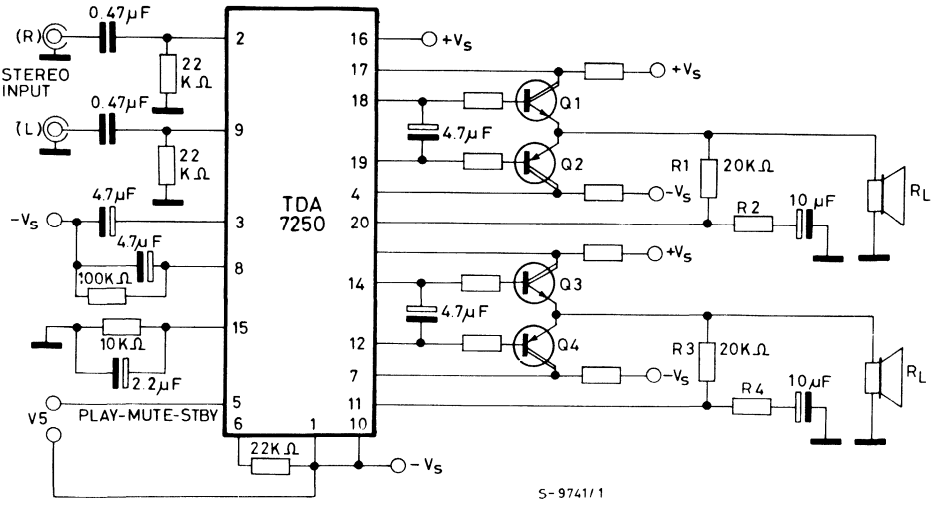
The TDA7250 stereo audio driver is designed to drive two pair of complementary output transistor in the Hi-Fi power amplifiers.



DIP-20 Plastic
(0.4)

ORDERING NUMBER: TDA7250

APPLICATION CIRCUIT

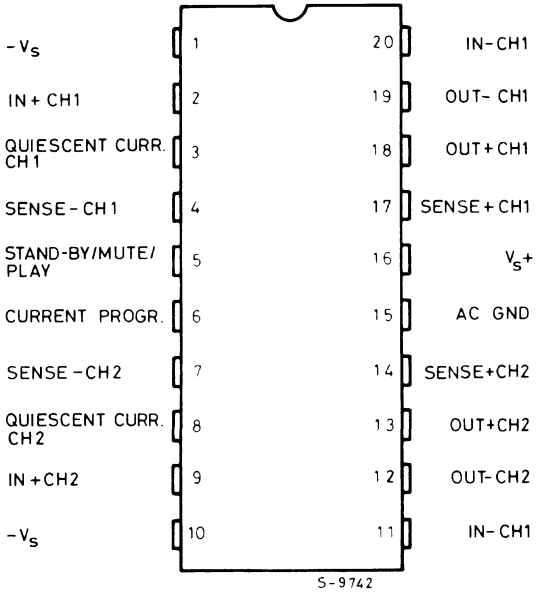


TDA7250

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	100	V
P_{tot}	Power dissipation at $T_{amb} = 60°C$	1.4	W
T_j, T_{stg}	Storage and junction temperature	-40 to +150	°C

CONNECTION DIAGRAM
(Top view)



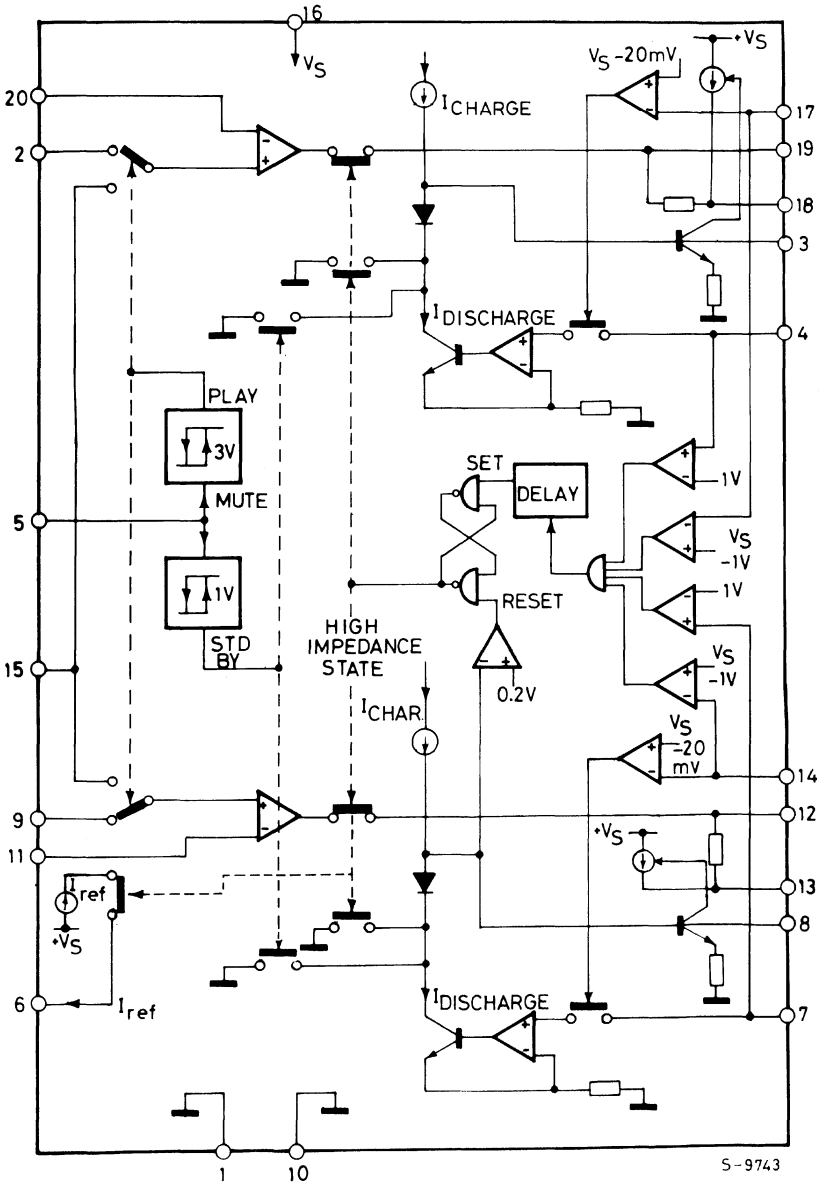
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	65	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	V_s- POWER SUPPLY	Negative supply voltage.
2	NON-INV. INP. CH. 1	Channel 1 input signal.
3	QUIESC. CURRENT CONTR. CAP. CH 1	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 1.
4	SENSE (-) CH. 1	Negative voltage sense input for overload protection and for automatic quiescent current control.
5	ST. BY / MUTE / PLAY	Three-functions terminal. For V_{IN} = 1 to 3V, the device is in MUTE and only quiescent current flows in the poser stages; - for $V_{IN} < 1V$, the device is in STAND-BY mode and no quiescent current is present in the power stages; - for $V_{IN} > 3V$, the device is fully active.
6	CURRENT PROGRAM	High impedance power-stages monitor.
7	SENSE (-) CH. 2	Negative voltage sense input for overload protection and for automatic quiescent current control.
8	QUIESC. CURRENT CONTR. CAP. CH. 2	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 2. If the voltage at its terminals drops under 250mV, it also resets the device from high-impedance state of output stages.
9	NON-INV. INP. CH. 2	Channel 2 input signals.
10	V_s- POWER SUPPLY	Negative supply voltage.
11	INVERT. INP. CH. 2	Feedback from output (channel 2).
12	OUT (-) CH. 2	Out signal to low driver transistor of channel 2.
13	OUT (+) CH. 2	Out signal to high driver transistor of channel 2.
14	SENSE (+) CH. 2	Positive voltage sense input for overload protection and for automatic quiescent current control.
15	COMMON AC GROUND	AC input ground in MUTE condition.
16	V_s+ POWER SUPPLY	Positive supply voltage.
17	SENSE (+) CH. 1	Positive voltage sense input for overload protection and for automatic quiescent current control.
18	OUT (+) CH. 1	Out signal to high driver transistor of channel 1.
19	OUT (-) CH. 1	Out signal to low driver transistor of channel 1.
20	INVERT. INP. CH. 1	Feedback from output (channel 1).

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = ± 35V, play mode, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 10		± 45	V
I_d	Quiescent drain current	Stand-by mode			8		mA
		Play mode			10	14	
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage				1	± 10	mV
I_{os}	Input offset current				100	200	nA
G_v	Open loop voltage gain	f = 100Hz			90		dB
		f = 10KHz			60		
e_N	Input noise voltage	R_G = 600Ω B = 20Hz to 20KHz			3		μV
SR	Slew rate				10		V/μs
d	Total harmonic distortion	G_v = 26dB	f = 1KHz		0.004		%
		P_o = 40W	f = 20KHz		0.03		
V_{opp}	Output voltage swing				60		V_{pp}
P_o	Output power (*)	V_s = ± 35V V_s = ± 30V V_s = ± 35V	R_L = 8Ω R_L = 8Ω R_L = 4Ω		60 40 100		W
I_o	Output current				± 5		mA
SVR	Supply voltage rejection	f = 100Hz			75		dB
C_s	Channel separation	f = 1KHz			75		dB

MUTE / STANDBY / PLAY FUNCTIONS

I_i	Input current (pin 5)			0.1		μA
V_{th}	Comparator standby/mute threshold (**)		1.0	1.25	1.5	V
H	Hysteresis standby/mute			200		mV
V_{th}	Comparator mute/play threshold (**)		2.4	3.0	3.6	V
H	Hysteresis mute/play			300		mV
	Mute attenuation			60		dB
V_i	Input voltage max. (Pin 5)		12 (**)			V

(*) Application circuit of fig. 1 f = 1KHz; d = 0.1%; G_v = 26dB
(**) Referred to $-V_S$

ELECTRICAL CHARACTERISTICS (continued)

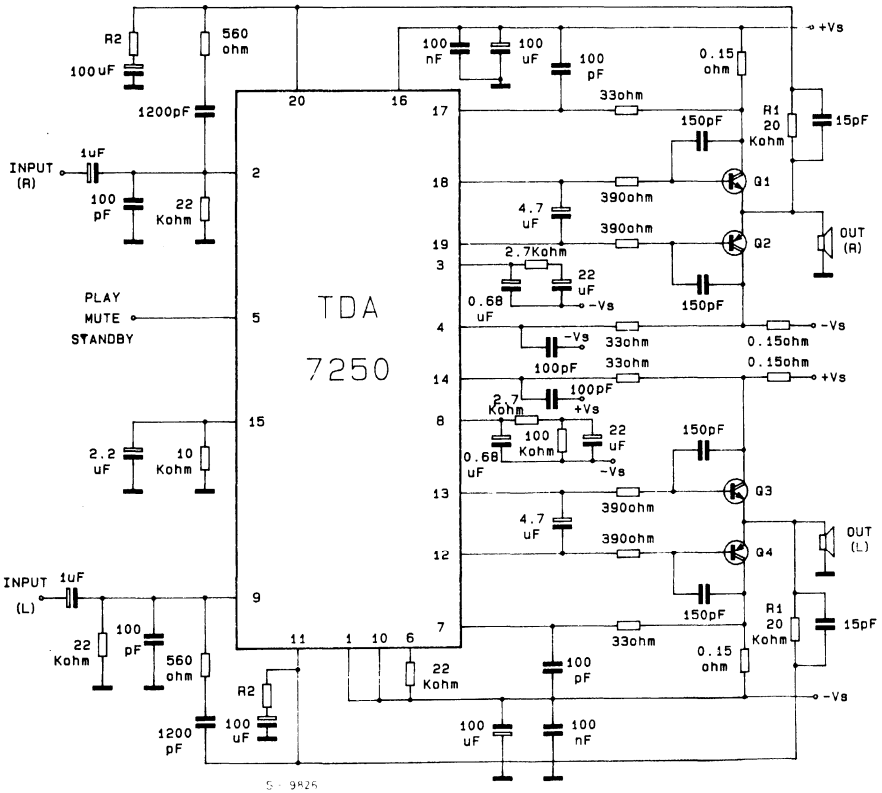
CURRENT SURVEY CIRCUITRY

	Comparator reference	to $+V_S$ to $-V_S$	0.8 0.8	1 1	1.4 1.4	V V
t_d	Delay time		10			μs

QUIESCENT CURRENT CONTROL

	Capacitor current	Charge Discharge	30 250	60 500		μA μA
	Comparator reference	to $+V_S$ to $-V_S$	15	20 10	25	mV mV

Fig. 1 - Application circuit with Power Darlingtons



NOTE: Q1/Q2 = Q3/Q4 = TIP 142/TIP 147

Fig. 2 - Output power vs. supply voltage

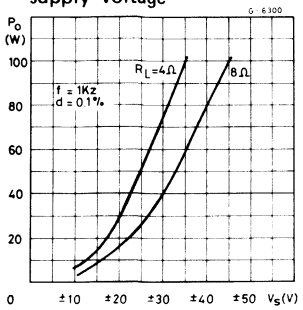


Fig. 3 - Distortion vs. output power (*)

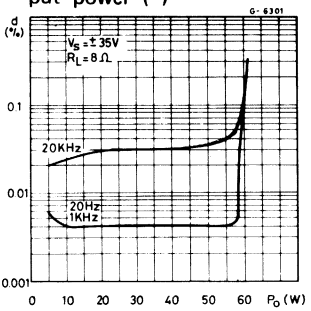


Fig. 4 - Channel separation

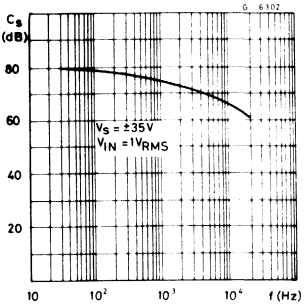


Fig. 5 - Supply voltage rejection vs. frequency

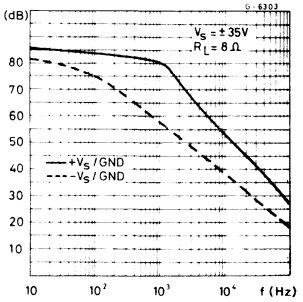


Fig. 6 - Quiescent current vs. supply voltage

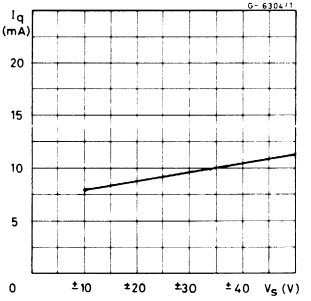


Fig. 7 - Quiescent current vs. T_{amb}

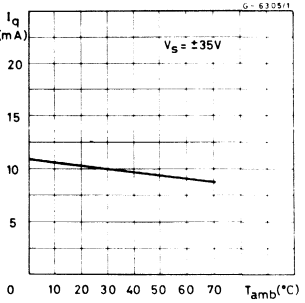


Fig. 8 - Total dissipated power vs. output power (*)

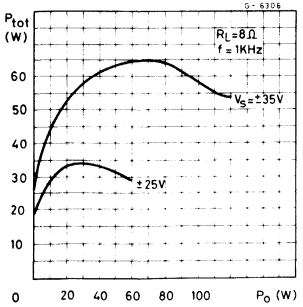


Fig. 9 - Efficiency vs. output power (*)

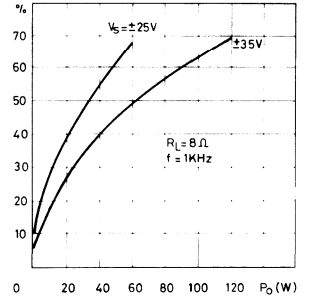
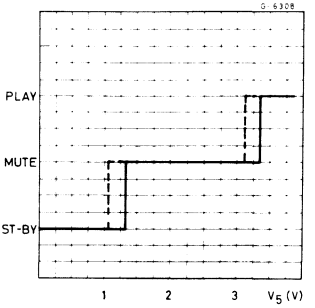
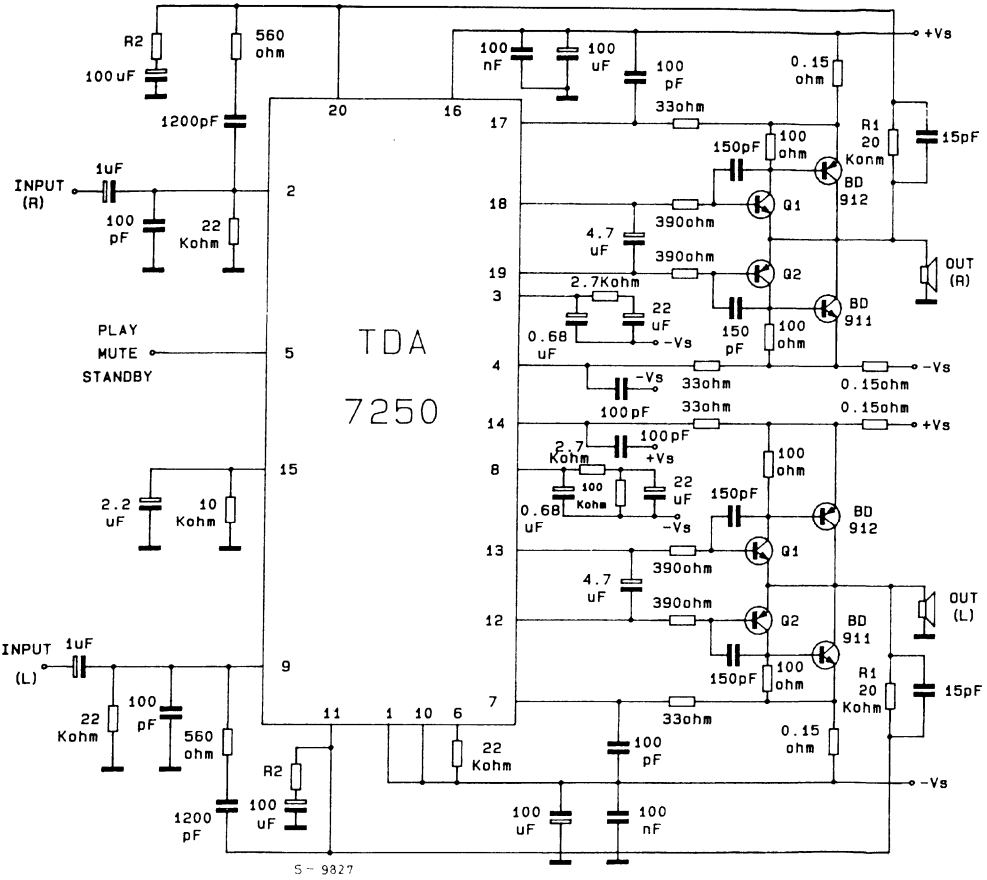


Fig. 10 - Play-mute standby operation



(*) Complete circuit

Fig. 11 - Application circuit using power transistors



TDA7255

ADVANCE DATA

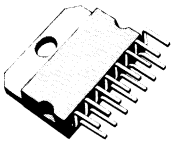
22W FRONT REAR OR BRIDGE FULLY PROTECTED CAR RADIO AMPLIFIER

- HIGH OUTPUT POWER
- POP FREE SWITCHING
- SHORT CIRCUIT PROTECTIONS: R_L SHORT - OUT TO GROUND - OUT TO V_S
- MUTING μP COMPATIBLE
- VERY LOW CONSUMTION STANDBY
- PROGRAMMABLE TURN ON DELAY
- LOW DISTORTION AND LOW NOISE
- DIFFERENTIAL INPUT

Other Protections:

- LOAD DUMP VOLTAGE SURGE
- LOUDSPEAKER DC CURRENT
- VERY INDUCTIVE LOAD
- OVERATING TEMPERATURE
- OPEN GROUND

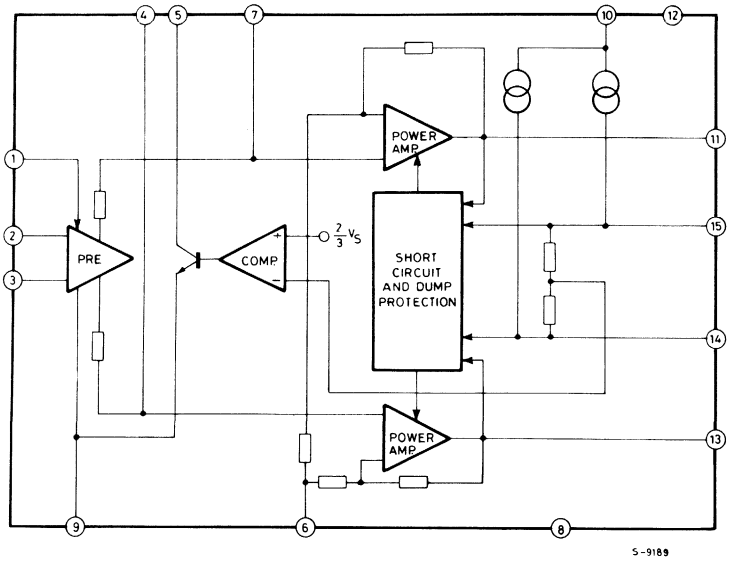
The TDA7255 a class B dual fully protected power amplifier designed for car radio applications. The device can be switched from Front-Rear to Bridge configuration by changing only the loudspeaker connection. An input fader for Front-Rear control is available. A high current capability allows to drive low impedance loads (up to 1.6Ω).



Multiwatt-15

ORDER CODE: TDA7255

BLOCK DIAGRAM

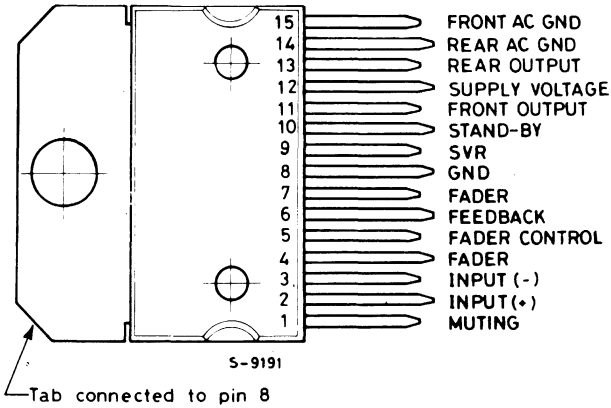


TDA7255

ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o	Output peak current (non repetitive t = 0.1ms)	4.5	A
I_o	Output peak current (repetitive f $\geqslant$ 10Hz)	4	A
P_{tot}	Power dissipation at T_{case} = 60°C	30	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	40	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 14.4V, R_L = 4Ω, f = 1KHz, T_{amb} = 25°C unless otherwise specified)

Paremeter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
I_d	Total quiescent drain current			80		mA
R_i	Input resistance			70		KΩ
V_i	Input saturation voltage		300			mV
T_j	Thermal shut down junction temperature			145		°C

FRONT REAR APPLICATIONS (Fig. 2)

P_o	Output power	THD = 10% R_L = 4Ω R_L = 2Ω R_L = 1.6Ω	5.5	6.5 11 12.5		W W W
d	Distortion	P_o = 0.1W to 4W		0.05	0.5	%
G_v	Voltage gain			28		dB
e_N	Input noise voltage	R_G = 10KΩ		2.5(**) 2 (*)		μV μV
SVR	Supply voltage rejection	R_G = 100KΩ V_r = 1V f = 300Hz	36	45		dB
CMR	Common mode rejection			55		dB
η	Efficiency	P_o = 6.5W + 6.5W		70		%

BRIDGE APPLICATION (Fig. 1)

V_{os}	Output offset voltage				250	mV
P_o	Output power	THD = 10% R_L = 4Ω R_L = 3.2Ω	18	22 25		W W
d	Distortion	P_o = 0.1W to 2W		0.05		%
G_v	Voltage gain (C_L)			36		dB
e_N	Total input noise voltage	R_G = 10KΩ		2.5(**) 2.0 (*)	10	μV μV
η	Efficiency	P_o = 20W		66		%
SVR	Supply voltage rejection	R_G = 10KΩ, V_r = 1V, f = 300Hz	45	58		dB

MUTING AND STAND-BY FUNCTIONS

	Muting attenuation	V_{ref} = 1W f = 100Hz to 10KHz	60			dB
	Muting-on threshold voltage		2.4			V
	Muting-off threshold voltage				0.8	V
	Stand-by attenuation	V_{ref} = 1V f = 100Hz to 10KHz	60			dB
	Stand-by quiescent drain current				100	μA

(**) B = 22Hz to 22KHz
(*) B = curve A

TDA7255

Fig. 1 - Test and application circuit (Bridge amplifier)

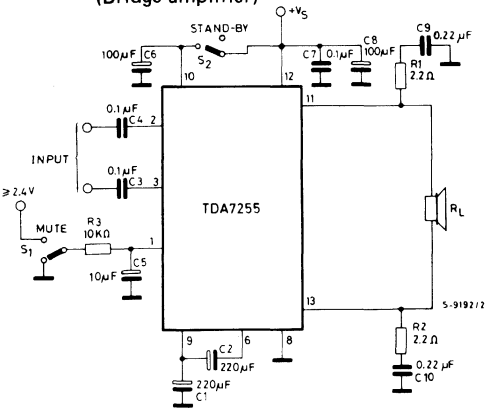
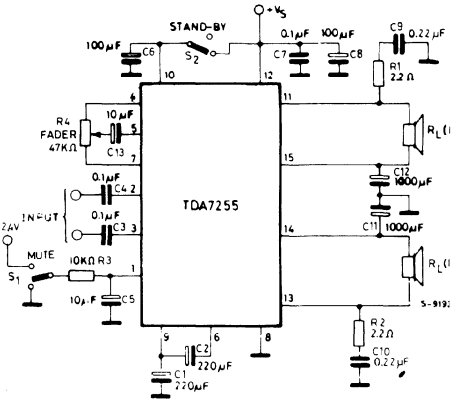
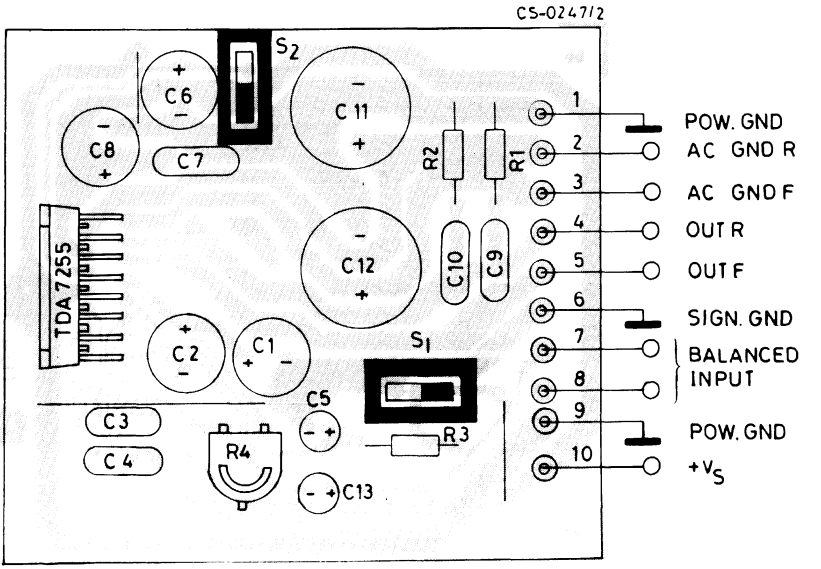


Fig. 2 - Test and application circuit (F/R amplifier)



- Two high impedance inputs available for balanced or unbalanced operation.
- The fader function is automatically inserted in front/rear configuration and allows the distortion of the power between the front and the rear. An external potentiometer must be connected between pins 4 and 7 with the control terminal connected to pin 5 through a decoupling capacitor. In bridge applications the pins 4-5-7 must be left open.
- Turn on delay. The output stages are muted during the turn on transient and start rising after the charge of the capacitor connected between pin 9 and ground. The capacitor also avoids pops during bridge F/R switching.

Fig. 3 - P.C. board and component layout of the circuits of Fig. 1 and 2 (1 : 1 scale)



FRONT/REAR CHARACTERISTICS

Fig. 4 - Quiescent drain current vs. supply voltage

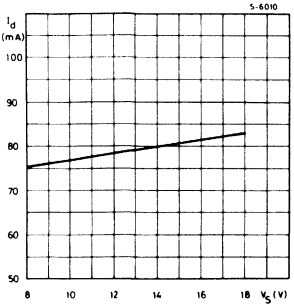


Fig. 5 - Quiescent output voltage vs. supply voltage

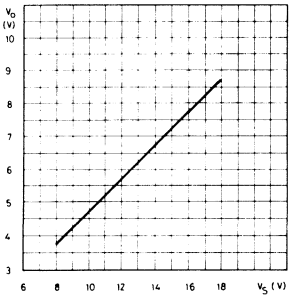


Fig. 6 - Output power vs. supply voltage

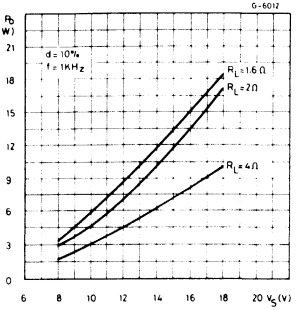


Fig. 7 - Distortion vs. frequency

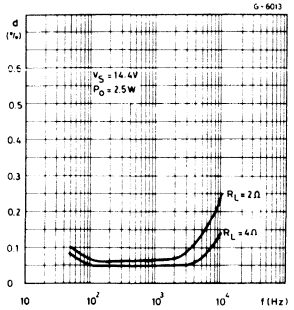


Fig. 8 - Supply voltage rejection vs. capacitor values (C2)

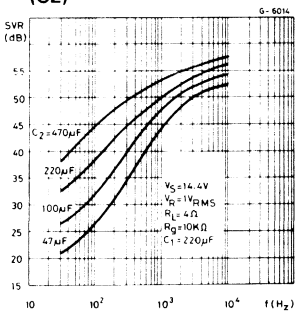


Fig. 9 - Supply voltage rejection vs. capacitor values (C1)

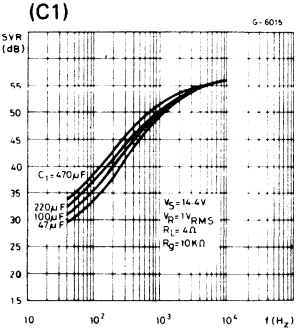


Fig. 10 - Output signal vs. fader control position

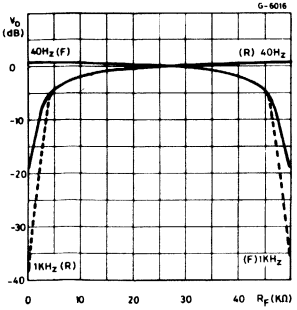


Fig. 11 - Power dissipation and efficiency vs. output power

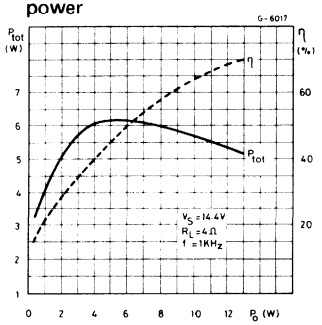
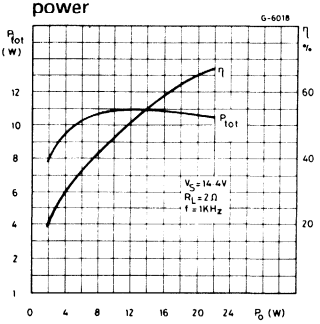


Fig. 12 - Power dissipation and efficiency vs. output power



BRIDGE CHARACTERISTICS

Fig. 13 -- Output power vs. supply voltage

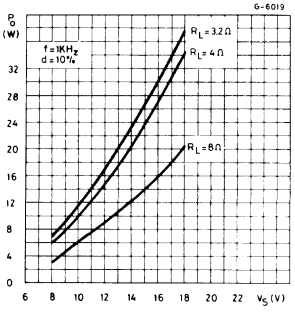


Fig. 14 - Distortion vs. frequency

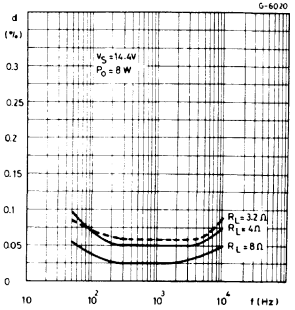


Fig. 15 - Supply voltage rejection vs. frequency

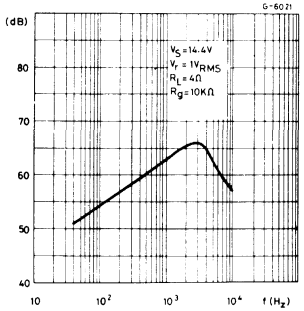
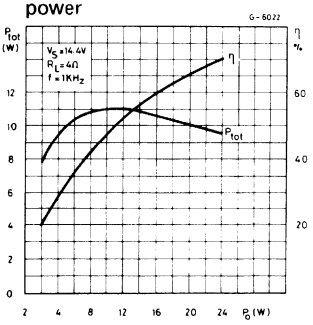


Fig. 16 - Power dissipation and efficiency vs. output power



TDA7260

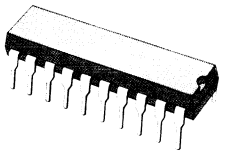
ADVANCE DATA

HIGH EFFICIENCY AUDIO PWM DRIVER

- HIGH EFFICIENCY
- P_o = 30W WITH POWER MOS BRIDGE
- LOW DISTORTION
- SINGLE SUPPLY OPERATION
- MUTING FACILITY
- THERMAL AND SHORT-CIRCUIT PROTECTION
- DUMP PROTECTION

The TDA7260 is a new type of audio driver mainly intended for use in car radio applications. In conjunction with four POWER MOS in bridge configuration it can deliver 30W ($d < 3\%$ R_L = 2Ω). The device acts in "class D" as a pulse width modulation circuit. That permits a very high efficiency (> 80% at rated output power) so no heatsinks are needed. Moreover, a built-in limiter reduces the clipping effects.

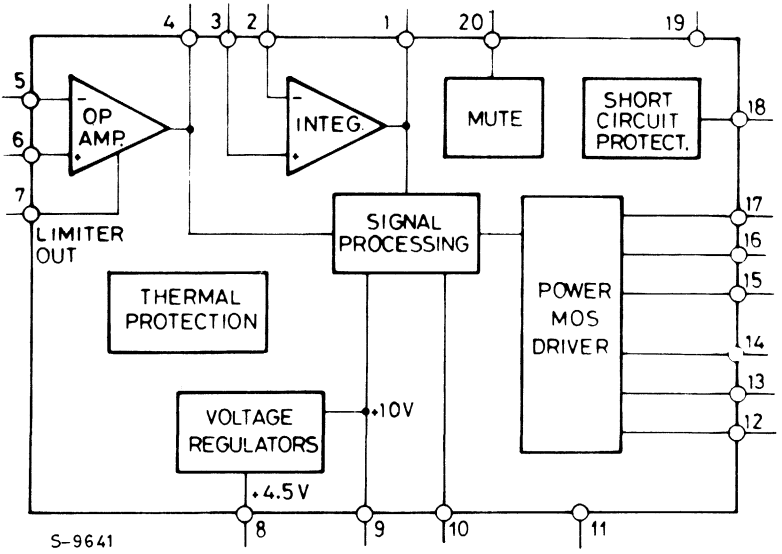
The TDA7260 is a monolithic integrated circuit in a 20 lead dual in line plastic package.



DIP-20 Plastic
(0.4)

ORDERING NUMBER: TDA7260

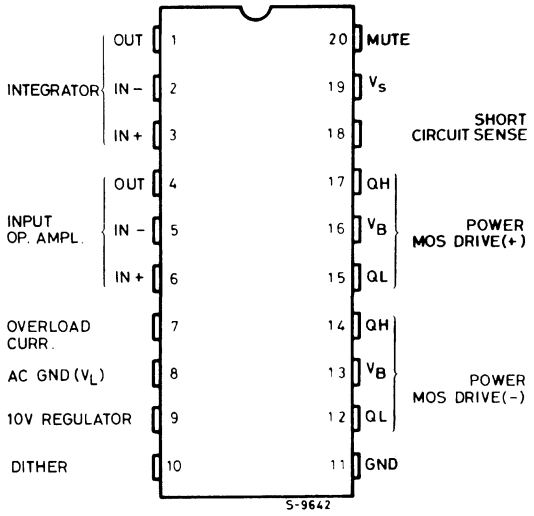
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
V_s	Peak supply voltage (50ms)	40	V
V_{IN}	Input voltage	10	V
V_D	Differential input voltage	± 6	V
I_P	Peak output current	300	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUITS

Fig. 1 -

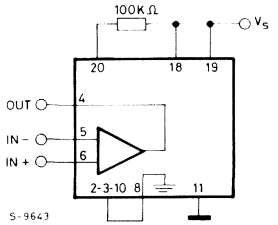


Fig. 2 -

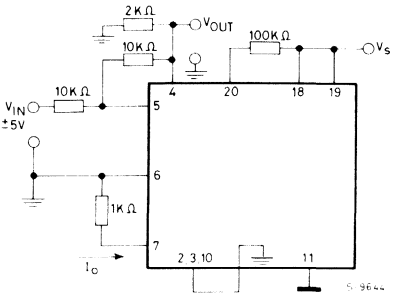


Fig. 3

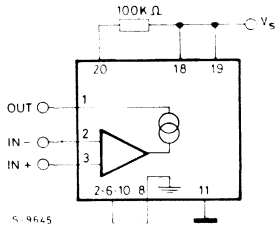


Fig. 4

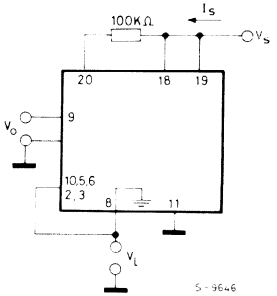


Fig. 5

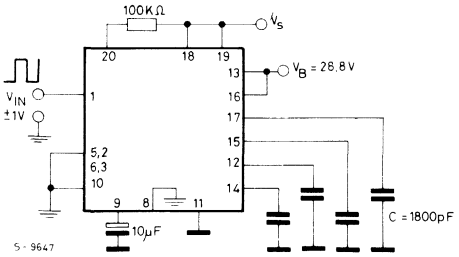
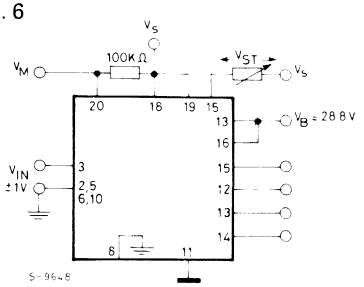


Fig. 6



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 14.4V unless otherwise specified, refer to test circuit)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
OP AMP							
V_{os}	Input offset voltage				± 4	mV	1
I_b	Input bias current			120	300	nA	1
I_{of}	Input offset current				± 50	nA	1
G_v	Open loop voltage gain		80			dB	1
d	Total harmonic distortion	f = 1KHz A_v = 1		0.005		%	1
BW	Unity gain bandwith		0.8	1.8		MHz	1
CMRR	Common mode rejection	V_{IN} = 1V f = 1KHz	70	90		dB	1
SVR	Supply voltage rejection	V_r = 1V f = 1KHz	80	100		dB	1
E_n	Input noise voltage	B = 200KHz		1		mV	1
I_n	Input noise current	B = 20KHz		20		nA	1
SR	Slew rate			0.8		V/ms	1
V_O	Output swing	R_L = 2KΩ A_v = 1	± 2.6		± 3.2	V	2
R_{IN}				100		KΩ	1
I_7	Overload indicator current			240		mA	
INTEGRATOR							
V_{os}	Input offset voltage				± 4	mV	3
I_b	Input bias current			0.5	2.5	mA	3
I_{of}	Input offset current				± 250	nA	3
I_o	Output current swing sink source	 ΔV_{IN} = ± 1V R_L = 0	 0.4 0.4	 1 1		 mA mA	3
V_o	Output voltage swing	ΔV_{IN} = ± 1V R_L = 5KΩ	± 3			V	3
CMRR	Common mode rejection	V_{IN} = 1V f = 1KHz	70	90		dB	3
SVR	Supply voltage rejection	V_r = 1V f = 1KHz	80	100		dB	3
R_{IN}			100			KΩ	3
BW	Unity gain bandwidth			4		MHz	3
G_n	Forward transconductance			30		mA/V	3
REGULATORS							
V_o	Output stability voltage			10		V	4
SVR	Supply voltage rejection	f = 1KHz V_r = 1V	60	70		dB	4
V_I	Ground voltage			4.5		V	4

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYSTEM SPECIFICATION							
V_s	Operating supply voltage range	See fig. 6		(10.5 to 16)		V	
I_s	Supply current	$V_{IN} = 0$		30	60	mA	4
V_{tm}	Mute threshold voltage (*)	$V_{IN} = 0$	3	4	5.5	V	6
V_{tmh}	Mute threshold hysteresis	$V_{IN} = 0$		0.5		V	6
V_{oH}	(QH, QH) Output swing	I = 70mA	25			V	6
V_{oH}	(QL, QL) Output swing	I = 70mA	10.8			V	6
V_{oL}	(QH, QH) Output swing	I = 70mA			2.8	V	6
V_{oL}	(QL, QL) Output swing	I = 70mA			2.8	V	6
V_{st}	Overload sense threshold		0.2		0.4	V	6
V_{om}	Muted outputs	I = 70mA Mute or overload condition			2.8	V	6
V_x	Gate crossover voltage	f = 1KHz		2		V	5
COMPLETE SYSTEM							
I_o	Supply current	$V_{IN} = 0$ $R_L = \infty$		90		mA	7
V_{of}	Output offset voltage	$V_{IN} = 0$		5		mV	7
CMRR	Common mode ripple rejection	$V_{IN} = 0.5V$ f = 100Hz		60		dB	7
SVR	Supply voltage ripple rejection	$\Delta V_s = 0.5V$ f = 100Hz		60		dB	7
G_v	Voltage gain	$P_o = 1W$ f = 1KHz		12		dB	7
E_n	Output noise voltage	B = 20KHz $V_{IN} = 0$		150		μV	7
P_o	Output power	d = 2% f = 1KHz		32		W	7
d	Total harmonic distortion	f = 14KHz $V_o = 2V$		0.4		%	7
f_s	Switching frequency	$V_{IN} = 2V$ $V_{10} = V_8$	70	125		KHz	7
f_d	Dither frequency			20		Hz	7
η	Efficiency	$P_o = 32W$ f = 1KHz		85		%	7

(*) Device on for $V_{pin\ 20}$ higher than V_{tm}

Fig. 7 - Application circuit

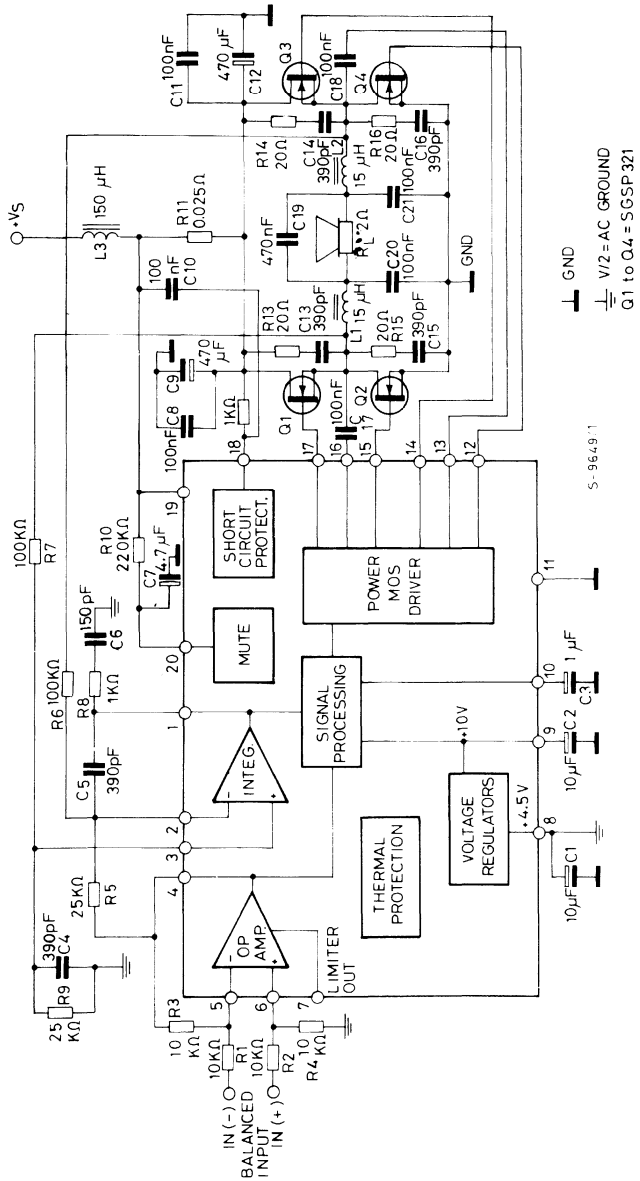


Fig. 7a - P.C. board and components layout of the circuits of fig. 7 (1 : 1 scale)

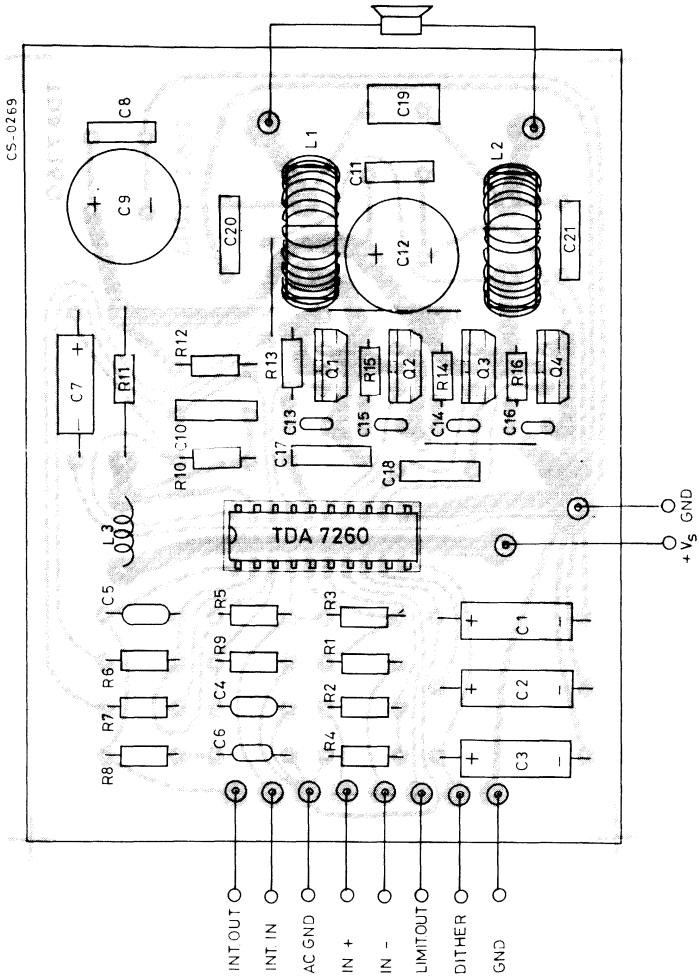


Fig. 8 - Quiescent current vs. supply voltage

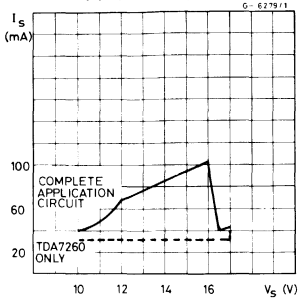


Fig. 9 - Distortion vs. output power

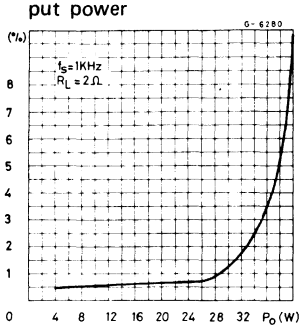


Fig. 10 - Distortion vs. frequency

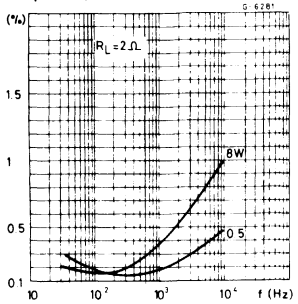


Fig. 11 - Frequency response

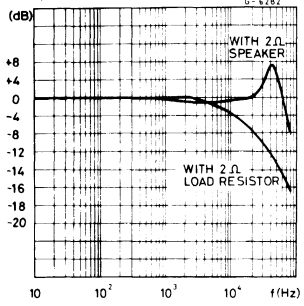


Fig. 12 - Dither frequency versus $C_{(PIN\ 10)}$

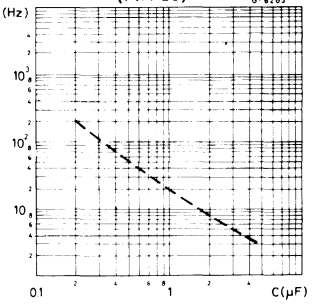


Fig. 13 - Efficiency vs. output power

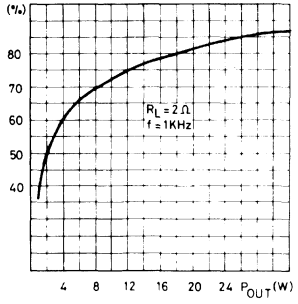


Fig. 14 - Power dissipation vs. output power

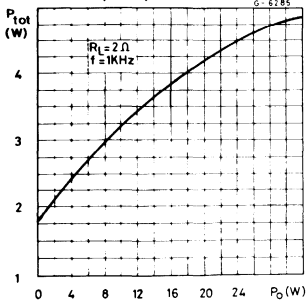


Fig. 15 - Suggested application circuit using the TDA7232 preamplifier/compressor

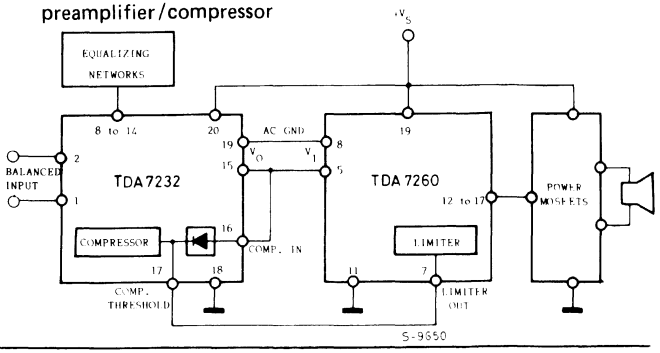


Fig. 16 - 25W application circuit

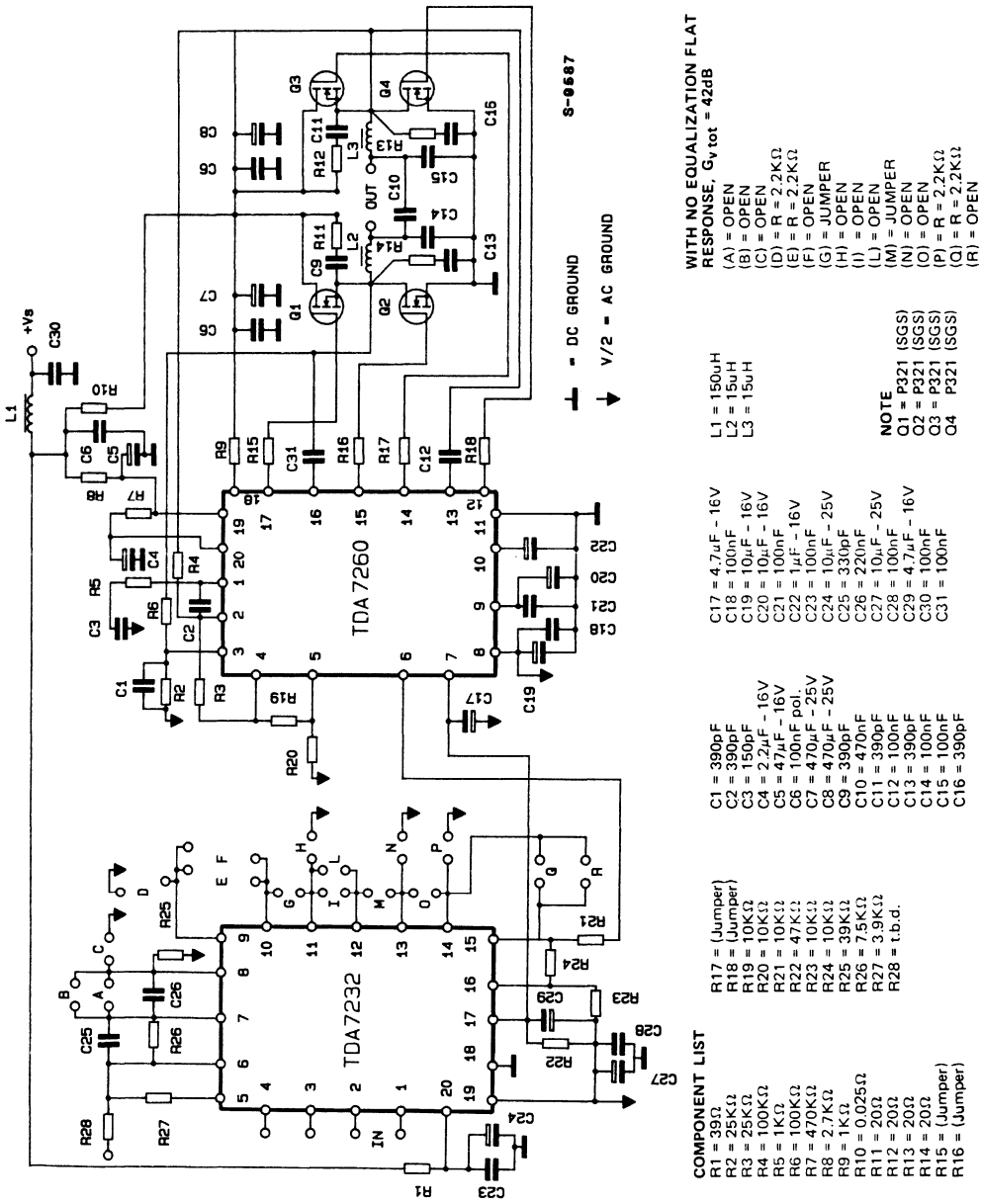
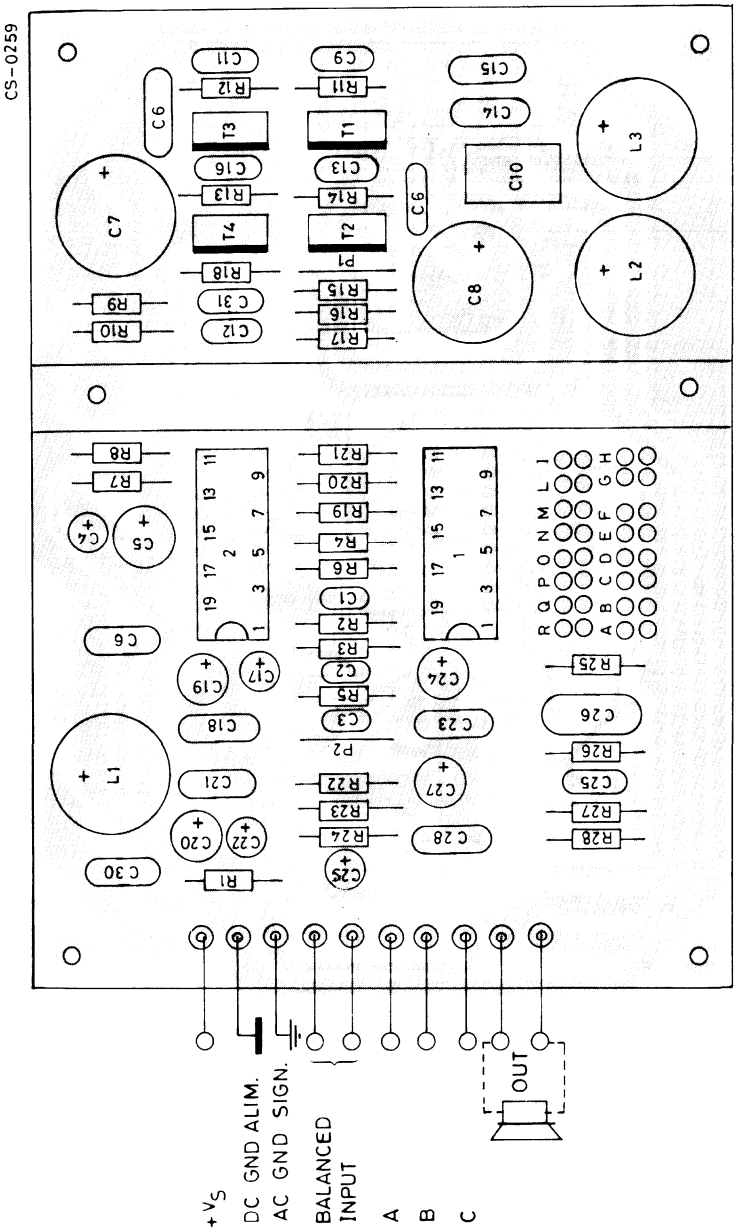
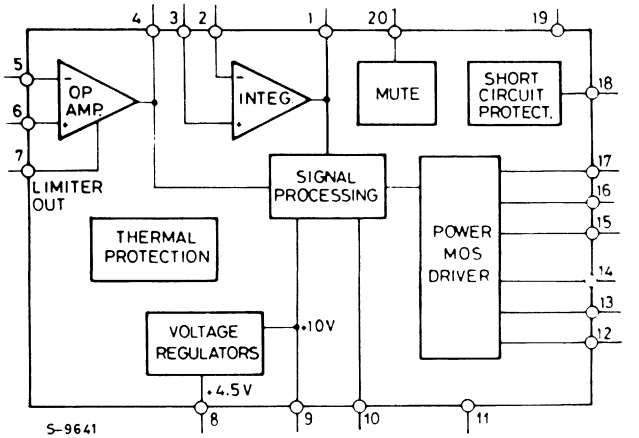


Fig. 17 - P.C. board and components layout of the circuit of fig. 16 (1:1 scale)



APPLICATION INFORMATION

Fig. 18 - Block diagram



CIRCUIT DESCRIPTION

BLOCK DIAGRAM

Fig. 18 shows the circuit block diagram. Following are described the single circuit blocks and their functions.

VOLTAGE REGULATOR

It generates two values of reference voltage, accessible even on external pins. 10V is the voltage that supplies all the analogic internal blocks. 4,5V (V1) is the voltage value which stands for ground of the signal inside the chip.

INPUT AMPLIFIER, INTEGRATOR, COMPARATOR WITH HYSTERESIS, N-FET BLOCK DRIVER

These components implement the control system main loop, together with the external four power devices. The TSM (two state modulation) system is used.

The input amplifier is utilized in differential configuration, and refers the input signal to V1 voltage; in such way the chip turns to general use. On the input amplifier acts a dynamic limiter circuit, with intervention proportional to supply voltage avoiding overload and aliasing at lower V_s (Fig. 19).

Fig. 19 - Duty cycle input dynamic limitation.

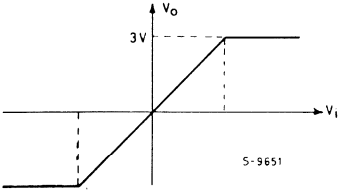
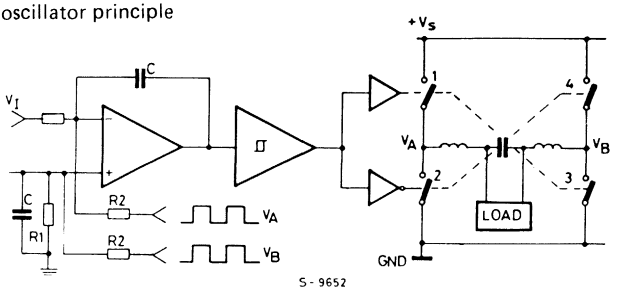


Fig. 20 - Free running oscillator principle



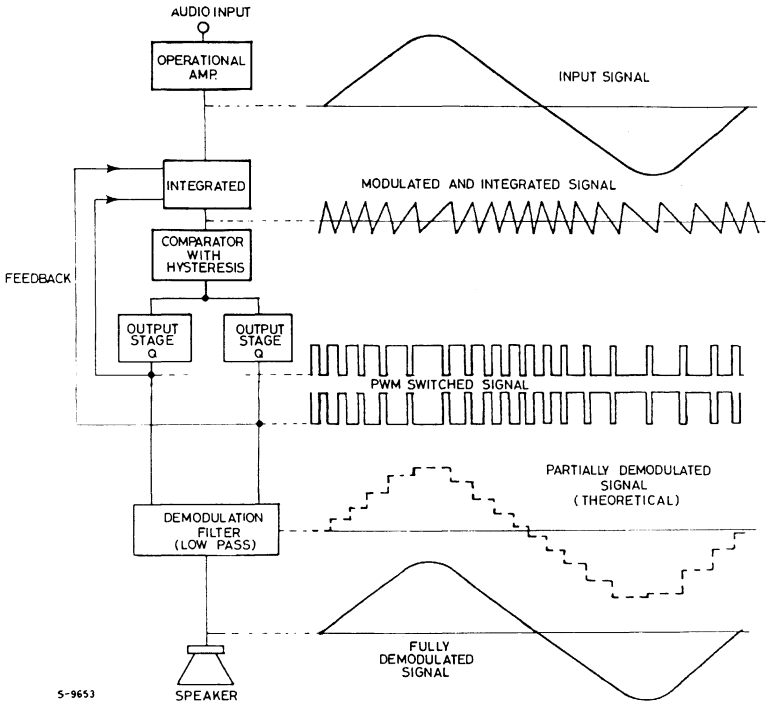
APPLICATION INFORMATION (continued)

A signal for supplying an external compressor stage (i.e. TDA7232) is available.

For the effective control loop the feedback signal is taken from switched points of external power bridge (before LC output demodulation filter) and sent to the integrator (see Fig. 20).

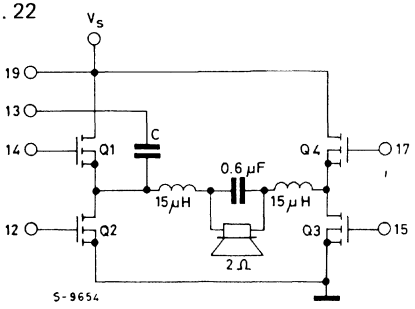
The triangle waveform at the integrator output drives the comparator with a hysteresis, and this supplies the correct time-intervals to the driving stages (Fig. 21).

Fig. 21



When an audio signal is introduced to the integrator, it generates an offset which varies the duty cycle and frequency of the switching output (with no audio signal the duty cycle is 50%). The bridge POWER MOS with the drain connected to the supply voltage, are driven in boostrap. The choice of MOS device is suggested by the high commutation speed and in order to reduce the chip dissipation. The Mosfets SGSP321 can be succesfully used. The LC filter on the bridge output demodulates the signal and reconstructs the sine wave on the speaker (see Fig. 22).

Fig. 22

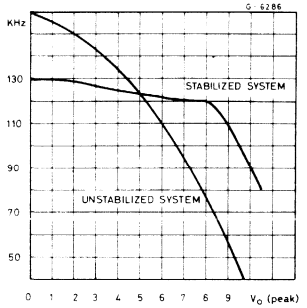


APPLICATION INFORMATION (continued)

SWITCHING FREQUENCY STABILIZER

It consists of a block which stabilizes the switching frequency of the system; it receives the supply voltage and the input signal amplitude as inputs, and accomplishes its function by varying the histeresis thresholds of the comparator. The purpose of such stabilizer is to reduce the range of the switching frequency (40KHz $< F_{sw} <$ 200KHz) avoiding greather variations versus supply voltage, input signal, output current. (Fig. 23).

Fig. 23



DITHER OSCILLATOR

it is a low-frequency oscillator. Its frequency (20Hz typ.) is set by an external capacitor; at this value it determines a frequency switching modulation of about 10% around its nominal value, in order to minimize the problem of the spurious irradiations of the harmonics at the switching frequency (EMI).

MUTE

It is a protection circuit which shuts the system off when the supply voltage is lower than 10.5V and higher than 16V. The switching-on is further delayed by an external capacitor. In mute condition the outputs are low (Figs. 24, 25).

SHORT CIRCUIT PROTECTION

It is a comparator having an offset which senses the current drawn by the power stage by a voltage drop across an external resistor (internal V_{TH} = 250mV): it acts on the mute circuit.

Fig. 24

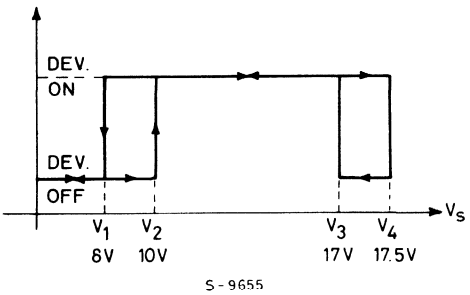
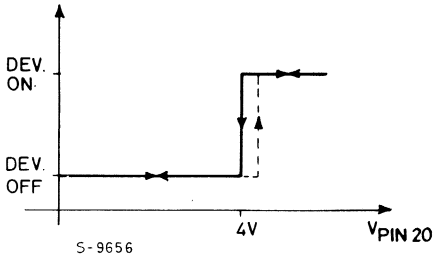


Fig. 25



THERMAL AND DUMP PROTECTIONS

It shuts the device off when the junction temperature rises above 150°C, and it has a hysteresis of above 20°C typ. It acts on the mute circuit..

The device is protected against supply overvoltages (V = 40V, t = 50ms).

TDA7270S

NOT FOR NEW DESIGN

MULTIFUNCTION SYSTEM FOR TAPE PLAYERS

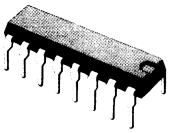
The TDA7270S is a multifunction monolithic integrated circuit in a 16-lead dual in-line plastic package specially designed for use in car radios cassette players, but suitable for all applications requiring tape playback.

It has the following functions:

- Motor speed regulator
- Automatic stop
- Manual stop
- Pause
- Cassette ejection
- Radio - Playback automatic switching.

The circuit incorporates also:

- Thermal protection
- Short circuit protection to ground (all the pins).



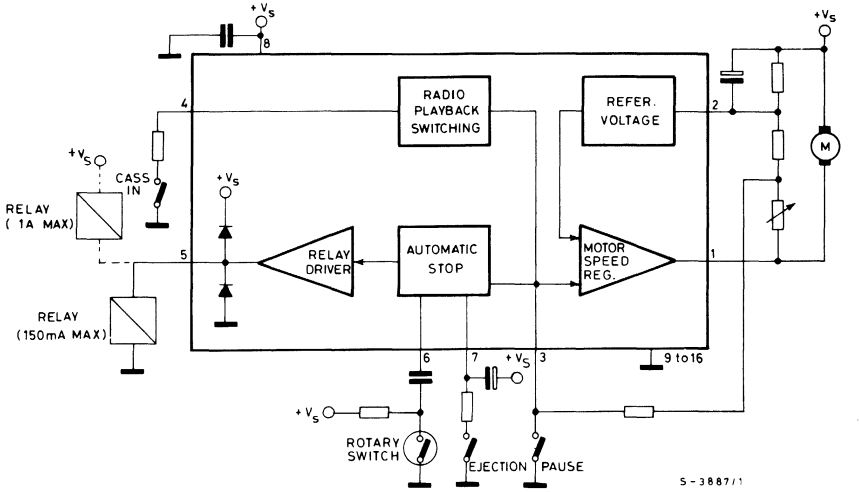
Powerdip
(8 + 8)

ORDERING NUMBER: TDA7270S

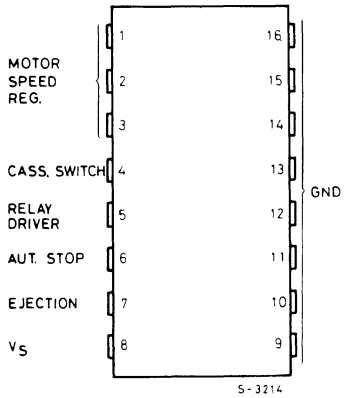
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_1	Sink peak current at pin 1	2	A
I_5	Sink peak current at pin 5	2	A
P_{tot}	Power dissipation at $T_{amb} \leqslant 80°C$	1	W
T_{stg} ; T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W

ELECTRICAL CHARACTERISTICS
(Refer to the test circuit; T_{amb}= 25°C; V_s = 14V; S_7 at B, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		6		18	V
I_d	Quiescent drain current	Automatic stop-S_3 at B; S_4 at B		5	10	mA
		Pause - S_3 at A; S_4 at A		9	15	
I_5	Maximum output current for relay driving		150			mA
T_{sd}	Thermal shut-down case temperature	P_{tot} = 1W ($\frac{\Delta V_{ref}}{V_{ref}}$ = -5%)	105	125		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MOTOR SPEED CONTROL						
I_{MS}	Starting current (pin 1)		1			A
V_{ref}	Reference voltage (pin 2-3)	I_M= 100 mA	1.15	1.25	1.35	V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$		I_M= 100 mA V_s = 8 to 18V		0.1	0.4	%/V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$		I_M= 50 to 400 mA		0.01	0.03	%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$		I_M= 100 mA T_{amb}= -20 to 70°C		0.01		%/°C
V_2	Operating voltage	I_M= 100 mA $\frac{\Delta V_{ref}}{V_{ref}}$ = -5%	2.4			V
K	Reflection coeff.(K= I_M/I_T see fig. 12)	I_M= 100 mA	18	20	22	—
$\frac{\Delta K}{K}/\Delta V_s$		I_M= 100 mA V_s= 8V to 18V		0.3	1	%/V
$\frac{\Delta K}{K}/\Delta I_M$		I_M= 50 to 400 mA		0.005	0.02	%/mA
$\frac{\Delta K}{K}/\Delta T$		I_M= 100 mA T_{amb}= -20 to 70°C		0.01		%/°C
PAUSE						
I_3	Current consumption	S_4 at A	1.4			mA
V_{8-1}		S_4 at A			0.2	V
EJECTION						
I_7		S_2 in A	20			μA
V_{5-8}	Saturation voltage	I_5 = 100 mA		2.1	3	V
V_5	Saturation voltage	I_{5-8}= 1.5A		2.2	3	V
V_4	(Pause condition)	S_1 at A S_3 at A S_4 at A	6			V
V_4	(Radio)	S_1 at A S_3 at B S_4 at B	6	9		V
V_4	(Tape)	S_1 at A S_3 at A S_4 at B			1.7	V
R_o	Output impedance at pin 4	S_3 at B		16	22	KΩ
AUTOMATIC STOP						
V_{8-1}	Saturation voltage	S_1 at B S_2 at B S_3 at B			1	μA
I_6	Minimum current to avoid stop	S_1 at C			1	μA
I_{7-8}	Load current for delay circuit	I_6= 0 S_7 at A S_2 at B	10.5	15	19.5	μA

APPLICATION INFORMATION

The TDA7270S incorporates four different functional blocks:

1) Motor speed control.
2) Autostop circuit.
3) Radio/Playback switching
4) Relay driver.

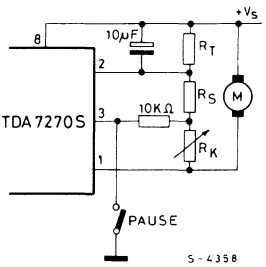
The motor speed control is a conventional circuit providing correction for the internal looses of the motor. Fig. 1 shows the external circuit.
The values of R_T, R_S and R_K determine the regulation characteristics and motor speed.

$$R_T = K \cdot R_M$$

where K = the IC regulator reflection coefficient and R_M = motor internal resistance.
The following condition must be always satisfied

$$R_S \leqslant 4\ R_T$$

Fig. 1



The voltage applied across the motor is given by

$$V_{8-1} = V_{ref}\left[1 + \frac{R_T}{R_S}\left(1 + \frac{1}{K}\right) + \frac{R_K}{R_S}\right]$$

and this is proportional to R_K which therefore adjust the speed.
The voltage between pin 2 and the supply must not fall below 0.3V and so

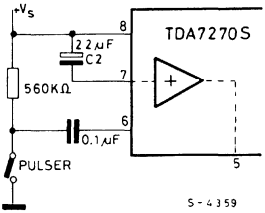
$$\left[V_{ref\ min}\left(\frac{R_T}{R_S}\right) + I_{M\ min}\left(\frac{R_T}{K_{max}}\right)\right] > 0.3V$$

The "pause" condition corresponds to $V_3 <$ 50mV; in this condition the motor will stop ($V_{1\text{-}8} < 0.2V$), the capacitor C_2 on the autostop circuit (see below) will no longer be charged and the pin 4 (cassette/radio switch output) will be pulled high.

The autostop circuit is shown in Fig. 2
In normal operation the capacitor C_2 (22μF) is slowly charged by a constant current drawn by pin 7 of 15μA, and each time the pulser (a switch on the cassette take-up speed shaft) closes, C_2 is discharged. If the cassette stops, and the pulse stops, the voltage on pin 7 falls.
This switches the power amplifier state and pin 5 goes low. Pin 5 can be used for one of two purposes:

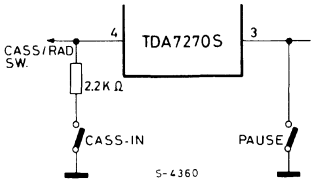
1) to drive a stop warning light connected from pin 5 supply V_s;
2) to actuate a solenoid wired either to ground (to release the cassette) or to supply (to eject the cassette).

Fig. 2



The **pause and/or cassette/radio switching** shown in Fig. 3 has an input/output on pin 4. If pin 4 is not used it should be grounded.

Fig. 3



This pin has the following logic.

Cass IN	Pause	Pin 4	Function
Open	Open	> 6V	motor off/radio on
Open	Close	> 6V	motor off/radio on
Close	Open	< 1.7V	motor on/cass. on
Close	Close	> 6V	pause/radio on

TDA7272

ADVANCE DATA

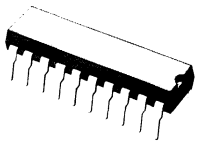
HIGH PERFORMANCE MOTOR SPEED REGULATOR

- TACHIMETRIC SPEED REGULATION WITH NO NEED FOR AN EXTERNAL SPEED PICK-UP
- V/I SUPPLEMENTARY PREREGULATION
- DIGITAL CONTROL OF DIRECTION AND MOTOR STOP
- SEPARATE SPEED ADJUSTMENT
- 5.5V TO 18V OPERATING SUPPLY VOLTAGE
- 1A PEAK OUTPUT CURRENT
- OUTPUT CLAMP DIODES INCLUDED
- SHORT CIRCUIT CURRENT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION (40V)

TDA7272 is an high performance motor speed controller for small power DC motors as used in cassette players.

Using the motor as a digital tachogenerator itself the performance of true tacho controlled systems is reached.

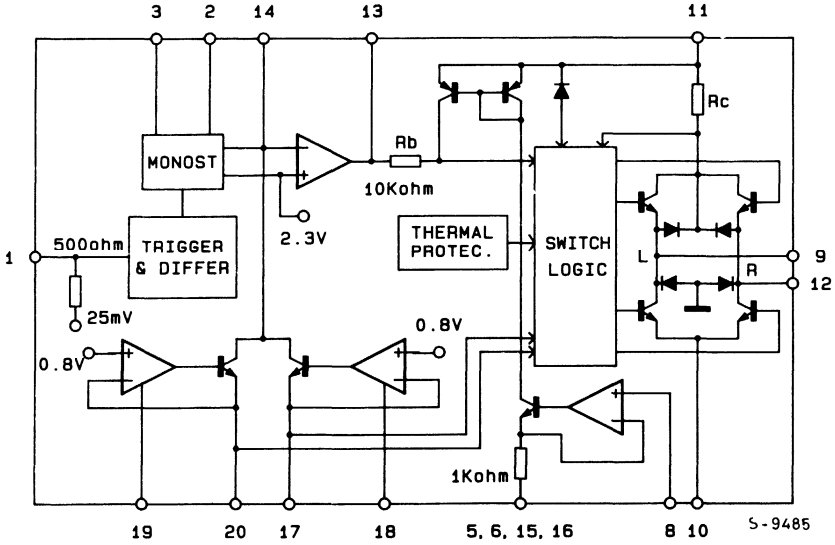
A dual loop control circuit provides long term stability and fast settling behaviour.



Powerdip
(16 + 2 + 2)

ORDERING NUMBER: TDA7272

BLOCK DIAGRAM

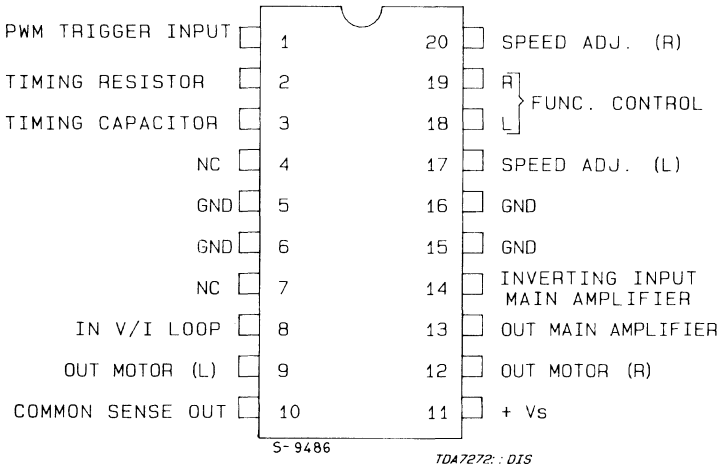


TDA7272

ABSOLUTE MAXIMUM RATINGS

V_S	DC supply voltage	24	V
V_S	Dump voltage (300ms)	40	V
I_O	Output current	internally limited	
P_{tot}	Power dissipation at $T_{pins} = 90°C$	4.3	W
	at $T_{amb} = 70°C$	1	W
T_j	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

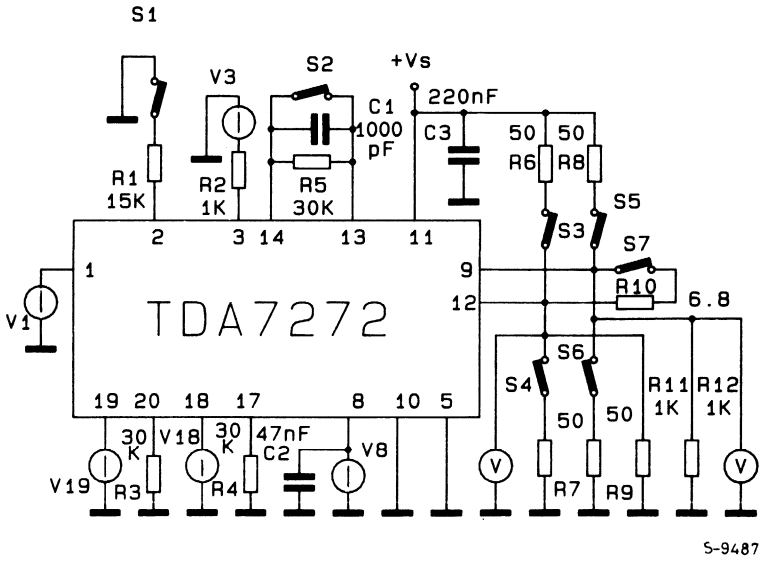
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	14	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = 13.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage		5.5		18	V
I_S	Supply current	No load		5	12	mA
OUTPUT STAGE						
I_O	Output current pulse		1			A
I_O	Output current continuous		250			mA
$V_{10\text{-}9,\ 12}$	Voltage drop	I_O = 250mA		1.2	1.5	V
$V_{11\text{-}9,\ 12}$	Voltage drop	I_O = 250mA		1.7	2	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
MAIN AMPLIFIER						
R_{14}	Input resistance		100			KΩ
I_b	Bias current			50		nA
V_{OFF}	Offset voltage			1	5	mV
V_R	Reference voltage	Internal at non inverting input		2.3		V
CURRENT SENSE AMPLIFIER V/I LOOP						
R_8	Input resistance		100			KΩ
G_L	Loop gain			9		
TRIGGER AND MONOSTABLE STAGE						
$V_{IN\,1}$	Input allowed voltage		-0.7		3	V
$R_{IN\,1}$	Input resistance			500		Ω
$V_{T\,Low}$	Trigger level			0		V
$V_{T\,B}$	Bias voltage (pin 1)		15	20	25	mV
$V_{T\,H}$	Trigger histeresis			10		mV
$V_{2\,REF}$	Reference voltage		750	800	850	mV
SPEED PROGRAMMING, DIRECTION CONTROL LOGIC AND CURRENT SOURCE PROGRAMMING						
$V_{18,\,19\,Low}$	Input Low level				0.7	V
$V_{18,\,19\,High}$	Input High level		2			V
$I_{18,\,19}$	Input current	$0 < V_{18,\,19} < V_S$		2		μA
$V_{17,\,20\,REF}$	Reference voltage		735	800	865	mV

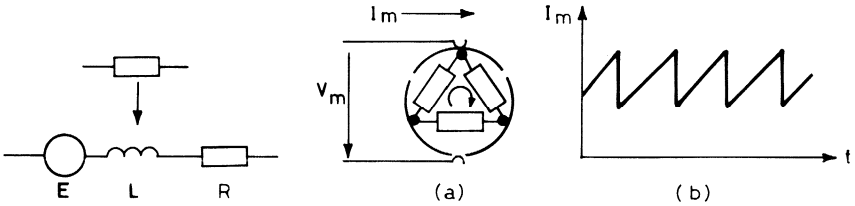
OPERATING PRINCIPLE

The TDA7272 novel applied solution is based on a tachometer control system without using such extra tachometer system. The information of the actual motor speed is extracted from the motor itself. A DC motor with an odd number of poles generates a motor current which contains a fixed number of discontinuitues within each rotation. (6 for the 3 pole motor example on Fig. 1)

Deriving this inherent speed information from the motor current, it can be used as a replacement of a low resolution AC tachometer system. Because the settling time of the control loop is limited on principle by the resolution in time of the tachometer, this control principle offers a poor reaction time for motors with a low number of poles. The realized circuit is extended by a second feed forward loop in order to improve such system by a fast auxiliary control path.

This additional path senses the mean output current and varies the output voltage according to the voltage drop across the inner motor resistance. Apart from a current averaging filter, there is no delay in such loop and a fast settling behaviour is reached in addition to the long term speed motor accuracy.

Fig. 1 - Equivalent of a 3 pole DC motor (a) and typical motor current waveform (b)



S-9494

BLOCK DESCRIPTION

The principle structure of the element is shown in Fig. 2. As to be seen, the motor speed information is derived from the motor current sense drop across the resistor R_S; capacitor CD together with the input impedance of 500Ω at pin 1 realizes a high pass filter.

This pin is internally biased at 20mV, each negative zero transition switches the input comparator. A 10mV hysteresis improves the noise immunity.

The trigger circuit is followed by an internal delay time differentiator.

Thus, the system becomes widely independent of the applied waveform at pin 1, the differentiator triggers a monostable circuit which provides a constant current duration. Both, output current magnitude and duration T, are adjustable by external elements CT and RT.

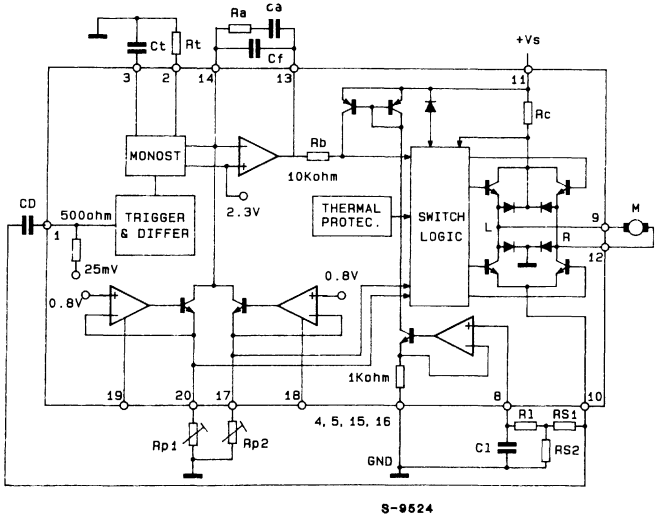
The monostable is retriggerable; this function prevents the system from fault stabilization at higher harmonics of the nominal frequency.

The speed programming current is generated by two separate external adjustable current sources. A corresponding digital input signal enables each current source for left or right rotation direction. Resistor RP1 and RP2 define the speed, the logical inputs are at pin 18 and 19.

At the inverting input (pin 14) of the main amplifier the reference current is compared with the pulsed monostable output current.

For the correct motor speed, the reference current matches the mean value of the pulsed monostable current. In this condition the charge of the feedback capacitor becomes constant.

Fig. 2 - Block diagram



The speed n of a k pole motor results:

$$n = \frac{10,34}{K\ CT\ R\ 17,20} \text{ (min -1)}$$

and becomes independent of the resistor RT which only determines the current level and the duty cycle which should be 1 : 1 at the nominal speed for minimum torque ripple.

The second fast loop consists of a voltage to current converter which is driven at pin 8 by the low pass filter R_L, C_L. The output current at this stage is injected by a PNP current mirror into the inner resistor R_B. So the driving voltage of the output stage consists of the integrator output voltage plus the fast loop voltage contribution across R_B.

The power output stage realizes different modes depending on the logic status at pin 18 and 19.

- Normal operation for left and right mode: each upper TR of the bridge is used as voltage follower whereas the lower acts as a switch.
- Stop mode where the upper half is open and the lower is conductive.
- High impedance status where all power elements are switched-off.

The high impedance status is also generated when the supply voltage overcomes the 5V to 20V operating range of when the chip temperature exceeds 150°C.

A short circuit protection limits the output current at 1.5A. Integrated diodes clamp spikes from the inductive load both at V_{CC} and ground.

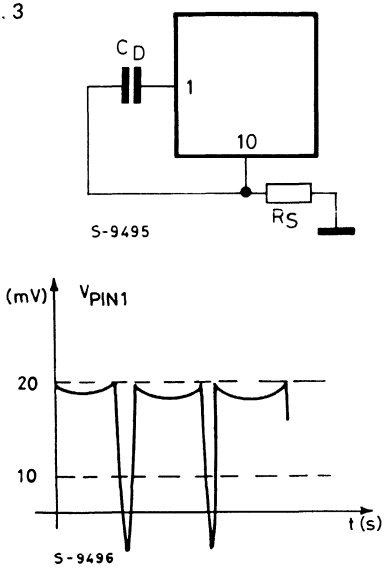
The reference voltages are derived from a common bandgap reference. All blocks are widely supplied by an internal 3.5V regulator which provides a maximum supply voltage rejection.

PIN FUNCTION AND APPLICATION INFORMATION

Pin 1

Trigger input. Receives a proper voltage which contains the information of the motor speed. The waveform can be derived directly by the motor current (Fig. 3). The external resistor generates a proper voltage drop. Together with the input resistance at pin 1 [R_{IN} (1) = 500Ω] the external capacitor C_D realize a high pass filter which differentiates the commutation spikes of the motor current. The trigger level is 0V.

Fig. 3

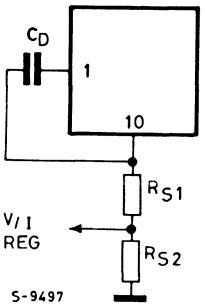


The biasing of the pin 1 is 20mV with a hysteresis of 10mV. So the sensing resistance must be chosen high enough in order to obtain a negative spike of the least 30mV on pin 1, also with minimum variation of motor current:

$$R_S \geqslant \frac{30mV}{\Delta I_{MOT}\ min.}$$

Such value can be too much high for the pre-regulation stage V-I and it could be necessary to split them into 2 series resistors $R_S = R_{S1} + R_{S2}$ (see fig. 4) as explained on pin 8 section.

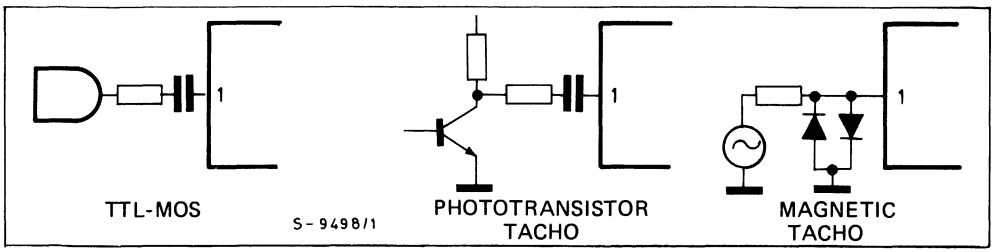
Fig. 4



The information can be taken also from an external tachogenerator. Fig. 5 shows various sources connections:

the input signal mustn't be lower than -0.7V.

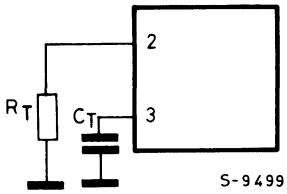
Fig. 5



Pin 2

Timing resistor. An internal reference voltage (V2 = 0.8V) gives possibility to fix by an external resistor (R_T), from this pin and ground, the output current amplitude of the monostable circuit, which will be reflected into the timing capacitor (pin 3); the typical value would be about 50μA.

Fig. 6



Pin 3

Timing capacitor. A constant current, determined by the pin 2 resistor, flowing into a capacitor between pin 3 and ground provides the output pulse width of the monostable circuit, the max voltage at pin 3 is fixed by an internal threshold: after reaching this value the capacitor is rapidly discharged and the pulse width is fixed to the value:

$$T_{on} = 2.88\ R_T\ C_T \quad \text{(Fig. 6)}$$

Pin 4

Not connected.

Pin 5

Ground. Connected with pins 6, 15, 16.

Pin 6

Ground. Connected with pins 5, 15, 16.

Pin 7

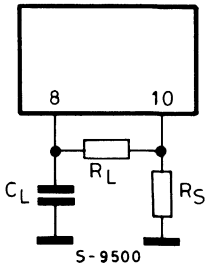
Not connected.

Pin 8

Input V/I loop. Receives from pin 10, through a low pass filter, the voltage with the information of the current flowing into the motor and produces a negative resistance output:

$$R_{out} = -9\ R_S \quad \text{(Fig. 7)}$$

Fig. 7



For compensating the motor resistance and avoiding instability:

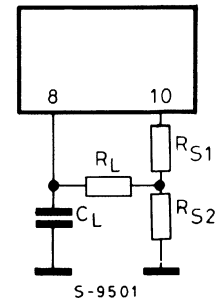
$$R_S \leqslant \frac{R_{MOTOR}}{9}$$

The optimization of the resistor R_S for the tachometric control must not give a voltage too high for the V/I stage: one solution can be to divide in two parts, as shown in Fig. 8, with:

$$R_{S2} = \frac{R_M}{10} \text{ and } R_{S1} + R_{S2} \geqslant$$

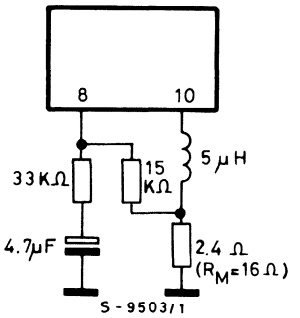
$$\geqslant \frac{30mV}{\Delta I \text{ mot min}} \quad \text{(see pin 1 sect.)}$$

Fig. 8



The low pass filter R_L, C_L must be calculated in order to reduce the ripple of the motor commutation at least 20dB. Another example of possible pins 10-8 connections is showed on Fig. 9. A choke can be used in order to reduce the radiation.

Fig. 9



Pin 9

Output motor left. The four power transistors are realized as darlington structures. The arrangement is controlled by the logic status at pins 18 and 19.

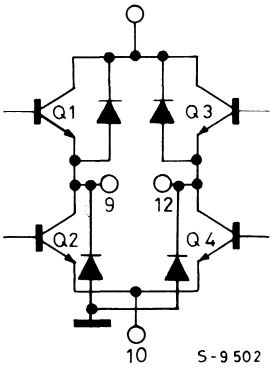
As before explained (see block description), in the normal left or right mode one of the lower darlington becomes saturated whereas the other remains open. The upper half of the bridge operates in the linear mode.

In stop condition both upper bridge darlingtons are off and both lower are on. In the high output impedance state the bridge is switched completely off.

Connecting the motor between pins 9 and 12 both left or right rotation can be obtained. If only one rotation sense is used the motor can be connected at only one output, by using only the upper bridge half. Two motors can be connected each at the each output: in such case they will work alternatively (See Application Section).

The internal diodes, together with the collector substrate diodes, protect the output from inductive voltage spikes during the transition phase (Fig. 10)

Fig. 10



Pin 10

Common sense output. From this pin the output current of the bridge configuration (motor current) is fed into R_S external resistor in order to generate a proper voltage drop.

The drop is supplied into pin 1 for tachometric control and into pin 8 for V/I control (See pin 1 and pin 8 sections).

Pin 11

Supply voltage.

Pin 12

Output motor right. (See pin 9 section)

Pin 13

Output main amplifier. The voltage on this pin results from the tachometric speed control and feeds the output stage.

The value of the capacitor C_F (Fig. 11), connected from pins 13 and 14, must be chosen low enough in order to obtain a short reaction time of the tachometric loop, and high enough in order to reduce the output ripple.

A compromise is reached when the ripple voltage (peak-to-peak) V_{ROP} is equal to 0.1 V_{MOTOR} :

$$C_F = 2.3 \frac{C_T}{V_{RIP}} \left(1 - \frac{R_T}{R_P}\right)$$

$$\text{with } V_{RIP} = \frac{V_{FEM} + I_{MOT} \cdot R_{MOT}}{10} \text{ and}$$

with duty cycle = 50%. (See pin 2-3 section)

Fig. 11

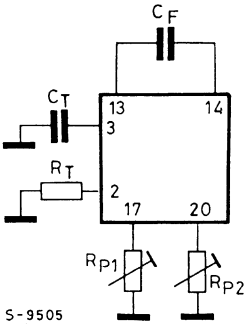
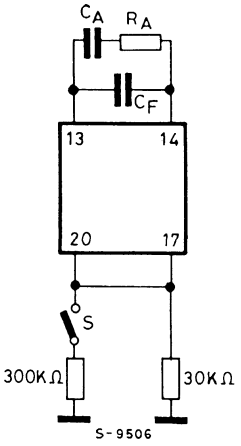


Fig. 12



In order to compensate the behaviour of the whole system regulator-motor-load (considering axis friction, load torque, inertias moment of the motor of the load. etc.) a RC series network is also connected between pins 13 and 14 (Fig. 12). The value of C_A and R_A must been chosen experimentally as follows:

– Increase of 10% the speed with respect to the nominal value by connecting in parallel to R_P a resistor with value about 10 time larger.

– Vary the R_A and C_A values in order to obtain at pin 13 a voltage signal with short response time and without oscillations. Fig. 13 shows the step response at pin 13 versus R_A and C_A values.

Fig. 13

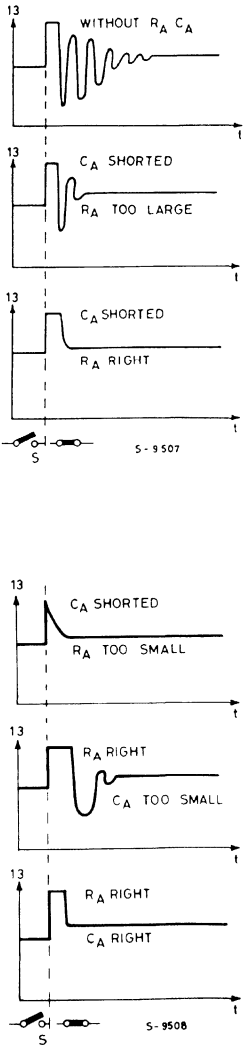
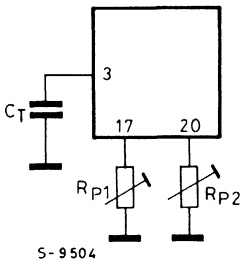


Fig. 14



Pin 14

Inverting input of main amplifier. In this pin the current reference programmed at pins 20, 17 is compared with the current from the monostable (stream of rectangular pulses).

In steady-state condition (constant motor speed) the values are equal and the capacitor C_F voltage is constant.

This means for the speed n (min -1) :

$$n = \frac{10.435}{C_T \ k \ R_P}$$

where "k" is the number of collector segments. (poles)

The non inverting input of the main amplifier is internally connected to a reference voltage (2.3V).

Pin 15

Ground.

Pin 16

Ground.

Pin 17

Left speed adjustment. The voltage at this pin is fixed to a reference value of 0.8V. A resistor from this pin and ground (Fig. 14) fixes the reference current which will be compared with the medium output current of the monostable in order to fix the speed of the motor at the programmed value. The correct value of R_P would be:

$$R_P = \frac{10.435}{C_T \cdot k \cdot n} =$$

n = motor speed, (min -1)
k = poles number

Fig. 15

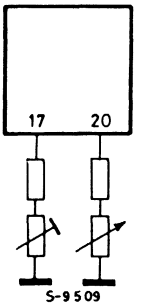


Fig. 16

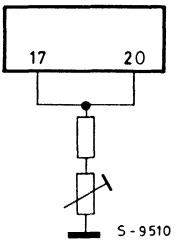


Fig. 17

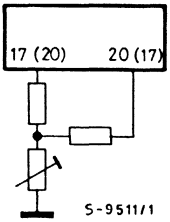
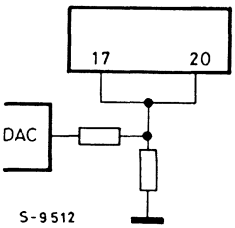


Fig. 18

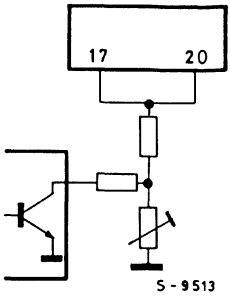


The control of speed can be done in different way:

- speed separately programmed in two senses of rotation (Figg. 14-15);
- only one speed for the two senses of rotation (Fig. 16);
- speeds of the two senses a bit different (i.e. for compensating different pulley effects) (Fig. 17);
- speed programmed with a DC voltage (Fig. 18) i.e. with DA converter;
- fast forward, by putting a resistor. In this case it is necessary that also at the higher speed for the duty cycle to be significatively less than 1 (see value of R_T, C_T on pin 2, pin 3 sections).

Fig. 19 shows the function controlled with a μP.

Fig. 19



Pin 18

Right function control. The voltages applied to this pin and to pin 19 determine the function, as showed in the table.

The typical value of the threshold (L-H) is 1.2V.

CONDITION		OUTPUT FUNCTION	OUTPUT VOLTAGE	
Pin 18	Pin 19		Pin 12	Pin 9
L	L	STOP	LOW	LOW
H	L	LEFT	LOW	REG
L	H	RIGHT	REG	LOW
H	H	OPEN	HIGH IMPEDANCE	

Pin 19

Left function control. (See pin 18 sect).

Pin 20

Right speed adjustment. (See pin 17 sect).

Fig. 20 - Typical application

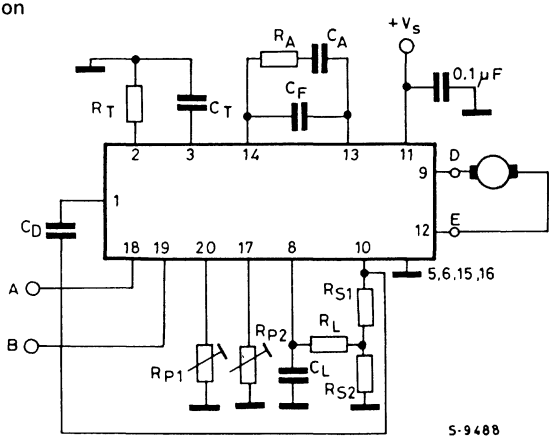


Fig. 21 - Tacho only speed regulation

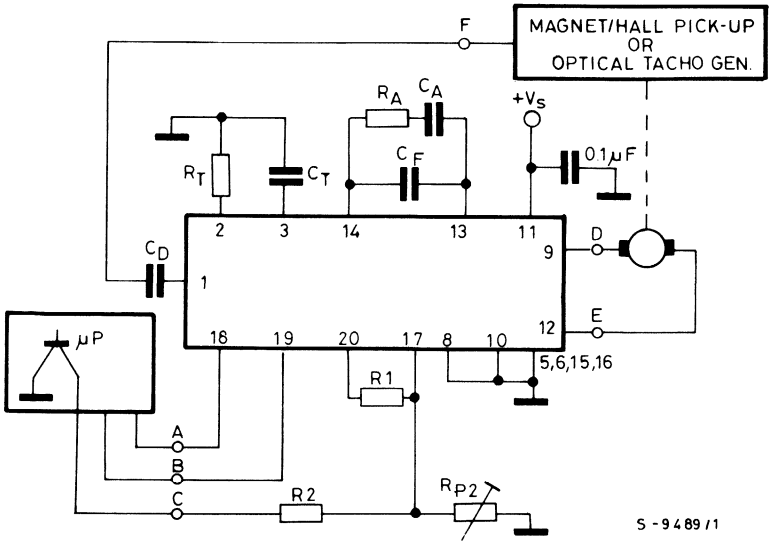


Fig. 22 - One direction reg. of one motor, or alternatively of two motors

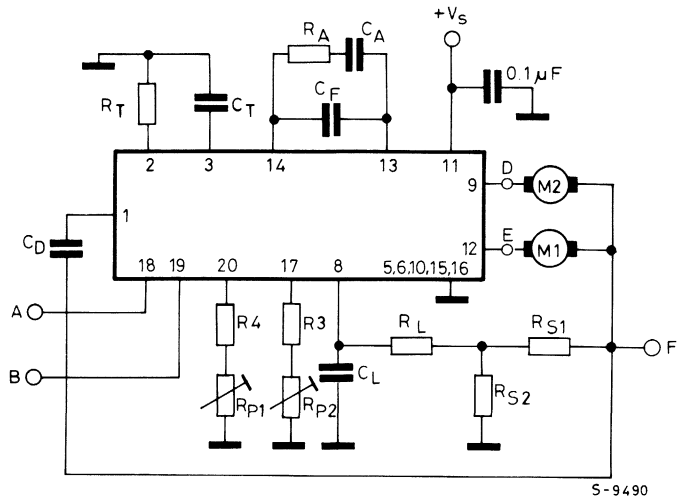
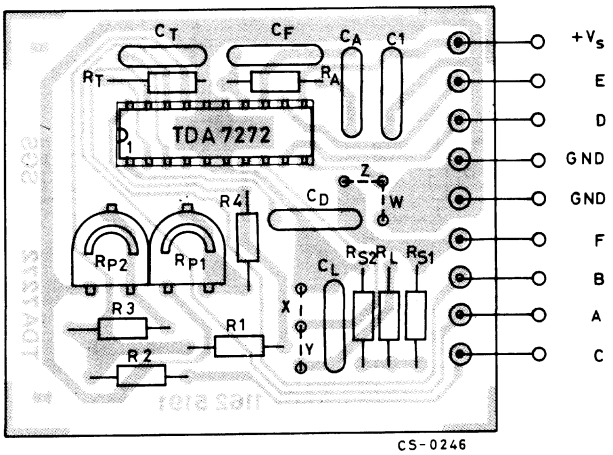


Fig. 23 - P.C. board and components layout of the circuits of Figg. 20, 21, 22



APPLICATION SUGGESTION (Fig. 20, 21, 22) - (For a 2000 r.p.m. 3 pole DC motor with $R_M = 16\Omega$)

Comp.	Recommended value	Purpose	If larger	If smaller	Allowed range	
					Min.	Max.
R_{S1}	1Ω	Current sensing tacho loop.		Tacho loop do not regulate.	0	
R_{S2}	1.5Ω	Curr. sensing V/I loop.	Instability may occur.	Motor regulator; undercompens.	0	$R_{MOT}/9$
R_L; C_L	22KΩ - 68nF	Spike filtering.	Slow V/I regulator response.	High output ripple.		
C_D	68nF	Pulse transf.			33nF	100nF
R_T; C_T	15KΩ - 47nF	Current source programming to obtain a 50% duty cycle.			6KΩ	30KΩ
R_{P1}; R_{P2}	47KΩ trim.	Set of speed.	Low speed.	High speed.	0	
C_F	Polyester 100nF	Optimization of integrator ripple and loop response time.	Lower ripple, slower tacho-regulator response.	Higher ripple, faster response.	10nF	470nF
R_A; C_A	220KΩ - 220nF	Fast response with no overshoot.	Depending on electromechanical system.		10KΩ 10nF	10MΩ 1μF

Fig. 24 - Speed regulation versus supply voltage (Circuit of Fig. 20)

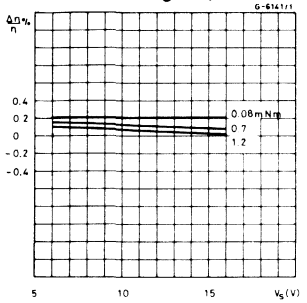


Fig. 25 - High current TDA7272 + 2 x L149 application

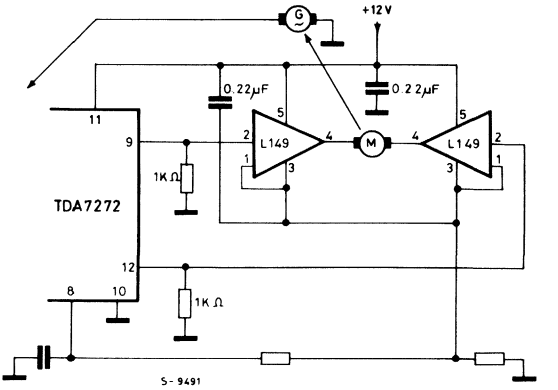
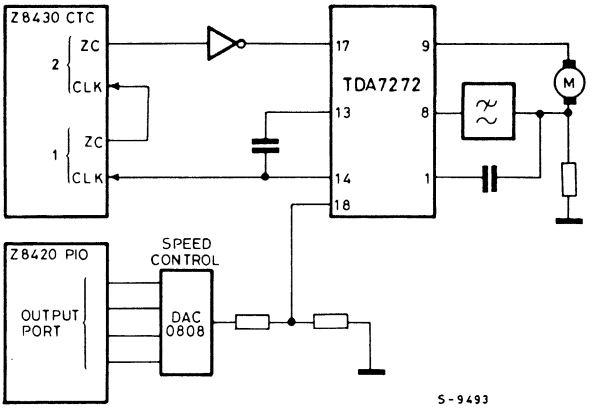


Fig. 26 - In connection with a presettable counter and I/O peripheral the TDA7272 controls the speed through a D/A converter



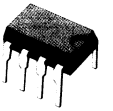
TDA7274

ADVANCE DATA

LOW-VOLTAGE DC MOTOR SPEED CONTROLLER

- WIDE OPERATING VOLTAGE RANGE (1.8 to 6V)
- BUILT-IN LOW-VOLTAGE REFERENCE (0.2V)
- LINEARITY IN SPEED ADJUSTMENT
- HIGH STABILITY VS. TEMPERATURE
- LOW NUMBER OF EXTERNAL PARTS

The TDA 7274 is a monolithic integrated circuit DC motor speed controller intended for use in microcassettes, radio cassette players and other consumer equipment. It is particulary suitable for low-voltage applications.



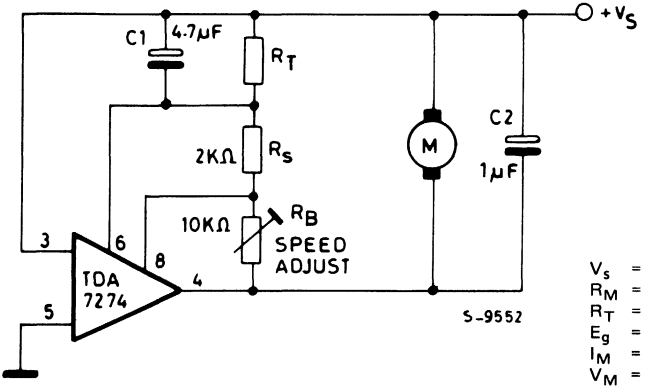
Minidip Plastic

ORDERING NUMBER: TDA 7274

ABSOLUTE MAXIMUM RATINGS

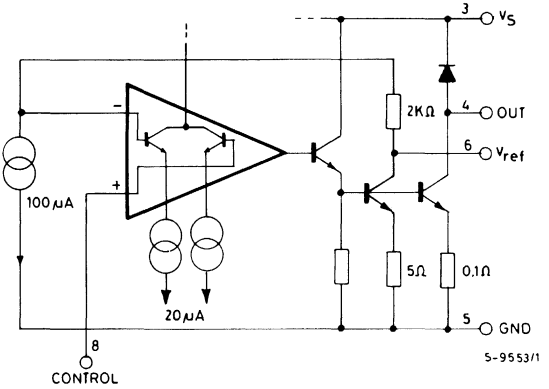
V_s	Supply voltage	6	V
I_M	Motor Current	700	mA
P_{tot}	Power dissipation at $T_{amb} = 25°C$	1.25	W
T_j, T_{stg}	Storage and junction temperature	-40 to +150	°C

APPLICATION CIRCUIT

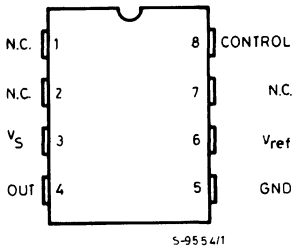


V_s = 3.0V
R_M = 4.9Ω
R_T = 220Ω
E_g = 1.65V
I_M = 100 mA
$V_M = R_M I_M + E_g$ = 2.14V

SCHEMATIC DIAGRAM



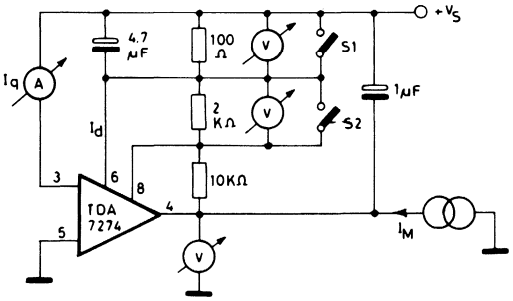
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

Fig. 1 - Test circuit



ELECTRICAL CHARACTERISTICS (Refer to test circuit, V_s = 3V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		1.8		6	V
V_{ref}	Reference voltage	I_M = 100mA	0.18	0.20	0.22	V
I_q	Qiescent current			2.4	6.0	mA
I_d (Pin 6)	Quiescent current			120		µA
K	Shunt ratio	I_M = 100mA	45	50	55	–
V_{sat}	Residual voltage	I_M = 100mA		0.13	0.3	V
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_s$	Line regulation	I_M = 100mA V_s = 1.8 to 6V		0.20		%/V
$\frac{\Delta K}{K} / \Delta V_s$	Voltage characteristic of shut ratio	I_M = 100mA V_s = 1.8 to 6V		0.80		%/V
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_M$	Load regulation	I_M = 20 to 200mA		0.004		%/mA
$\frac{\Delta K}{K} / \Delta I_M$	Current characteristic of shut ratio	I_M = 20 to 200mA		-0.03		%/mA
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	Temperature characteristic of reference voltage	I_M = 100mA T_{amb} = -20 to +60°C		0.04		%/°C
$\frac{\Delta K}{K} / \Delta T_{amb}$	Temperature characteristic of shut ratio	I_M = 100mA T_{amb} = 20 to +60°C		0.02		%/°C

Fig. 2 - Quiescent current vs. supply voltage

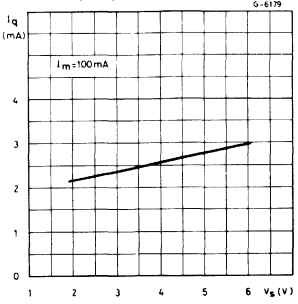


Fig. 3 - Reference voltage vs. supply voltage

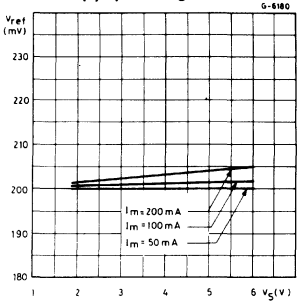


Fig. 4 - Shunt ratio vs. supply voltage

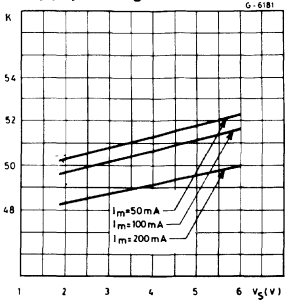


Fig. 5 - Reference voltage vs. load current

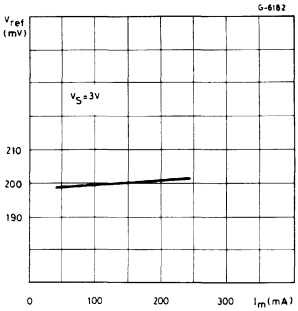


Fig. 6 - Shunt ratio vs. load current

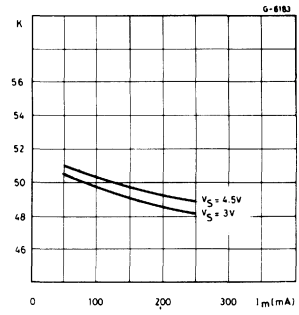


Fig. 7 - Minimum supply voltage (typical) vs. load current

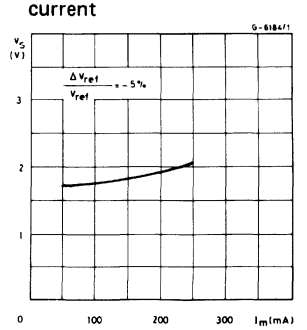


Fig. 8 - Saturation voltage vs. load current

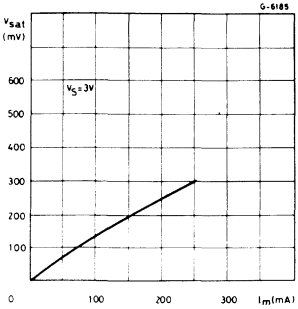


Fig. 9 - Quiescent current vs. ambient temperature

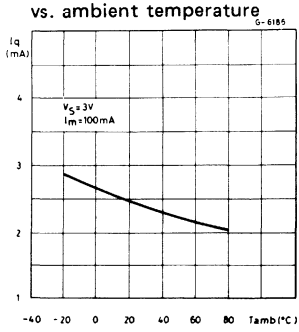


Fig. 10 - Reference voltage vs. ambient temperature

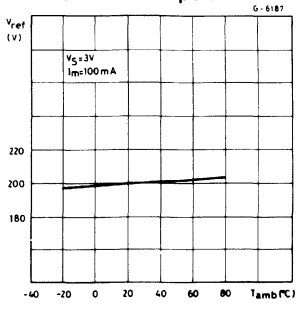


Fig. 11 - Application circuit

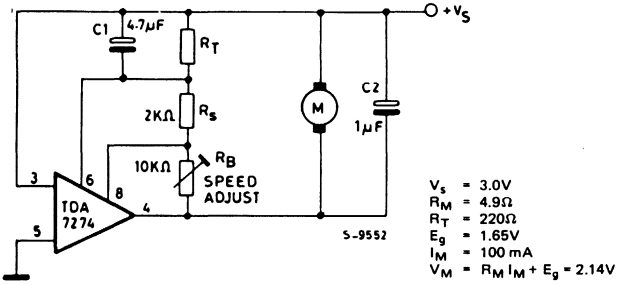


Fig. 12 - P.C. board and components layout of the circuit of fig. 11 (1 : 1 scale)

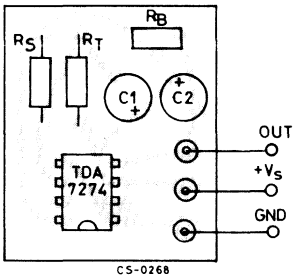


Fig. 13 - Speed variations vs. supply voltage

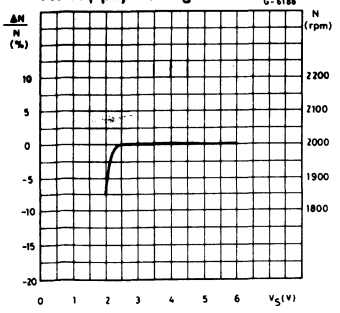


Fig. 14 - Speed variations vs. motor current

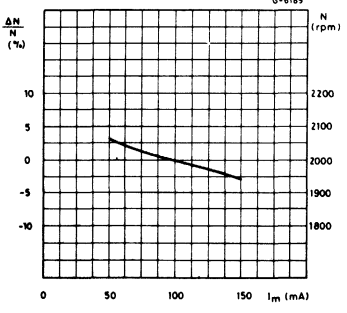
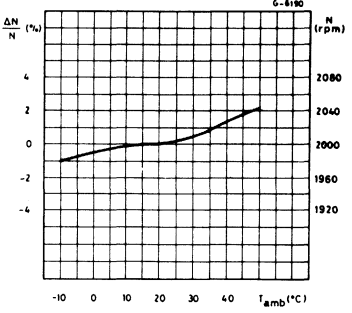
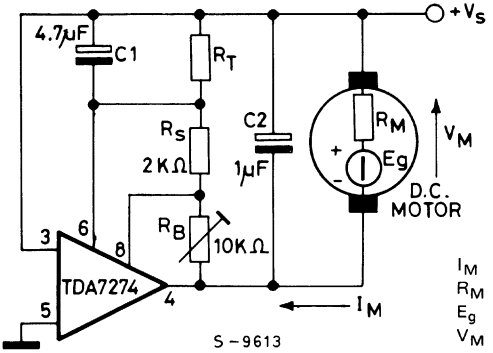


Fig. 15 - Speed variations vs. ambient temperature



APPLICATION INFORMATION

Fig. 16



I_M = Motor current at rated speed
R_M = Motor resistance
E_g = Back electromotive force
$V_M = I_M \cdot R_M + E_g$

$$E_g = R_T\, I_d + I_M\,(\frac{R_T}{K} - R_M) + V_{ref}$$

$$[1 + \frac{R_B}{R_S} + \frac{R_T}{R_S}\,(1 + \frac{1}{K})]$$

R_S has to be adjusted so that the applied voltage V_M is suitable for a given motor, the speed is then linearly adjustable varing R_B.

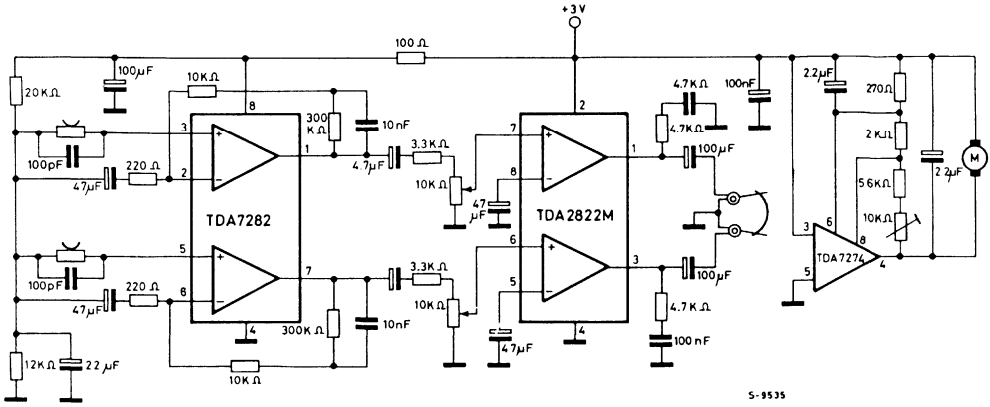
The value of R_T is calculated so that

$$R_{T\ (max.)} < K_{(min.)} \cdot R_{M\ (min.)}$$

If $R_{T\ (max.)} > K \cdot R_M$, instability may occur.

The values of C_1 (4.7 µF typ.) and C_2 (1 µF typ.) depend on the type of motor used. C_1 adjusts WOW and flutter of the system. C_2 suppresses motor spikes.

Fig. 17 - 3V stereo cassette miniplayer with motor speed control



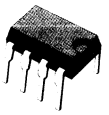
TDA7275

ADVANCE DATA

MOTOR SPEED REGULATOR

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (UP TO 1.5A)
- LOW QUIESCENT CURRENT
- LOW REFERENCE VOLTAGE (1.32V)
- EXCELLENT PARAMETERS STABILITY VERSUS AMBIENT TEMPERATURE
- START/STOP FUNCTION (TTL LEVELS)
- THERMAL PROTECTION
- DUMP PROTECTION

The TDA7275 is a linear integrated circuit in minidip plastic package. It is intended for use as speed regulator for DC motors of record players, tape and cassette recorders.
The dump protection make it particularly suitable for car radio applications.



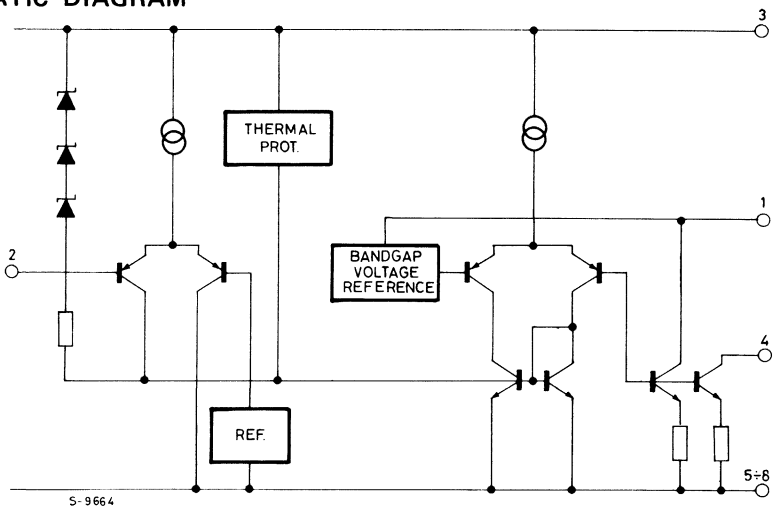
Minidip
(4 + 4)

ORDERING NUMBER: TDA7275

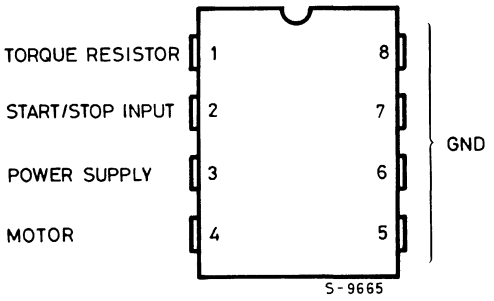
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	19	V
V_s	Peak supply voltage (for 50ms)	45	V
I_M	Maximum output current	1.5	A
T_{op}	Operating temperature range	-30 to 85	°C
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
	T_{pins} = 70°C	4	W

SCHEMATIC DIAGRAM



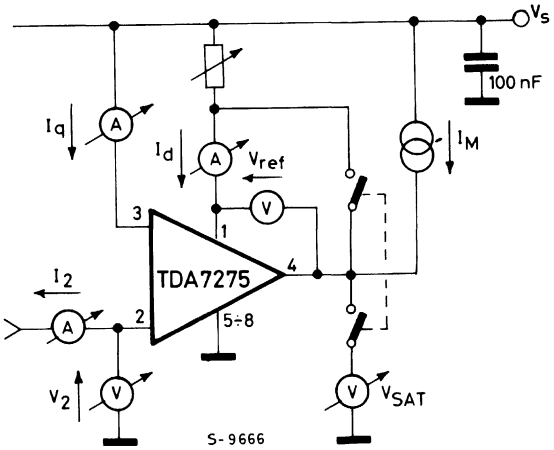
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W

Fig. 1 - Test circuit



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 12V unless otherwise specified, refer to test circuit)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		8		18	V
V_{ref}	Reference voltage	I_M = 0.1A	1.15	1.32	1.45	V
$I_q + I_d$	Total quiescent current	I_M = 0.1mA		2.5		mA
I_d	Quiescent current	I_M = 0.1mA		1.3		mA
I_{ms}	Starting motor current	$\frac{\Delta V_{ref}}{V_{ref}}$ = -50%	1			A
V_4	Saturation voltage	I_M = 0.5A		1.7	2	V
$K = I_M/I_T$	Reflection coefficient	I_M = 0.1A	18	20	22	V
$\frac{\Delta K/\Delta V_s}{K}$		I_M = 0.1A V_s = 8V to 16V		0.5		%/V
$\frac{\Delta K/\Delta I_M}{K}$		I_M = 25 to 200mA		-0.05		%/mA
$\frac{\Delta K/\Delta T}{K}$		I_M = 0.1A T_{op} = -30 to 85°C		0.02		%/°C
$\frac{\Delta V_{ref}/\Delta V_s}{V_{ref}}$	Line regulation	V_s = 8V to 16V I_M = 0.1A		-0.04		%/V
$\frac{\Delta V_{ref}/\Delta I_M}{V_{ref}}$	Load regulation	I_M = 25 to 200mA		-0.01		%/mA
$\frac{\Delta V_{ref}/\Delta T}{V_{ref}}$	Temperature coefficient	I_M = 0.1A T_{op} = -30 to 85°C		0.02		%/°C
V_2	Motor "Stop" (Acc. Following data or grounded)			1		V
I_2	Motor "Stop"	V_2 = 1V		-0.05		mA
V_2	Motor "Run" (Acc. following data or open			1.5		V
I_2	Motor "Run"	V_2 = 1.5V		-0.1		mA

Fig. 2 - Application circuit

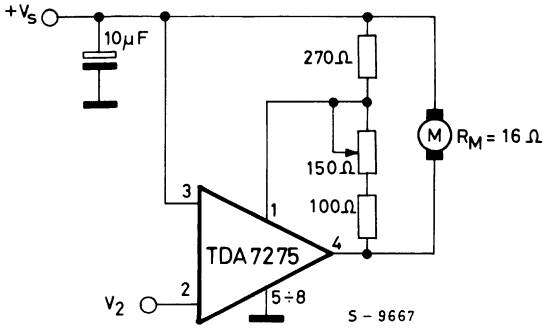


Fig. 3 - Quiescent current vs. supply voltage

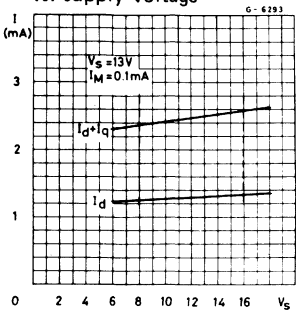


Fig. 4 - Reference voltage vs. supply voltage

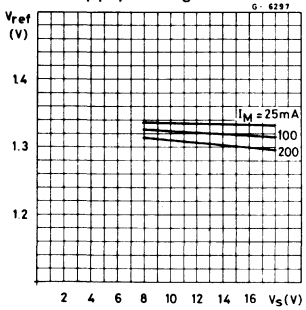


Fig. 5 - Reference voltage vs. load current

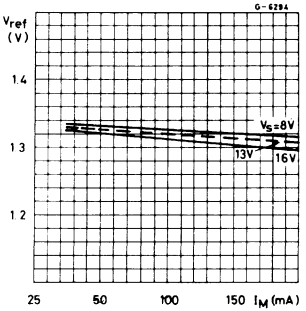


Fig. 6 - Reference voltage vs. temperature

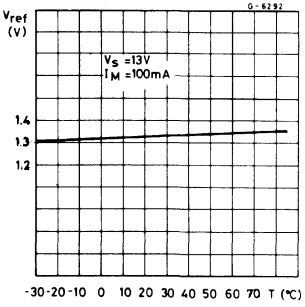


Fig. 7 - Shunt ratio vs supply voltage

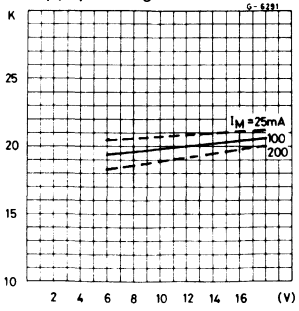


Fig. 8 - Shunt ratio vs. load current

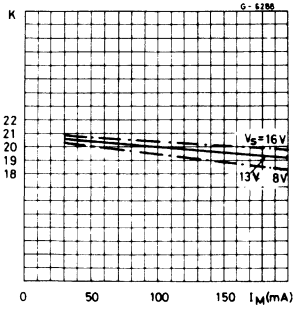


Fig. 9 - Shunt ratio vs. temperature

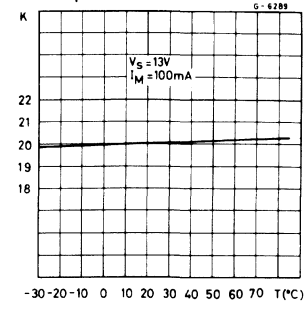


Fig. 10 - Saturation voltage vs. load current

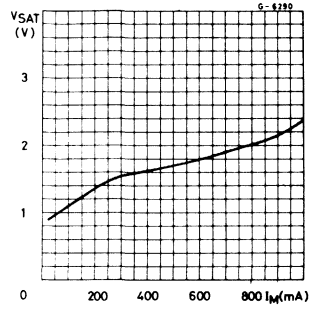


Fig. 11 - Speed variation vs. supply voltage

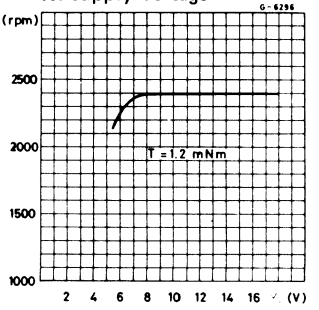
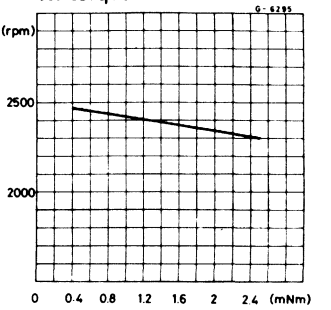


Fig. 12 - Speed variation vs. torque



TDA7276

ADVANCE DATA

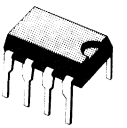
SPEED REGULATOR FOR SMALL DC MOTORS

The TDA7276 is a monolithic integrated circuit in 4 + 4 lead minidip plastic package designed for DC motors speed regulation in tape and cassette recorders, toys, etc.

It offers speed regulation versus supply voltage temperature and load changes better than conventional circuits built with discrete components.

Main features are:

- Excellent versatility in use
- High output current (up to 1A)
- Low reference voltage (1.25V)
- High temperature stability
- High power capability
- Low number of external parts



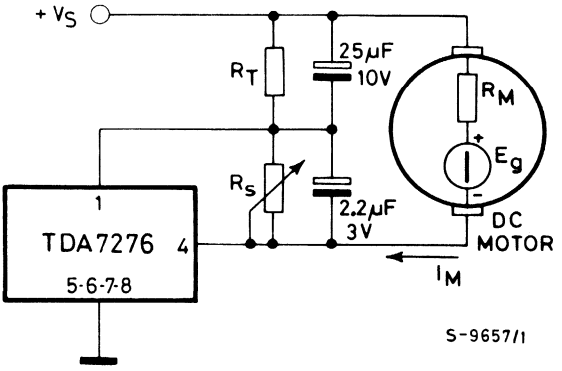
Minidip
(4 + 4)

ORDERING NUMBER: TDA7276

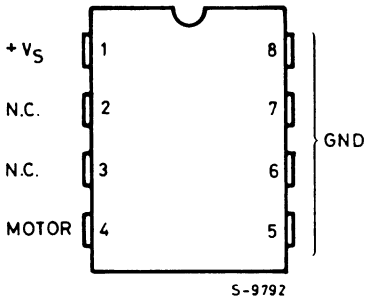
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Output current	1.2	A
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	1	W
P_{tot}	Total power dissipation at $T_{pins} = 70°C$	4	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT



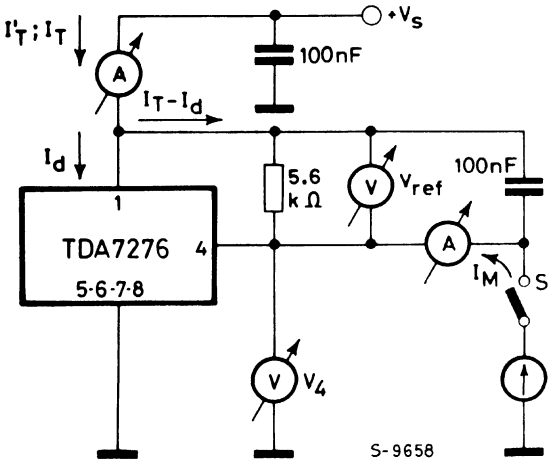
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb} = 25°C$, $V_s = 6V$)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{in}	Supply voltage range	$I_M = 0.1A$	$\Delta V_{ref}/V_{ref} = -5\%$	2.5		18	V
V_{ref}	Reference voltage (between pins 1 and 4)	$I_M = 0.1A$		1.1	1.25	1.35	V
I_d	Quiescent drain current	$I_M = 100\mu A$			1.1	2.1	mA
I_{MS}	Starting current	$V_s = 2.5V$	$\Delta V_{ref}/V_{ref} = -50\%$	0.5	0.8		A
I_{MS}	Starting current	$V_s = 5V$	$\Delta V_{ref}/V_{ref} = -50\%$	1.0			A
$K = I_M/I_T$	Reflection coefficient	$I_M = 0.1A$		18	20	22	–
$\frac{\Delta K}{K}/\Delta V_s$		$V_s = 6V$ to $18V$	$I_M = 0.1A$		0.45		%/V
$\frac{\Delta K}{K}/\Delta I_M$		$I_M = 25$ to $400mA$			0.005		%/mA
$\frac{\Delta K}{K}/\Delta T$		$T_{amb} = -20$ to $70°C$	$I_M = 0.1A$		0.02		%/°C
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$	Line regulation	$V_s = 6V$ to $18V$	$I_M = 0.1A$		0.02		%/V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$	Load regulation	$I_M = 25$ to $400mA$			0.009		%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$	Temperature coefficient	$T_{amb} = -20$ to $70°C$	$I_M = 0.1A$		0.02		%/°C

PRINCIPLE OF OPERATION

The device acts an emf speed regulator providing correction for the internal losses of the motor represents the device in its standard application; the voltage across R_S is kept constant by the IC and equal to $V_{ref} = 1.25V$ typ.

The current through the resistance R_T is:

$$I_{RT} = I_{RS} + I_d + \frac{I_M + I_{RS}}{K}$$

where:

$$I_{RS} = \frac{V_{ref}}{R_S}$$

I_d = quiescent drain current (1.1mA typ.)
I_M = motor current
K = reflection coefficient (20 typ.)

E_g being the motor's back electromotive force and R_M its internal resistance; the voltage across the motor itself will be:

$$E_g + R_M I_M = R_T I_{RT} + V_{ref}$$

therefore:

$$E_g = I_M \left(\frac{R_T}{K} - R_M\right) + V_{ref} \cdot$$

$$\cdot \left[\frac{R_T}{R_S}\left(1 + \frac{1}{K}\right) + 1\right] + R_T I_d$$

Motor's speed will be independent from resisting torque if E_g doesn't depend on I_M, then will do:

$R_T = K R_M$ (if $R_T > K_{min} R_{M\,min}$ oscillations may occur) - Back emf rated to the wanted speed can be selected acting to R_S - R_S variations will lead to an hyperbolic adjustment of the speed:

$$R_S = R_T \frac{V_{ref}(1 + 1/K)}{E_g - V_{ref} - R_T I_d}$$

TDA7282

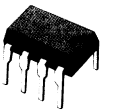
ADVANCE DATA

STEREO LOW VOLTAGE CASSETTE PREAMPLIFIER

- LOW ON/OFF POP NOISE
- LOW OPERATING VOLTAGE
- VERY LOW DISTORTION

The TDA7282 is a monolithic integrated circuit intended for stereo cassette players.

The TDA7282 is assembled in 8 leads plastic minidip.



Minidip Plastic

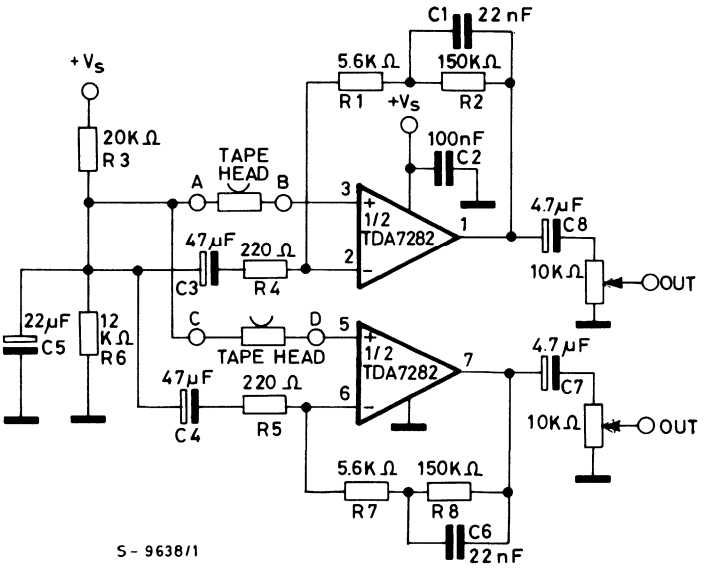
SO-8

ORDERING NUMBER: TDA7282 (Minidip)
TDA7282D (SO.8)

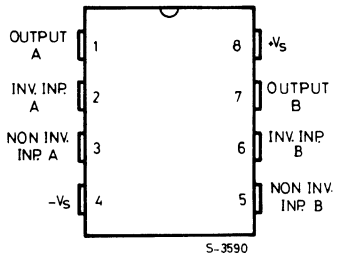
ABSOLUTE MAXIMUM RATINGS

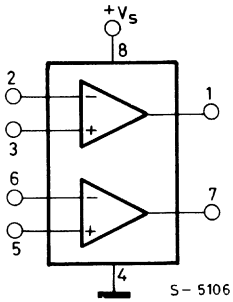
V_s	Supply voltage	10	V
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C
P_{tot}	Total power dissipation at T_{amb} = 70°C	400	mW

STEREO PREAMPLIFIER FOR CASSETTE PLAYERS

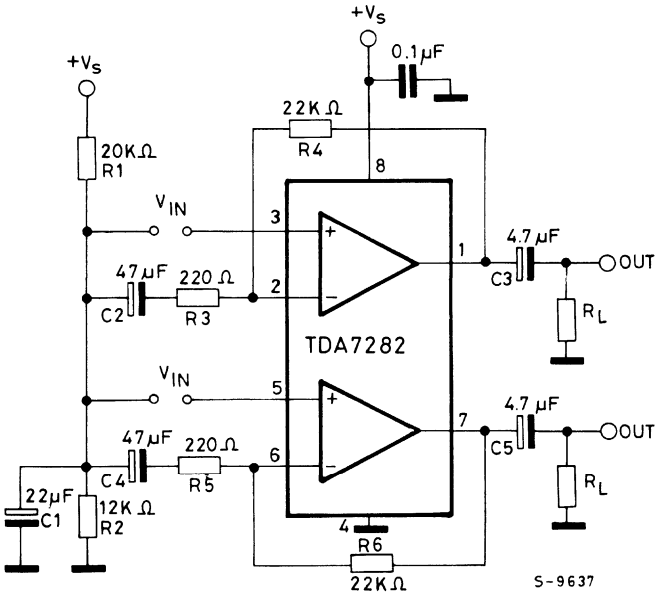


CONNECTION AND BLOCK DIAGRAM





TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 3V, T_{amb} = 25°C, f = 1KHz, G_v = 40dB, R_L = 10KΩ, R_s = 600Ω unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		1.8		9	V
I_d	Supply current			1.5	3	mA
I_b	Input bias current			280	500	nA
I_{os}	Input offset current			20		nA
V_{os}	Input offset voltage			0.5		mV
$V_{o\,DC}$	Quiescent voltage			1.1		V
V_o	Output voltage	THD = 1%	550	650		mV
THD	Total harmonic distortion f = 100Hz f = 1KHz f = 10KHz	 V_o = 300mV		 0.08 0.07 0.1	 0.5	 % % %
G_v	Open loop voltage gain	f = 1KHz	68	80		dB
G_v	Closed loop gain			40		dB
	Channel balance			0.5		dB
e_N	Total input noise voltage	B_W = 22KHz to 22KHz		1.5		μV
C_S	Channel separation	f = 1KHz V_o = 30mV		65		dB
SVR	Supply voltage rejection	f = 100Hz	36	45		dB
R_{IN}	Input resistance			100		KΩ
R_o	Output resistance			15		Ω

APPLICATION INFORMATION

Fig. 1 - Stereo preamplifier for cassette players

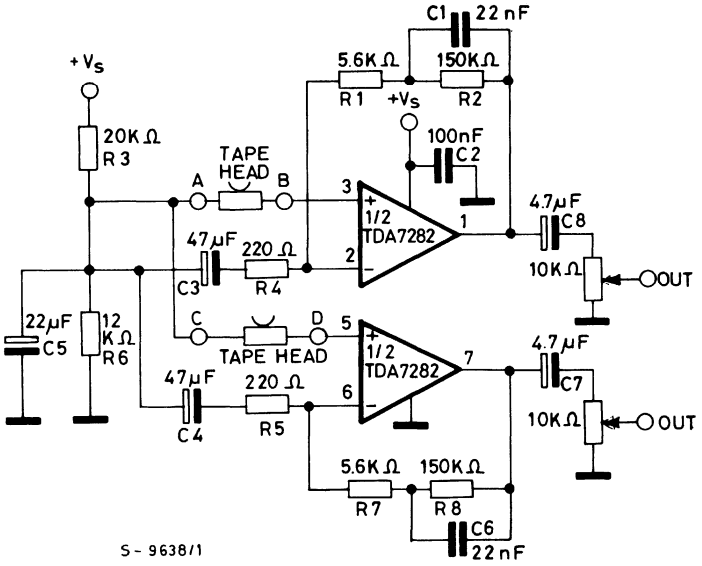
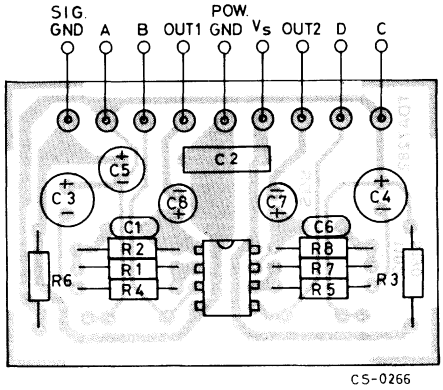


Fig. 2 - P.C and components layout of the circuit of Fig. 1 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Fig. 3 - Quiescent current vs. supply voltage

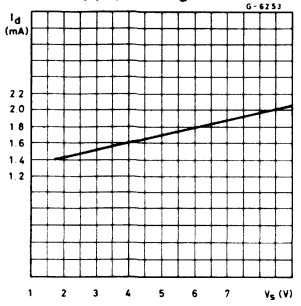


Fig. 4 - DC output voltage vs. supply voltage

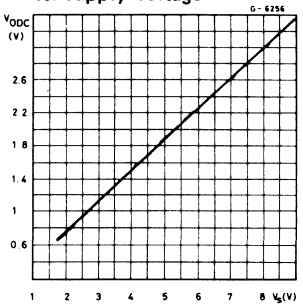


Fig. 5 - Input bias current vs. supply voltage

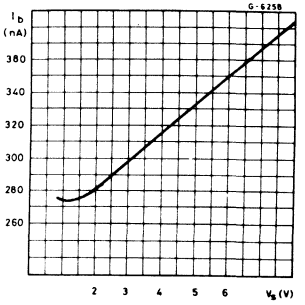


Fig. 6 - Distortion versus output level

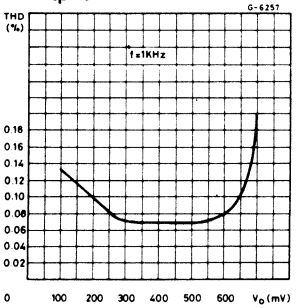


Fig. 7 - Distortion vs. frequency

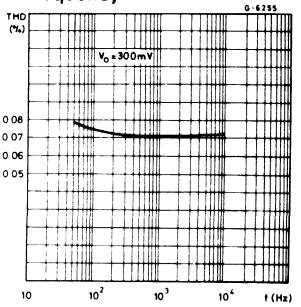


Fig. 8 - NAB response of the circuit of Fig. 1

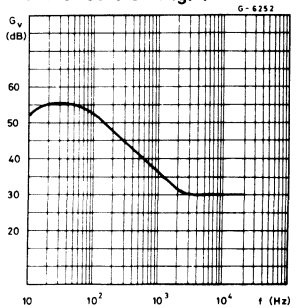


Fig. 9 - Supply voltage rejection vs. frequency

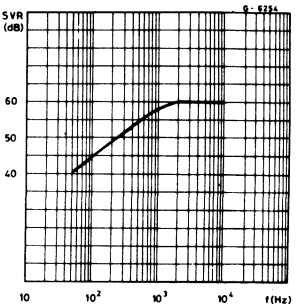
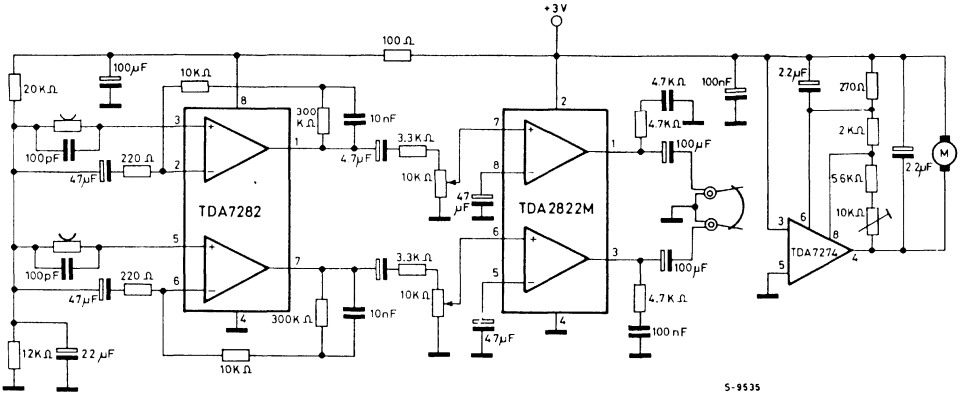


Fig. 10 - Stereo cassette player with motor speed control



TDA7300

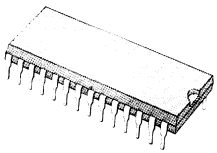
ADVANCE DATA

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- SINGLE SUPPLY OPERATION
- FOUR STEREO INPUT SOURCE SELECTION
- MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING

The TDA7300 is a volume, loudness, tone (bass and treble) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

Control is accomplished by serial bus microprocessor interface.
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.
The results are: low noise, low distortion and high dynamic range.



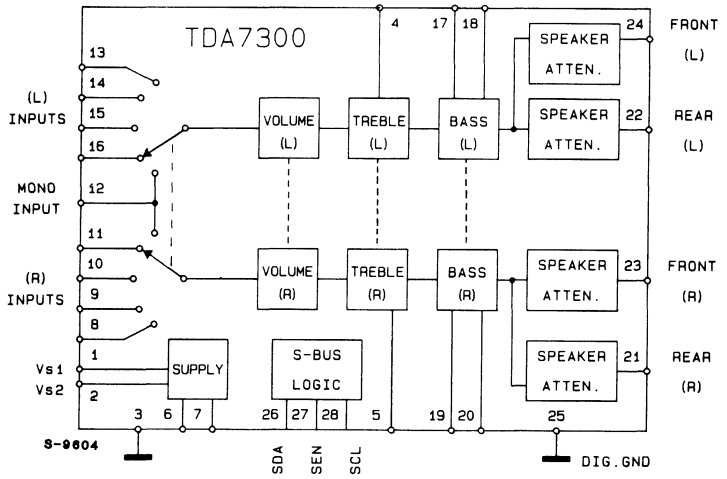
DIP-28 Plastic

ORDERING NUMBER: TDA 7300

ABSOLUTE MAXIMUM RATINGS

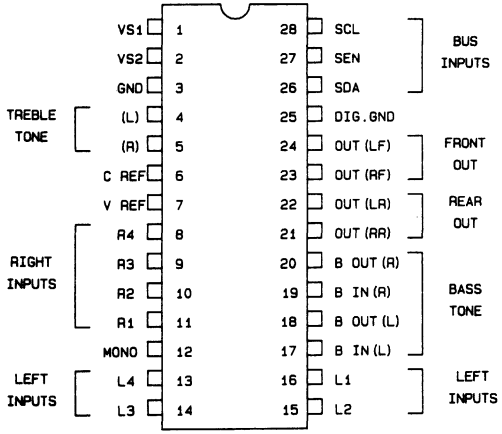
V_s	Supply voltage	18	V
P_{tot}	Total power dissipation (T_{amb} = 25°C)	2	W
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature	-55 to 150	°C

BLOCK DIAGRAM



TDA7300

CONNECTION DIAGRAM



S-9607

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max.	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_{s1} = 12V or V_{s2} = 8.5V; R_L = 10 KΩ; and R_g = 600Ω; f = 1 KHz unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY (1)						
V_{s1}	Supply voltage V_{s1}		10	12	16	V
V_{s2}	Supply voltage V_{s2}		6	8.5	10	V
I_s	Supply current			30		mA
V_{ref}	Reference voltage (pin 7)			4.3		V
SVR	Ripple rej. at V_{s1}	f = 300 Hz to 10 KHz	80			dB
SVR	Ripple rej. at V_{s2}	f = 300 Hz to 10 KHz	50			dB
INPUT SELECTORS						
R_i	Input resistance		30	50		KΩ
$V_{IN\ MAX}$	Input signal	G_v = 0 dB; d = 0.3%		1.8		VRMS
C_s	Channel separation	f = 1 KHz		96		dB
		f = 10 KHz		78		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
	Control range			78		dB
G_{max}	Max gain			10		dB
	Max attenuation			68		dB
	Step resolution			2		dB
	Attenuator set error	G_v = -50 to 10 dB			2	dB
	Tracking error				2	dB
SPEAKER ATTENUATORS						
	Control range			38		dB
	Step resolution			2		dB
	Attenuator set error				2	dB
	Tracking error				2	dB
BASS AND TREBLE CONTROL(2)						
	Control range			± 15		dB
	Step resolution			2.5		dB
AUDIO OUTPUT						
V_o	Output voltage	d = 0.3%		1.8		VRMS
R_L	Output load resistance		2			KΩ
C_L	Output load capacitance				1	nF
R_o	Output resistance			70	150	Ω
V_o (DC)	DC voltage level			3.5		V
GENERAL						
e_{No}	Output noise	G_v = 0 dB BW = 22 Hz to 22 KHz		6		μV
		G_v = 0 dB Curve A		4		μV
S/N	Signal to noise ratio	All gain = 0 dB V_o = 1VRMS BW= 22Hz to 22KHz		105		dB
d	Distortion	f = 1 KHz; V_o = 1V; G_v = 0		0.01		%
	Frequency response (-1 dB)	G_v = 0 dB High Low	20 30			KHz Hz
S_c	Channel separation left/right	f = 1 KHz f = 10 KHz		100 82		dB dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit

BUS INPUTS

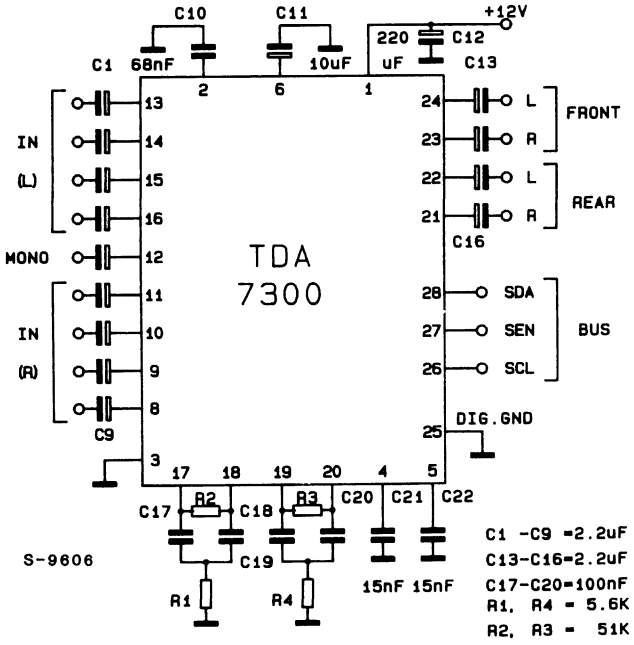
V_{iL}	Input LOW voltage				0.8	V
V_{iH}	Input HIGH voltage		2			V
V_o	Output voltage SDA acknowledge	I = 1.6 mA			0.4	V

Notes:

1) The circuit can be supplied either at V_{s1} or at V_{s2} without the use of the internal voltage regulator. The circuit also operate at a supply voltage V_{s1} lower than 10V. In this case the ripple rejection of V_{s2} is valid, because the voltage regulator saturates to about 0.8V.

2) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

Fig. 1 - Test circuit



APPLICATION INFORMATION

Fig. 2 - P.C. board and component layout of the circuit in Fig. 11 (1 : 1 scale)

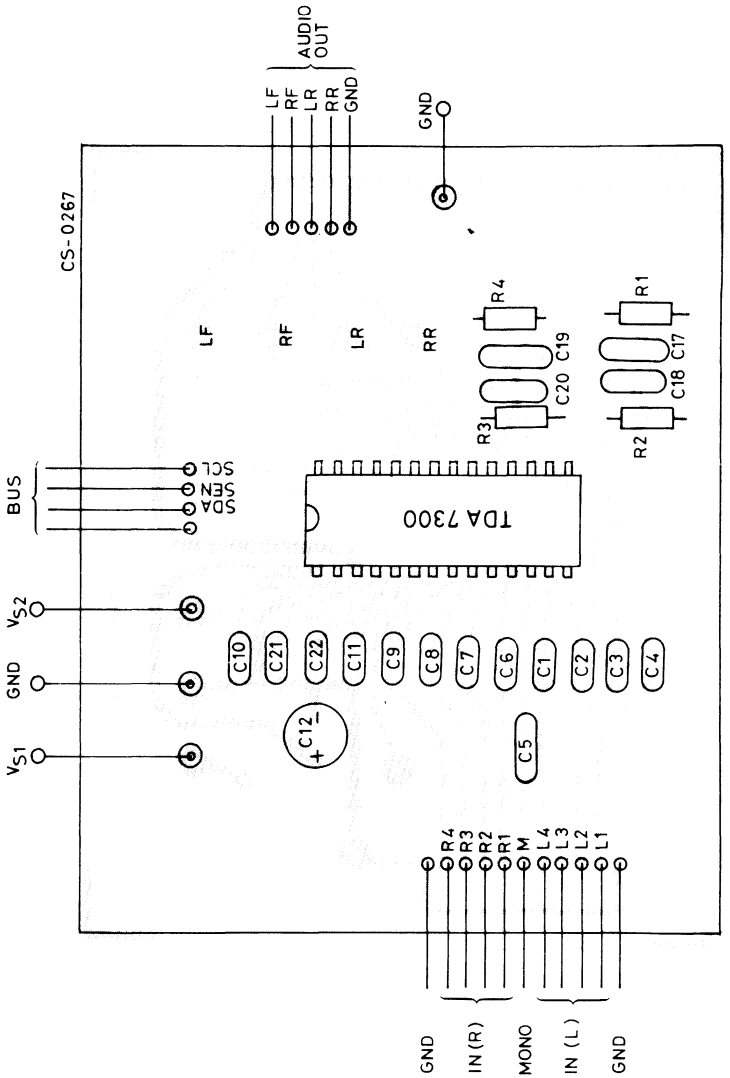


Fig. 3 - Total output noise vs. volume setting

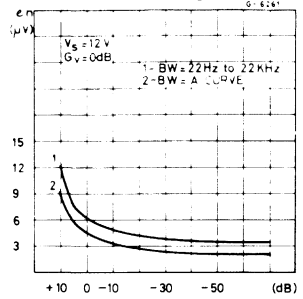


Fig. 4 - Signal to noise ratio vs. volume setting

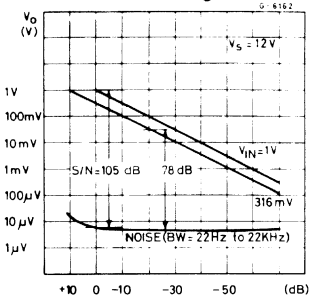


Fig. 5 - Distortion + noise vs. frequency

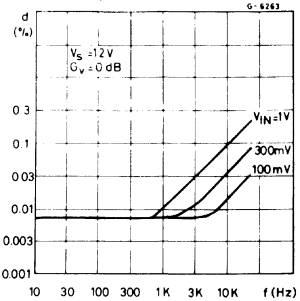


Fig. 6 - Distortion vs. output voltage

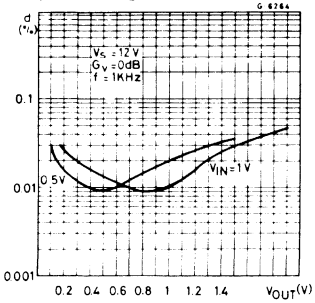


Fig. 7 - Distortion vs. load resistance

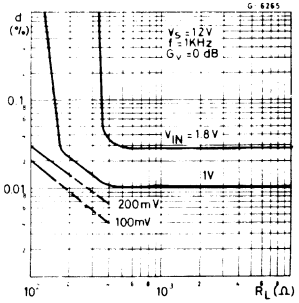


Fig. 8 - Channel separation (L1 - R1) vs. frequency

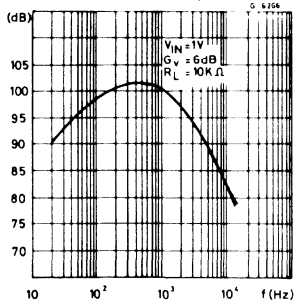


Fig. 9 - Channel separation (L1 - L2) vs. frequency

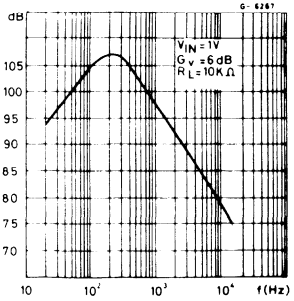


Fig. 10 - Supply voltage rejection (V_{S1}) vs. frequency

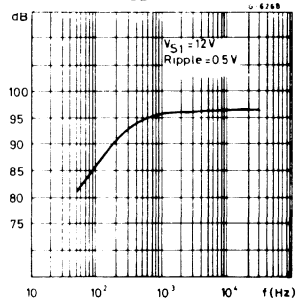


Fig. 11 - Supply voltage rejection (V_{S2}) vs. frequency

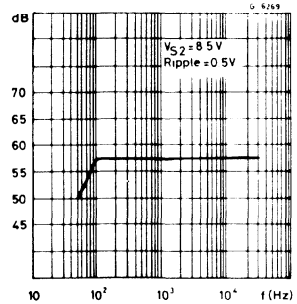


Fig. 12 - Supply voltage rejection versus V_{S1}

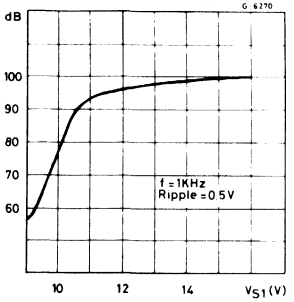


Fig. 13 - Supply voltage rejection versus V_{S2}

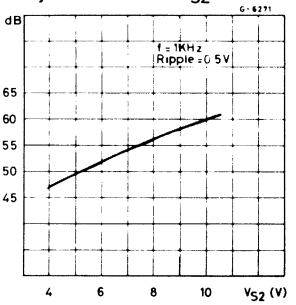


Fig. 14 - Clipping level (V_{rms}) vs. supply voltage

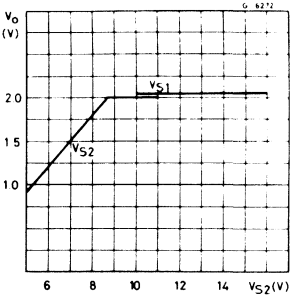


Fig. 15 - Quiescent current vs. supply voltage

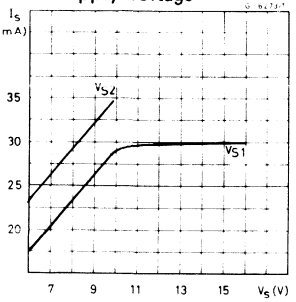


Fig. 16 - Quiescent current vs. temperature

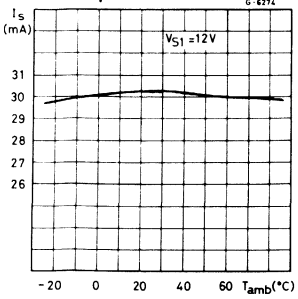
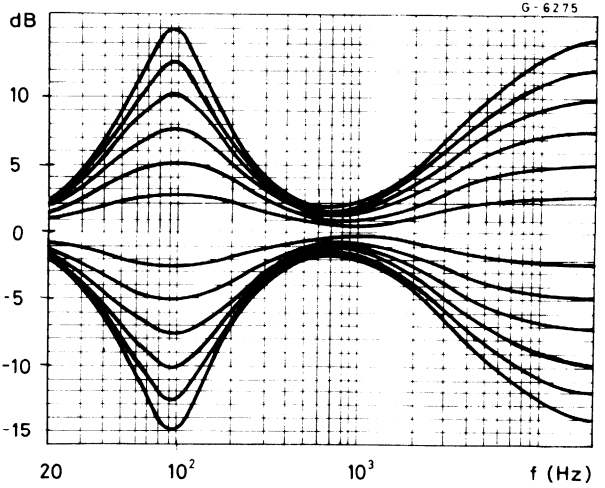
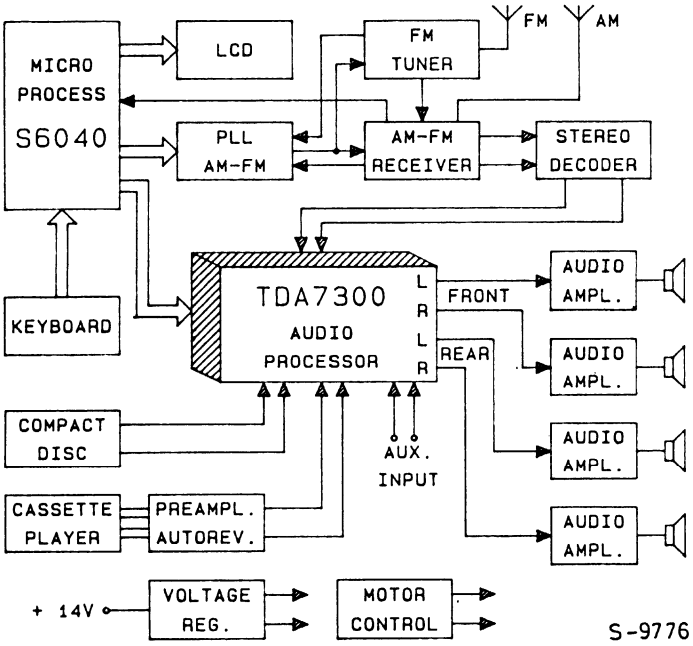


Fig. 17 - Typical tone response



APPLICATION INFORMATION (continued)

Fig. 18 - Complete car-radio system using digital controlled audio processor.



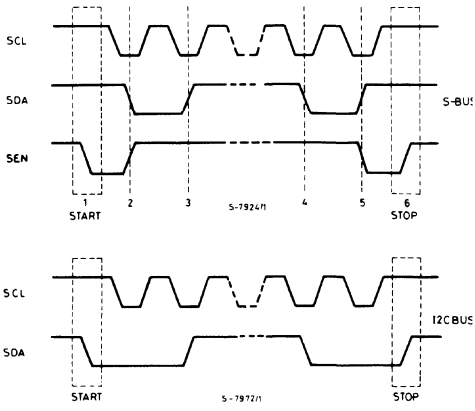
SERIAL BUS INTERFACE

S-BUS Interface and I2CBUS Compatibility

Data transmission from microprocessor to the TDA7300 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7300 appears as a standard I2CBUS slave.

In this case the S6040 μP can be programmed to generate the two different transmission systems: the S-BUS using the three lines of the serial bus, and the I2CBUS using the SCL and SDA lines only.

Fig. 19 - Timing Diagram of S-BUS and I2CBUS



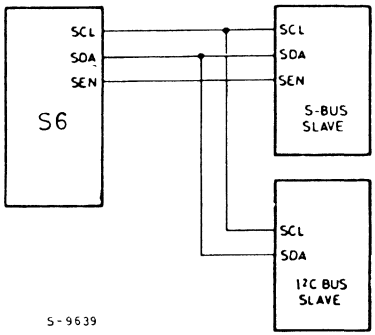
APPLICATION INFORMATION (continued)

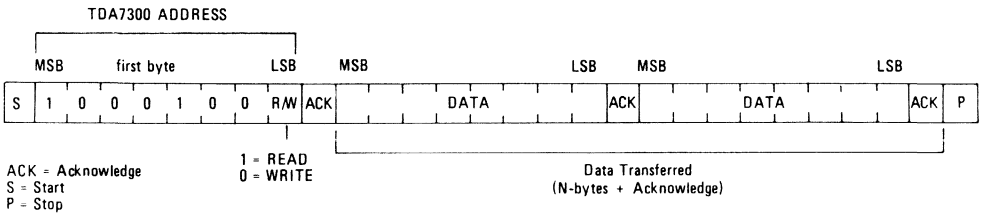
Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7300 address and the direction of the transmission on the BUS (this information is given in the 8th bit of the byte: "0" means "write", that is from the master to the slave, while "1" means "read"). The TDA7300 must always acnowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

Fig. 20 - System with Mixed S-BUS Peripherals





SOFTWARE SPECIFICATION

Chip address (TDA7300 address)

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care
Ax = 2dB steps
Bx = 10dB steps
Cx = 2.5dB steps

Status after power-on-reset

Volume	-68dB
Speaker	-38dB
Audio switch	Mono
Bass	+2.5dB
Treble	+2.5dB

NOTE - Using S6 is it necessary an external EPROM (M2716 F6X) previously programmed. Further information is available in S6 μP data sheet.

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB				LSB			
0 0	B2	B1	B0	A2	A1	A0	Volume 2dB steps
				0	0	0	0
				0	0	1	- 2
				0	1	0	- 4
				0	1	1	- 6
				1	0	0	- 8
				1	0	1	Not allowed
				1	1	0	Not allowed
				1	1	1	Not allowed
0 0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
	0	0	0				+ 10
	0	0	1				0
	0	1	0				- 10
	0	1	1				- 20
	1	0	0				- 30
	1	0	1				- 40
	1	1	0				- 50
	1	1	1				- 60

For example if you want setting the volume at -32dB the 8 bit string is : 0 0 1 0 0 0 0 1

Speaker attenuators

MSB		LSB				
1 0	0	B1	B0	A2	A1	A0	Speaker LF
1 0	1	B1	B0	A2	A1	A0	Speaker RF
1 1	0	B1	B0	A2	A1	A0	Speaker LR
1 1	1	B1	B0	A2	A1	A0	Speaker PR
				0	0	0	0
				0	0	1	- 2
				0	1	0	- 4
				0	1	1	- 6
				1	0	0	- 8
				1	0	1	Not allowed
				1	1	0	Not allowed
				1	1	1	Not allowed
		0	0				0
		0	1				- 10
		1	0				- 20
		1	1				- 30

For example attenuation of 24dB on speaker RF is giving by:
1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

Audio Switch- Select the input channel to activate

MSB					LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Stereo 4
			X	X	1	0	0	Mono
			X	X	1	0	1	Not allowed
			X	X	1	1	0	Not allowed
			X	X	1	1	1	Not allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string may be : 0 1 0 0 0 0 0 1

Bass and Treble - Control range of ±15dB (boost and cut) steps of 2.5dB

0 1 1 0 0 1 1 1	C3 C2 C1 C0 C3 C2 C1 C0	Bass Treable
	0 0 0 0	- 15
	0 0 0 1	- 15
	0 0 1 0	- 12.5
	0 0 1 1	- 10
	0 1 0 0	- 7.5
	0 1 0 1	- 5
	0 1 1 0	- 2.5
	0 1 1 1	- 0
	1 1 1 1	+ 0
	1 1 1 0	+ 2.5
	1 1 0 1	+ 5
	1 1 0 0	+ 7.5
	1 0 1 1	+ 10
	1 0 1 0	+ 12.5
	1 0 0 1	+ 15
	1 0 0 0	+ 15

C3 = Sign

For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

TDA7320

ADVANCE DATA

AM/FM CAR RADIO SYSTEM

The TDA7320 is high performance AM/FM radio IC designed for use in a wide range of car radio and home radio applications, operating with a supply voltage from 7 to 12V. The TDA7320 is supplied in a 20 pin plastic DIP package.

AM SECTION

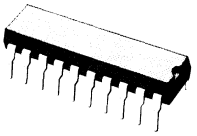
- WB balanced RF amplifier
- Double balanced mixer
- Balanced detector
- Level controlled oscillator
- Oscillator booster for digital tuning
- Field strength meter

FM SECTION

- IF balanced amplifier and limiter
- Quadrature detector
- Field strength meter and AFC outputs
- Adjustable interstation noise mute

FEATURES

- Soft AM/FM switching μP compatible
- High recovered audio signal
- Very good AM signal handling
- Suitable for capacitance, varicap and inductive tuning (SW included)
- Low crossmodulation
- Very low tweet



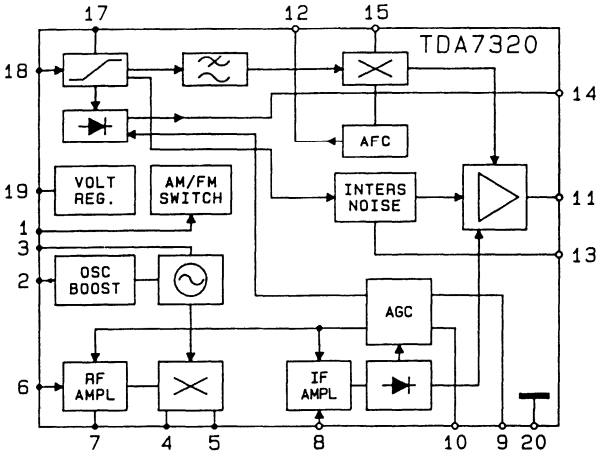
DIP-20 Plastic
(0.4)

ORDERING NUMBER: TDA7320

ABSOLUTE MAXIMUM RATINGS

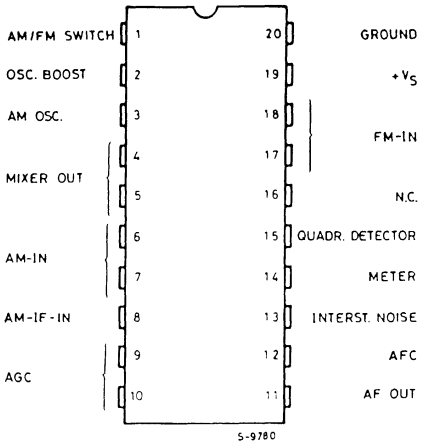
V_s	Supply voltage	14	V
P_{tot}	Total power dissipation at $T_{amb} < 85°C$	0.8	W
T_{op}	Operating temperature	-30 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

BLOCK DIAGRAM



TDA7320

CONNECTION DATA
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_s = 8.5V unless otherwise specified)

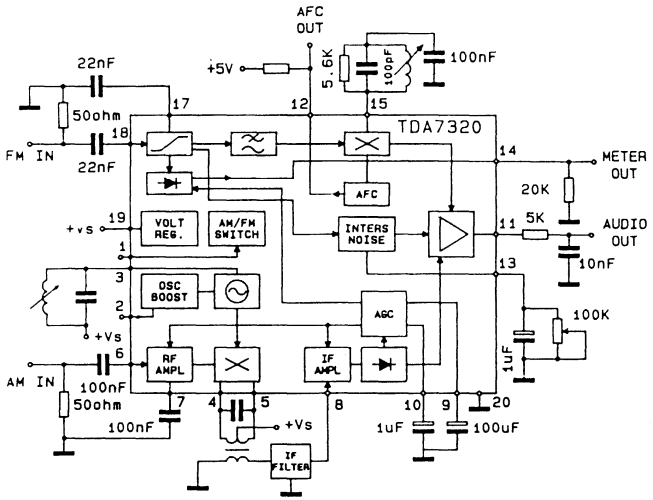
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		7		12	V
I_d	Current drain AM FM			30 30		mA
AM SECTION (f_o = 1MHz; f_m = 1KHz)						
V_i	Input sensitivity	S/N = 26dB m = 0.3		12	30	μV
S/N	Signal to noise	V_i = 1mV m = 0.3	48	50		dB
ΔV_i	AGC range	ΔV_{out} = 10dB m = 0.8		90		dB
V_o	Recovered audio signal	V_i = 1mV m = 0.3	90	150	220	mV
d	Distortion	V_i = 1mV m = 0.3		0.4		%
V_h	Max input signal handling capability	d = 3% m = 0.8	90			dBμV
R_i	Input resistance			6		KΩ
C_i	Input capacitance			18		pF
R_o	Output resistance				1	KΩ
	Tweet 2 IF	V_i = 1mV m = 0.3		38		dB
	Tweed 3 IF			40		
	AM Oscillator out	R_L = 150Ω		0.2		V
	IF Rejection			40		dB
V_M	Field meter output	V_i = 12μV		0.7		V
		V_i = 1mV		3.2		

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
FM SECTION (f_o = 10.7MHz; f_m = 1KHz)						
V_i	Input limiting voltage	-3dB limiting point		30		μV
AMR	Amplitude modulation reject.	f = 22.5KHz V_i = 3mV m = 0.3		50		dB
S/N	Signal to noise	f = 22.5KHz V_i = 1mV	60	68		dB
d	Distortion	f = 75KHz V_i = 1mV f = 22.5KHz V_i = 1mV		0.8 0.25		%
V_o	Recovered audio	f = 22.5KHz V_i = 1mV	110	150	220	mV
R_i	Input resistance			5		KΩ
C_i	Input capacitance			14		pF
R_o	Output resistance				1	KΩ
	Frequency detuning of AFC output with R = 10KΩ	from -3dB lim. point to 10mV			10	KHz
	Interstation noise output variation (*)			9		dB
V_m	Field meter output	V_i = 100μV V_i = 100mV		1.2 4.5		V V

(*) No input signal. Input connection to ground by 50Ω than 330Ω.

Fig. 1 - Test circuit



TDA7322

ADVANCE DATA

AM/FM CAR RADIO SYSTEM

The TDA7322 is high performance AM/FM radio IC designed for use in a wide range of car radio and home radio applications, operating with a supply voltage from 7 to 12V. The TDA7322 is supplied in a 20 pin plastic DIP package.

AM SECTION

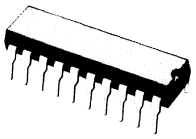
- WB balanced RF amplifier
- Double balanced mixer
- Balanced detector
- Level controlled oscillator
- Oscillator booster for digital tuning
- Field strength meter

FM SECTION

- IF balanced amplifier and limiter
- Quadrature detector
- Field strength meter and AFC outputs
- Adjustable interstation noise mute

FEATURES

- Soft AM/FM switching μP compatible
- High recovered audio signal
- Very good AM signal handling
- Suitable for capacitance, varicap and inductive tuning (SW included)
- Low crossmodulation
- Very low tweet



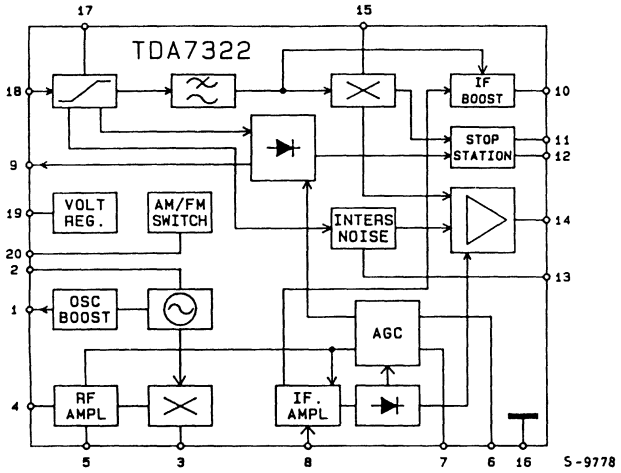
DIP-20 Plastic (0.4)

ORDERING NUMBER: TDA7322

ABSOLUTE MAXIMUM RATINGS

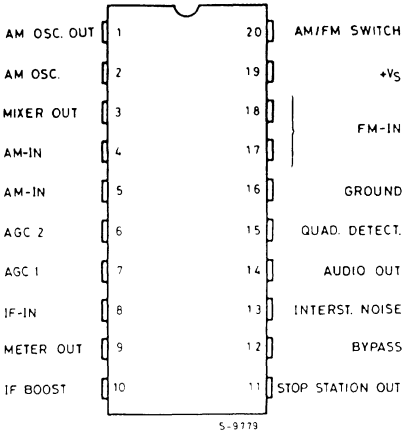
V_s	Supply voltage	14	V
P_{tot}	Total power dissipation at $T_{amb} < 85°C$	0.8	W
T_{op}	Operating temperature	-30 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-56 to 150	°C

BLOCK DIAGRAM



TDA7322

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_s = 8.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		7		14	V
I_d	Current drain AM FM			30 30		mA

AM SECTION (f_o = 1MHz; f_m = 1KHz)

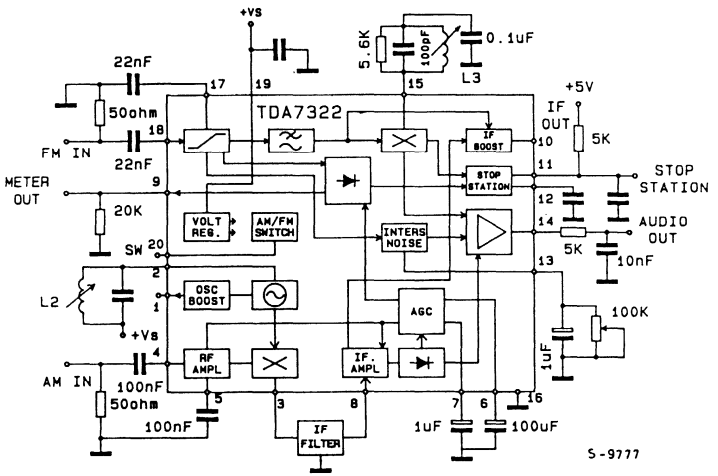
V_i	Input sensitivity	S/N = 26dB m = 0.3		12	30	μV
S/N	Signal to noise	V_i = 1mV m = 0.3		50		dB
ΔV_i	AGC range	ΔV_{out} = 10dB m = 0.8		90		dB
V_o	Recovered audio	V_i = 1mV m = 0.3	90	150	220	mV
d	Distortion	V_i = 1mV m = 0.3		0.4		%
V_H	Max input signal handling	d = 3% m = 0.8	90			dBμV
R_i	Input resistance			6		KΩ
C_i	Input capacitance			18		pF
R_o	Output resistance				1	KΩ
	Tweet 1 IF	V_i = 1mV m = 0.3		38		dB
	Tweed 3 IF			40		
	AM Oscillator out	R_L = 150Ω		200		mV
	IF Rejection			40		dB
	IF Output	R_L = 150Ω		100		mV
V_M	Field meter output	V_i = 12μV		0.7		V
		V_i = 1mV		3.8		

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
FM SECTION (f_o = 10.7MHz, f_m = 1KHz)						
V_i	Input limiting voltage	-3dB limit. point		30		μV
AMR	Amplitude modulation reject.	f = 22.5KHz V_i = 3mV m = 0.3		52		dB
S/N	Signal to noise	f = 22.5KHz V_i = 1mV	60	65		dB
d	Distortion	f = 75KHz V_i = 1mV f = 22.5KHz V_i = 1mV		0.8 0.25		% %
V_o	Recovered audio	f = 22.5KHz V_i = 1mV	110	150	220	mV
R_i	Input resistance			5		KΩ
C_i	Input capacitance			14		pF
R_o	Output resistance				1	KΩ
	Frequency detuning of AFC output with R = 10KΩ	From -3dB lim. point to 10mV			10	KHz
	Interstation noise output variation (*)			9		dB
IF	Output	R_L = 150Ω		100		mV
	Stop detuning			± 20		KHz
V_m	Field meter output	V_i = 100μV V_i = 100mV		1.2 4.5		V

(*) No input signal. Input connection to ground by 50Ω than 330Ω.

Fig. 1 - Test circuit



TDA7359

ADVANCE DATA

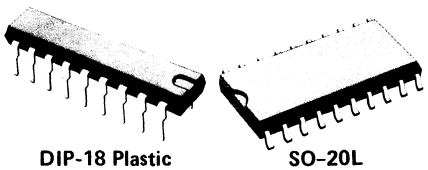
LOW VOLTAGE NBFM IF SYSTEM

- OPERATION FROM 1.8V TO 9V
- LOW DRAIN CURRENT (4mA, V_s = 4V)
- HIGH SENSITIVITY (-3dB INPUT LIMITING AT 3μV)
- 8μV INPUT FOR 20dB S/N
- LOW EXTERNAL FAIR COUNT

The TDA7359 is a low-power narrow band FM IF demodulation system operable to less than 2V supply voltage.

The device includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Op. Amp., Squelch, Scan Control and Mute Switch.

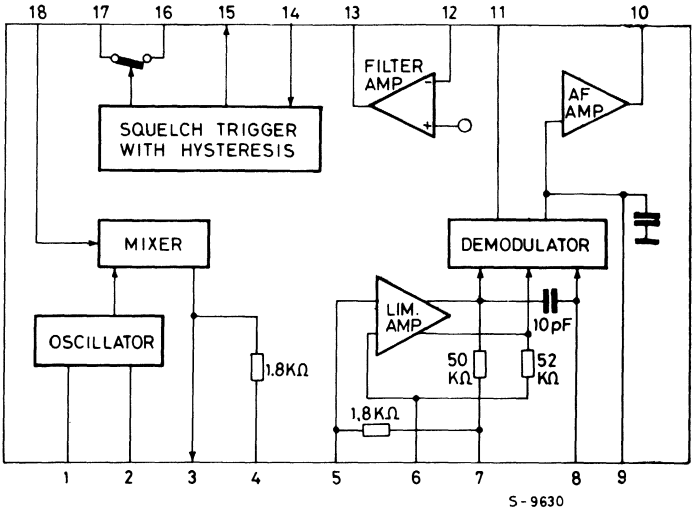
The TDA7359 is designed for use in NBFM dual conversion communication equipments using a 455KHz ceramic filter like cordless telephones, walkie-talkies, scan receivers, etc.



DIP-18 Plastic SO-20L

ORDERING NUMBERS: TDA7359 (DIP-18)
TDA7359D (SO-20L)

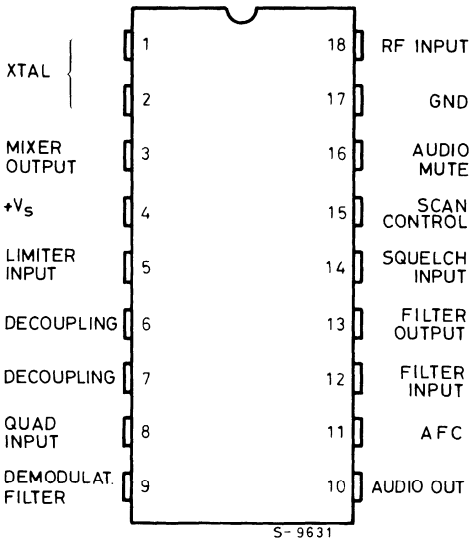
BLOCK DIAGRAM (PIN. NUMBERS are for DIP-18)



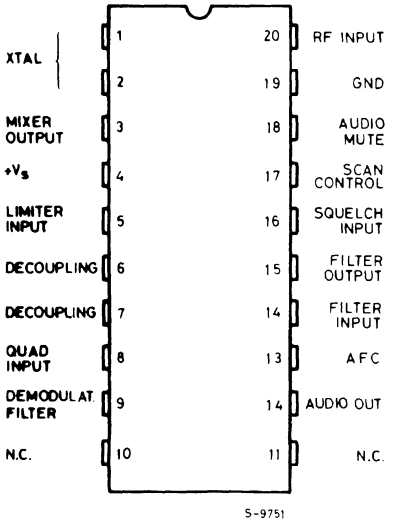
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9	V
V_I	RF input voltage (pin 18)	1	V_{rms}
V_8	Detector input voltage	1	V_{PP}
V_{14}	Mute function voltage	-0.5 to 5	V
T_{op}	Operating ambient temperature	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-65 to 150	°C

CONNECTION DIAGRAMS
(Top view)



DIP-18



SO-20L

THERMAL DATA			DIP-18	SO-20L
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100°C/W	200°C/W

PIN FUNCTION (DIP-18)

N°	NAME	FUNCTION
1-2	XTAL OSCILLATOR	Connections for the Colpitts XTAL oscillator. The XTAL may be replaced by an inductor (see fig. 5) if the application does not require high stability.
3	MIXER OUT	The Mixer is double balanced to reduce spurious products. The output impedance is 1.8KΩ to match the input impedance of a 455KHz ceramic filter.
4	SUPPLY VOLTAGE	Must be well decoupled with a 100nF ceramic capacitor.
5	IF LIMITER INPUT	Input pin of the six stages amplifier with about 50μV limiting sensitivity and 1.8KΩ input impedance. The if output is connected to the external quadrature coil (pin 8) via an internal 10pF capacitor.
6-7	DECOUPLING	Good quality 100nF ceramic capacitors and a suitable layout are important.
8	QUADRATURE COIL	A quadrature detector is used to demodulate the 455KHz FM signal. The Q of the quad coil has direct effect on output level and distortion (see fig. 6). For proper operation the voltage should be $100mV_{rms}$.
10	AUDIO OUTPUT	The Audio signal after detection and deemphasis is buffered by an internal emitter follower.
11	AFC OUT	AFC output, with high gain and high output impedance. If not needed, it should be grounded or connected to pin 9 (to double the recovered audio).
12 13	OP AMP. INPUT OP AMP. OUTPUT	Because of the low DC bias, the swing on the operational amplifier output is limited to $550mV_{rms}$. This can be increased by adding a resistor from the operational amplifier input to ground.
14 15 16	SQUELCH INPUT SCAN CONTROL MUTE	The Squelch trigger circuit with a low bias on the input (pin 14) will force pin 15 high; and pin 16 Low. Pulling pin 14 above mute threshold (0.65V) will force pin 15 to an impedance of about 60KΩ to ground and pin 16 will be an open circuit. An hysteresis of about 50mV at pin 12 will effectively prevent jitter.
17	GND	Ground connection.
18	10.7MHz MIXER INPUT	Input of the wide-band mixer. Normally used as 10.7MHz/455KHz converter, it can be also used with input frequencies up to 60MHz.

ELECTRICAL CHARACTERISTICS ($V_s = 4V$; $f_o = 10.7MHz$; $f = \pm 3KHz$; $f_m = 1KHz$; $T_{amb} = 25°C$; unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		1.8	4	9	V
I_s	Supply current	Squelch OFF Squelch ON		3.8 4.7		mA
V_i	Input quieting voltage	S/N = 20dB		8		μV
V_i	Input limiting voltage	-3dB limiting		3		μV
V_o	Recovered audio output	V_i = 10mV		150		mV_{rms}
V_{10}	Detector output voltage			1.5		V_{DC}
R_{10}	Detector output impedance			400		Ω
	Detector center frequency slope			150		mV/KHz
G_v	Operating amplifier gain	f = 10KHz $G_v = V_{13}/V_{12}$	40	55		dB
V_{13}	Operating amplifier output voltage			1.5		V_{DC}
I_B	Op. Amp. input bias current	Pin 10		20		nA
V_T	Trigger hysteresis			50		mV
R_m	Mute switching impedance	LOW		50		Ω
		HIGH		10		MΩ
V_{15}	Scan voltage	pin 14 HIGH (2V) pin 14 LOW (0V)	 3.0	0 3.4	0.5	V_{DC}
G_c	Mixer converter gain			30		dB
R_i	Input resistance			3.3		KΩ
C_i	Input capacitance			2.2		pF

Fig. 2 - Test circuit

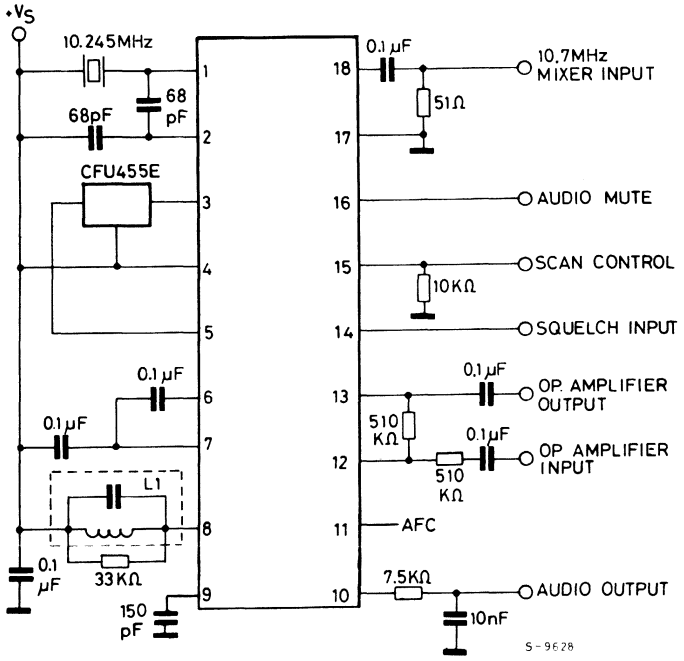


Fig. 3 - Supply current vs. supply voltage

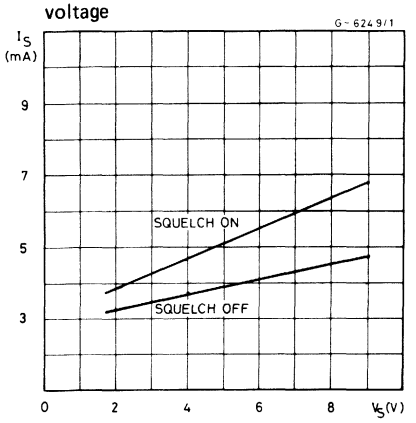


Fig. 4 - FM IF characteristics

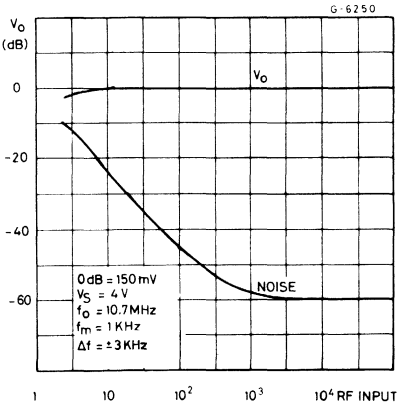


Fig. 5 - Colpitts XTAL oscillator

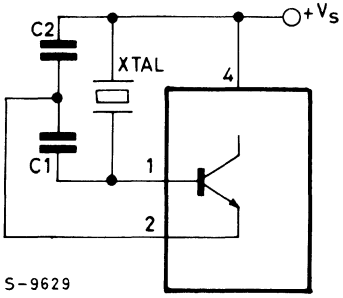
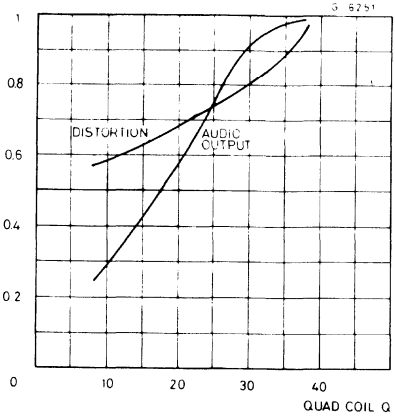


Fig. 6 - Effect of quadrature coil "Q" on audio level and distortion



TDA7361

ADVANCE DATA

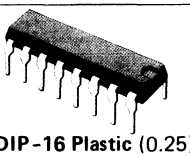
LOW VOLTAGE NBFM IF SYSTEM

- OPERATION FROM 1.8V TO 9V
- LOW DRAIN CURENT (4mA, V_s = 4V)
- HIGH SENSITIVITY (-3dB INPUT LIMITING AT 3μV)
- 8μV INPUT FOR 20dB S/N
- LOW EXTERNAL FAIR COUNT

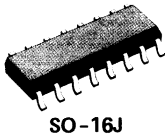
The TDA7361 is a low-power narrow band FM IF demodulation system operable to less than 2V supply voltage.

The device includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Op. Amp. Squelch, Scan Control and Mute Switch.

The TDA7361 is designed for use in NBFM dual conversion communication equipments using a 455KHz ceramic filter like cordless telephones, walkie-talkies, scan receivers, etc.



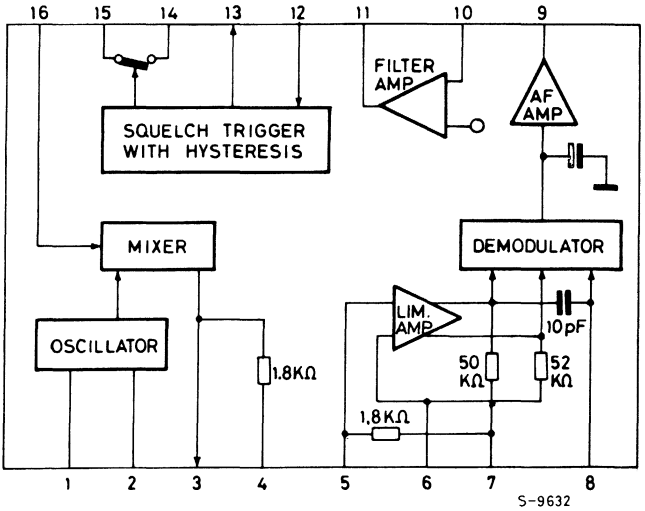
DIP-16 Plastic (0.25)



SO-16J

ORDERING NUMBERS: TDA7361 (DIP-16)
TDA7361D (SO-16)

BLOCK DIAGRAM

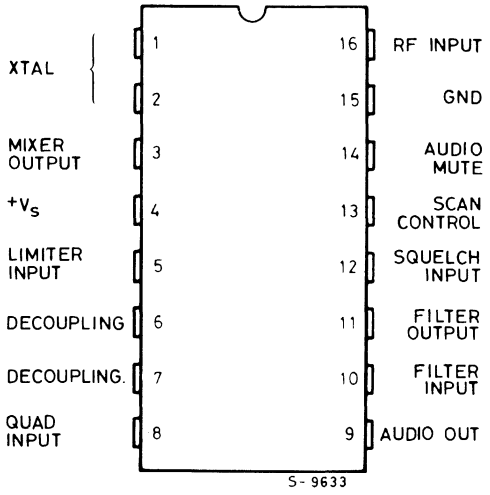


TDA7361

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9	V
V_I	RF input voltage (pin 16)	1	V_{rms}
V_8	Detector input voltage	1	V_{pp}
V_{14}	Mute function voltage	-0.5 to 5	V
T_{op}	Operating ambient temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

			DIP-16	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100°C/W	200°C/W

PIN FUNCTION

N°	NAME	FUNCTION
1-2	XTAL OSCILLATOR	Connections for the Colpitts XTAL oscillator. The XTAL may be replaced by an inductor (see fig. 5) if the application does not require high stability.
3	MIXER OUT	The Mixer is double balanced to reduce spurious products. The output impedance is 1.8KΩ to match the input impedance of a 455KHz ceramic filter.
4	SUPPLY VOLTAGE	Must be well decoupled with a 100nF ceramic capacitor.
5	IF LIMITER INPUT	Input pin of the six stages amplifier with about 50μV limiting sensitivity and 1.8KΩ input impedance. The if output is connected to the external quadrature coil (pin 8) via an internal 10pF capacitor.
6-7	DECOUPLING	Good quality 100nF ceramic capacitors and a suitable layout are important.
8	QUADRATURE COIL	A quadrature detector is used to demodulate the 455KHz FM signal. The Q of the quad coil has direct effect on output level and distortion (see fig. 6). For proper operation the voltage should be $100mV_{rms}$.
10	OP AMPLIFIER INPUT	Because of the Low DC bias, the swing on the operational amplifier output is limited to $500mV_{rms}$.
11	OP AMPLIFIER OUTPUT	This can be increased by adding a resistor from the operational amplifier input to ground.
12	SQUELCH INPUT	The squelch trigger circuit with a Low bias on the input (pin 12) will force pin 13 high; and pin 14 Low.
13	SCAN CONTROL	Pulling pin 12 above mute threshold (0.65V) will force pin 13 to an impedance of about 60KΩ to ground and pin 14 will be an open circuit.
14	MUTE	An hysteresis of about 50mV at pin 12 will effectively prevent jitter.
15	GND	Ground connection.
16	10.7MHz MIXER INPUT	Input of the wide-band mixer. Normally used as 10MHz / 455KHz converter, it can be also used with input frequencies up to 60MHz.

ELECTRICAL CHARACTERISTICS ($V_s = 4V$; $f_o = 10.7MHz$; $\Delta f = \pm 3KHz$; $f_m = 1KHz$; $T_{amb} =$ 25°C unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		1.8	4	9	V
I_s	Supply current	Squelch OFF Squelch ON		3.8 4.7		mA
V_i	Input quieting voltage	S/N = 20dB		8		μV
V_i	Input limiting voltage	-3dB limiting		3		μV
V_o	Recovered audio output	V_i = 10mV		150		mV_{rms}
V_9	Detector output voltage			1.5		V_{DC}
R_9	Detector output impedance			400		Ω
	Detector center frequency slope			150		mV/KHz
G_v	Operational amplifier gain	f = 10KHz $G_v = V_{11} / V_{10}$	40	55		dB
V_{11}	Operational amplifier output voltage			1.5		V_{DC}
I_B	Operational amplifier input bias current	Pin 10		20		nA
V_T	Trigger hysteresis			50		mV
R_m	Mute switching impedance	LOW		50		Ω
		HIGH		10		MΩ
V_{13}	Scan voltage	Pin 12 HIGH (2V) Pin 12 LOW (0V)	 3.0	0 3.4	0.5	V_{DC}
G_c	Mixer converter gain			30		dB
R_i	Input resistance			3.3		KΩ
C_i	Input capacitance			2.2		pF

Fig. 2 - Test circuit

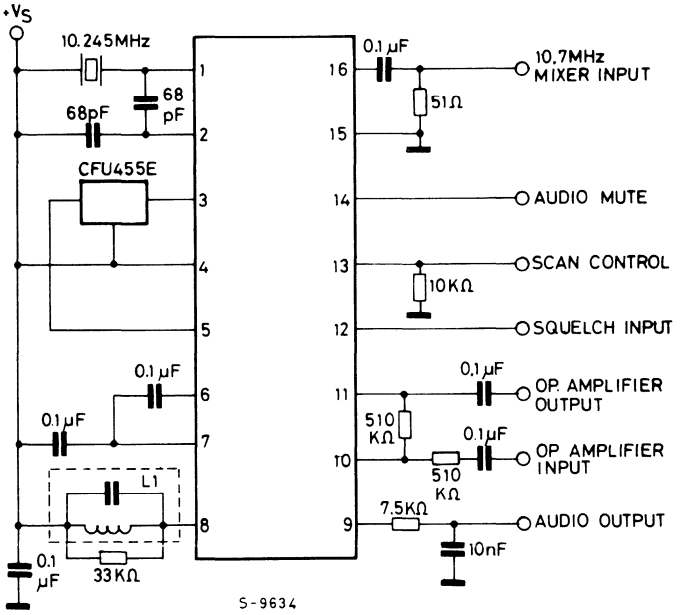


Fig. 3 - Supply current vs. supply voltage

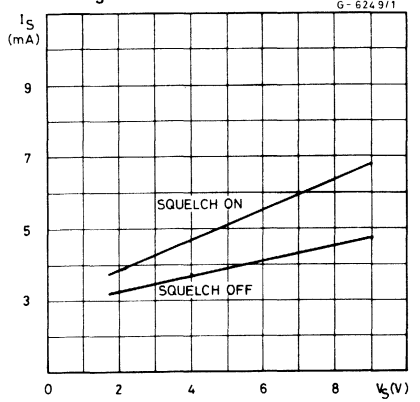


Fig. 4 - FM IF characteristics

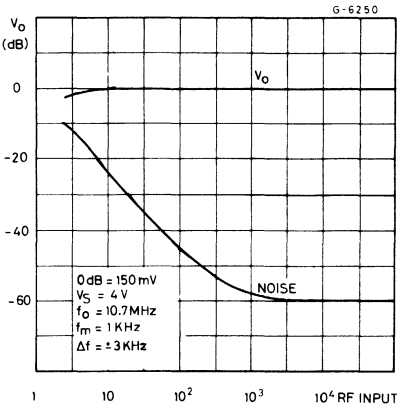


Fig. 5 - Colpitts XTAL oscillator

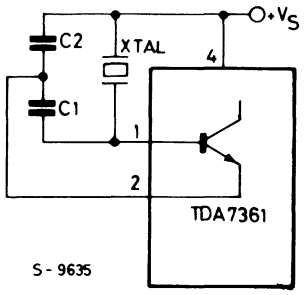


Fig. 6 - Effect of quadrature coil "Q" on audio level and distortion

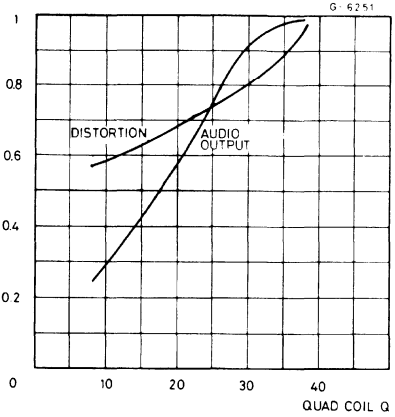
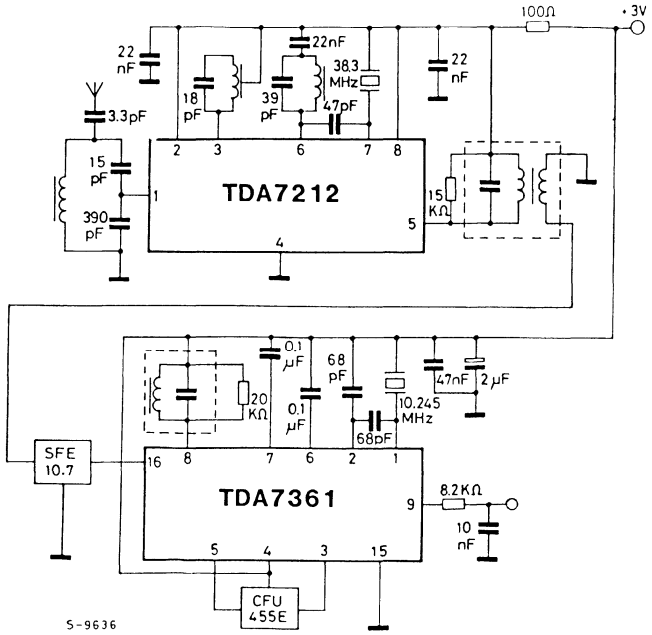


Fig. 7 - Application information (49MHz cordless receiver)



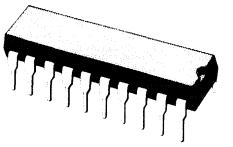
TDA8114

ADVANCE DATA

VCR PROCESSOR INTERFACE CIRCUIT

- CAPSTAN TACHO AMPLIFIER WITH OC OUTPUT
- CTL-PLAYBACK AMPLIFIER WITH OC OUTPUT
- CTL-RECORD AMPLIFIER WITH OC INPUT
- REEL TACHO AMPLIFIER WITH OC OUTPUT
- DRUM POSITION DETECTOR WITH OC OUTPUT + INTERNAL PULL UP RESISTOR
- RESET GENERATOR

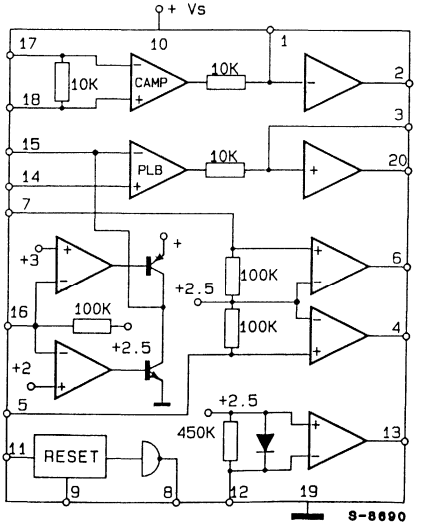
The TDA 8114 is a monolithic integrated circuit for VCR-applications. It is intended to convert signals from optical and magnetical sensors to μP TTL-level. A special circuit includes a supply voltage supervisor and generates a reset signal for μ-Processor.



DIP-20 Plastic (0.4)

ORDERING NUMBER: TDA 8114

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	DC supply voltage	10	V
V_i	DC input voltage	7	V
V_O	Open collector output voltage (all outputs high)	15	V
T_{op}	Operating junction temperature	0 to 85	°C
T_{stg}	Storage temperature	-55 to 125	°C

PIN FUNCTIONS

No.	Name
1	Capstan tacho amplifier output and low pass filter
2	Capstan tacho amplifier OC output
3	CTL amplifier output and low pass filter
4	Reel tacho OC output
5	Teel tacho sensor input
6	Reel tacho OC output
7	Reel tacho sensor input
8	Reset open collector output with internal pull up
9	Reset delay time capacitor
10	Supply voltage
11	Reset supply voltage store
12	Drum position sensor input
13	Drum position open collector output with internal pull-up resistor
14	CTL tacho reference voltage
15	CTL tacho amplifier input
16	CTL Record amplifier TTL input
17	Capstan tacho amplifier input
18	Capstan tacho reference voltage
19	Ground
20	CTL Playback amplifier OC output

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified V_S = 5V)

Parameter		Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage operation range	10		4.5		6	V
I_S	Supply current	10					mA
CAPSTAN TACHO AMPLIFIER							
R_I	Input resistance	17			10		KΩ
V_R	Capstan reference voltage	18			2.5		V
V_I	AC-tacho input voltage	17	f input 50 to 2500Hz	150			μV_{rms}
R_F	Filter output impedance	1			10		KΩ
V_{sat}	Output saturation voltage	2	Low state I_T = 1.8mA			0.4	V
V_O	Output voltage	2	High state I_T = 0mA			15	V
	Negative slope of output signal Pin T yields to zero crossing of input signal Input to output phase relation is non invert.						
CTL-PLAYBACK AMPLIFIER							
R_I	Input resistance	15		100			KΩ
V_R	CTL-Reference voltage	14			2.5		V
V_I	Synchronous peak input voltage	15	Pos. plus detected	200			μV
R_F	Filter output impedance	3			10		KΩ
V_{sat}	Output saturation voltage	20	Low state I_R = 1.8mA			0.4	V
V_O	Output voltage	20	High state I_R = 0			15	V
	Input to output phase relations is invert						
CTL-RECORD AMPLIFIER							
R_I	Input resistance	16	V_I between V_S and GND		100		KΩ
V_R	Input reference voltage	16	Pin open		2.5		V
V_i	Input threshold for output high state	16			3		V
V_{IL}	Input threshold for output low state	16			2		V
$V_{sat\,L}$	Output saturation voltage low state	15	V_Q = L (I_{sink} 5mA)			0.4	V
$V_{sat\,H}$	Output saturation voltage	15	V_Q = H (I_{source} 5mA)			3.5	V
	Input to output phase relation is non invert						

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Pin	Test Conditions	Min.	Typ.	Max.	Unit
REEL-TACHO AMPLIFIER							
R_I	Input resistance	5/14		100			KΩ
V_R	Inpur reference voltage	5/14			2.5		V
V_I	AC-tacho input voltage	5/14	f = 1Hz to 5KHz	1			V_{pp}
V_{sat}	Output saturation voltage	4/6	Low state $I_{O/P}$ = 1.8mA			0.4	V
V_O	Output voltage	4/6	High state $I_{O/P}$ = 0			15	V
	Input to output phase relation is non invert						
DRUM TACHO AMPLIFIER							
R_i	Input resistance	12	V_{IN} between 1 and 7V		450		KΩ
V_R	Input reference voltage	12			2.5		V
V_{ic}	Input clamping voltage	12	Sink current 100μA		V_R-0.6		V
V_{IP}	Input peak voltage	12				8	V
V_{sat}	Output saturation voltage	13	Low state I_N = 1.8mA			0.4	V
V_O	Output voltage	13	High state I_N = 0			15	V
V_i	AC-tacho input voltage	12		1			V_{pp}
	Input to output phase relation is non invert						
RESET GENERATION							
V_S	Reset supply voltage	11			V_S-0.6		V
V_{SR}	Reset supply voltage operation range	11		3		V_S	V
I_R	Reset supply current	11			2		mA
I_C	Charging current	9			25		μA
I_{DC}	Discharging current	9	U_K = 2V Discharging current is present for $V_S < V_{sens}$		2.5		mA
V_{sen}	Reset sense voltage	10		4.5	4.6	4.7	V
V_{CH}	Comparator high threshold	9	Output low to high		2		V
V_{CL}	Comparator low threshold output open collector with intervall pull up resistor	9	Output high to low		3		V
V_{sat}	Output saturation voltage	8	Low state I_M = 1.8mA			0.4	V
OPTIONAL OUTPUT (push-pull)							
V_{sat}	Output saturation voltage	8	Low state I_M = 1.8mA			0.4	V
V_{sat}	Output saturation voltage	8	High state I_M = 1.8mA	3.5			V

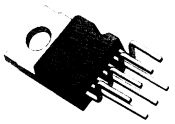
TDA8115

ADVANCE DATA

DUAL MOTOR DRIVER

- HIGH OUTPUT CURRENT, EACH CHANNEL UP TO 1A
- WIDE SUPPLY VOLTAGE RANGE, 4V UP TO 28V
- SHORT CIRCUIT PROTECTION
- SAFE OPERATING AREA CURRENT LIMITING
- TEMPERATURE SHUT DOWN WITH HYSTERESIS
- HIGH INPUT IMPEDANCE
- GROUND COMPATIBLE INPUT

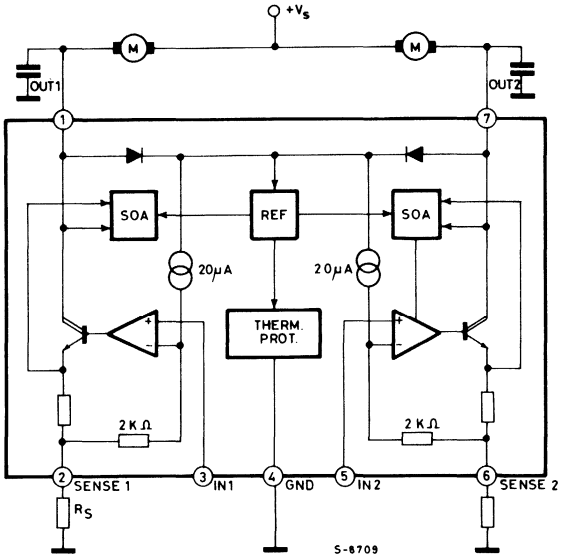
The TDA8115 is a monolithic integrated circuit which realizes two independent programmable current sources. The device is well suited for motor driving applications such as reel motors in video recorders. A wide supply voltage range permits battery operation.



Heptawatt

ORDERING NUMBER: TDA8115

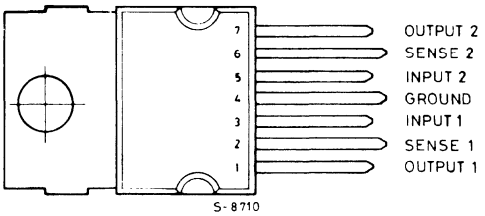
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	28	V
I_o	Output current (each channel)	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{op}	Operation junction temperature	-40 to + 150	°C
T_{stg}	Storage temperature	-40 to + 150	°C

CONNECTION DIAGRAM
(Top view)



Pin 4 connected to the TAB

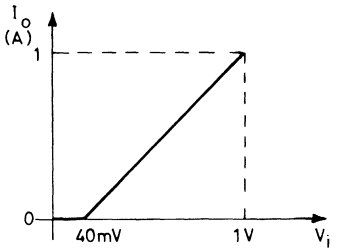
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage		4		23	V
I_Q	Quiescent current			2	5	mA
I_O	Output current range				1	A
V_{IR}	Input voltage range		0		V_S -3	V
V_{OS}	Positive input offset for current starting point		50	60	80	mV
	Thermal shut down			150		°C
	Hysteresis			20		°C
I_L	Output current limit V_S = 10V V_S = 20V			 1.4 0.4		 A A
I_b	Input bias current				1	μA
V_{sat}	Saturation voltage	I_{OUT} = 0.9A		1.4	2	V
R_B	Bond resistance			60		mΩ

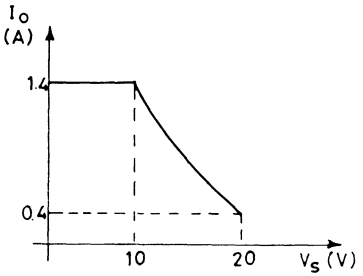
Fig. 1 - Transconductance characteristic



S-8711

with $I_O = \frac{V_{IN} - 40mV}{(R_S + 60m\Omega)}$

Fig. 2 - Max output current vs. supply voltage (SOA)



S-8712

TDA8116

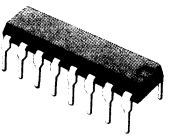
ADVANCE DATA

BRUSHLESS SERVO CONTROLLER

- WIDE OPERATING VOLTAGE RANGE 6V TO 14V
- HIGH CURRENT CAPABILITY UP TO 1A
- OUTPUT DC CURRENTS UP TO 0.4A
- TWO LOGICAL INPUTS FOR THE CODED COMUNICATION SIGNAL
- LIMITED SLEW RATE OF THE OUTPUT VOLTAGE
- ANALOG INPUT WITH FIXED VOLTAGE GAIN
- INTEGRATED FLYBACK DIODES AT EACH OUTPUT
- THERMAL PROTECTION

The TDA 8116 is a monolithic integrated circuit in bipolar technology.

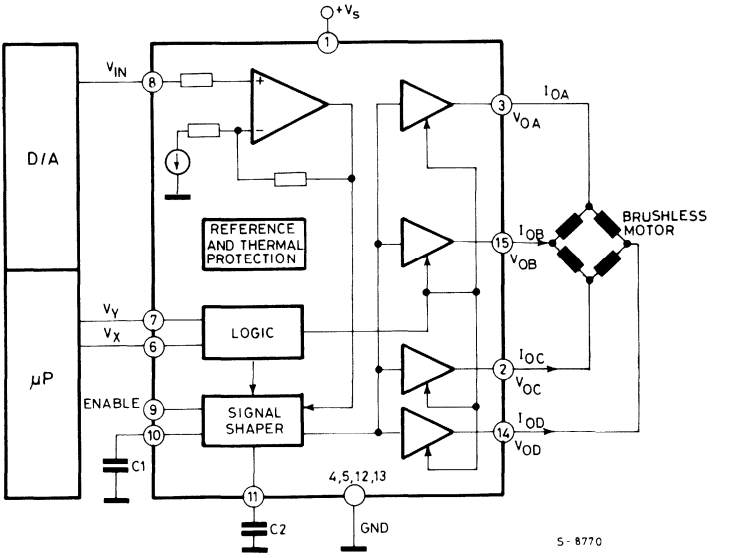
It is intended for driving a four phase brushless motor in microcomputer controlled servo systems.



Powerdip (12 + 2 + 2)

ORDERING NUMBER: TDA 8116

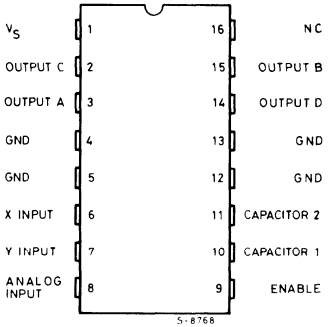
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	-0.3 to 18	V
I_O	Output current DC	± 0.4	A
	Pulse output current (during start)	± 1	A
T_{JOP}	Operating junction temperature	0 to 150	°C
T_{stg}	Storage junction temperature	-40 to 150	°C
$V_{EN, IN, X, Y}$	Input voltage	-0.3 to 7	V
P_{tot}	Power dissipation at $T_{case} = 80°C$	5	W

CONNECTION DIAGRAM
(Top view)



PIN FUNCTION

N°	NAME	FUNCTION
1	V_S	Supply voltage connection.
2	OUTC	Push-Pull type output for the C phase.
3	OUTA	Push-Pull type output for the A phase
4, 5, 12, 13	GND	Ground connection.
6	X INPUT	Commutation signal X input.
7	Y INPUT	Commutation signal Y input.
8	INPUT	Analog control signal input.
9	ENABLE	Enable input, with low level (< 1,5V) at this pin the device outputs are set into TRISTATE.
10, 11	CAPACITOR 1, 2	The shaping capacitors at these pins define the output signal shape of the A, C and B, D outputs respectively.
14	OUTD	Push-Pull type output for the D phase.
15	OUTB	Push-Pull type output for the B phase.
16	N.C.	No connection at this pin.

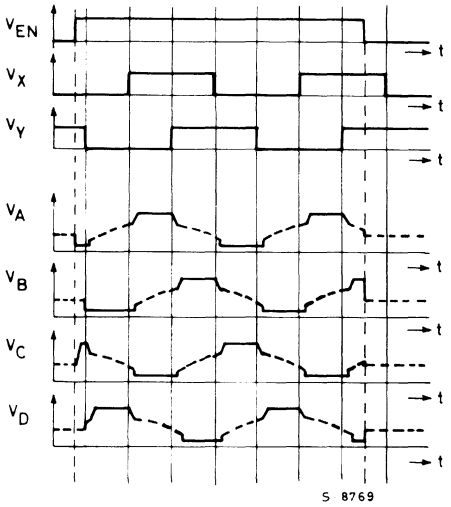
THERMAL DATA

Parameter		Min.	Typ.	Max.	Unit
T_{JSTD}	Thermal shut down threshold		150		°C
T_{JSDH}	Thermal shut down hysteresis		20		°C
$R_{th\ j\text{-}case}$	Thermal resistance junction-ground pins			14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient			80	°C/W

ELECTRICAL CHARACTERISTICS ($6V < V_S < 14V$, $T_j = 25°C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{Sop}	Operating sypply voltage range		6		14	V
V_{SO}	Source stage saturation voltage	$V_{IN} = 5V$ $I_O = 1A$ $I_O = 0.4A$		1.4 1	2 1.4	V V
V_O	Sink stage saturation voltage	$V_{IN} = 5V$ $I_O = 1A$ $I_O = 0.4A$		1.4 1	2 1.4	V V
A_V	Voltage gain	$V_{IN} = 1V$ $R_L = 50\Omega$	2.5	2.75	3.0	V
V_{INth}	Input voltage threshold		0.6	0.7	0.8	V
I_N	Input current	$V_{IN} = 5V$	-5	-1	+5	μA
V_{IN}	Input voltage operating voltage range		0		$V_S - 1$	V
$V_{X,Y\ High}$	Control input HIGH level		1.7	2.4	7	V
$I_{X,\ Y\ High}$	Control input HIGH current	$V_{IN} = 5V$			20	μA
$V_{X,\ Y\ Low}$	Control input LOW level		0.3		0.8	V
$I_{X,\ Y\ Low}$	Control input LOW current	$V_{IN} = 0.4V$	-20		20	μA
$V_{EN\ Low}$	Enable input LOW level		-0.3		1.5	V
$V_{EN\ High}$	Enable input HIGH level		2.4		7	V
$I_{EN\ Low}$	Enable input LOW current	$V_{EN} = 0V$		-20	-40	μA
$I_{EN\ High}$	Enable input HIGH current	$V_{EN} = 5V$		1		μA
$VH_{X,\ Y,\ EN}$	Control and enable inputs hysteresis			150		mV
$\frac{dV_{out}}{dt}$	Output voltage slope	$C_{1,2} = 10nF$		6		V/ms
$\lvert I_{OST} \rvert$	Starting output current	$V_{IN} = 5V$ $V_S = 12V$			1	A
I_S	Quiescent supply current	$V_{IN} = 0$		3	5	mA
I_S	Supply current	$V_{IN} = 5V$		8	15	mA

TYPICAL WAVEFORMS



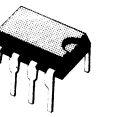
TDA8160

ADVANCE DATA

INFRARED REMOTE CONTROL RECEIVER

- LOW SUPPLY VOLTAGE (V_S = 5V)
- LOW CURRENT CONSUMPTION (I_S = 6mA)
- INTERNAL 5.5V SHUNT REGULATOR
- PHOTODIODE DIRECTLY COUPLED WITH THE I.C.
- INPUT STAGE WITH GOOD REJECTION AT LOW FREQUENCY
- LARGE INPUT DYNAMIC RANGE
- FEW EXTERNAL COMPONENTS

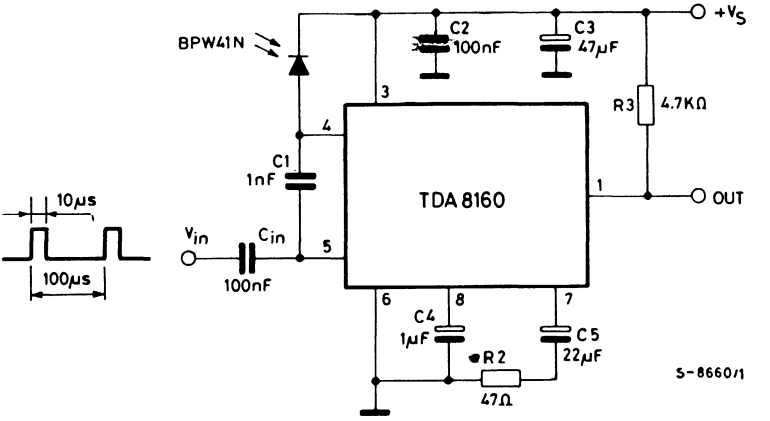
The TDA 8160 is a monolithic integrated circuit in -lead minidip plastic package specially designed to amplify the infrared signals in remote controlled TV, Radio or VCR sets. It can be used in flash transmission mode in conjunction with dedicated remote control circuits (for example: M491-494).



Minidip Plastic

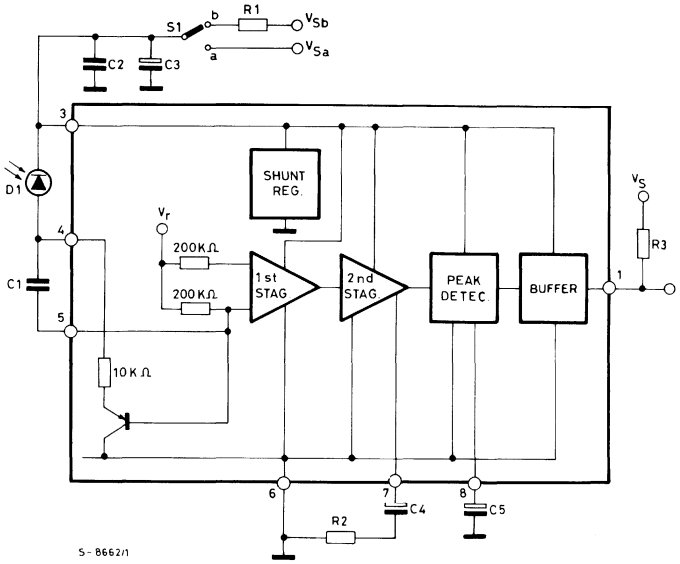
ORDERING NUMBER: TDA8160

TEST CIRCUIT



TDA8160

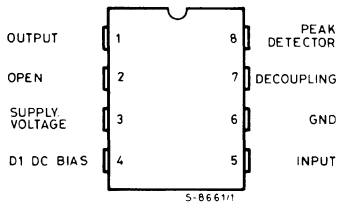
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	16	V
T_{stg-j}	Storage and junction temperature	-40 to 150	°C
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_S = 5V, f_o = 10kHz, T_{amb} = 25°C, unless otherwise specified)

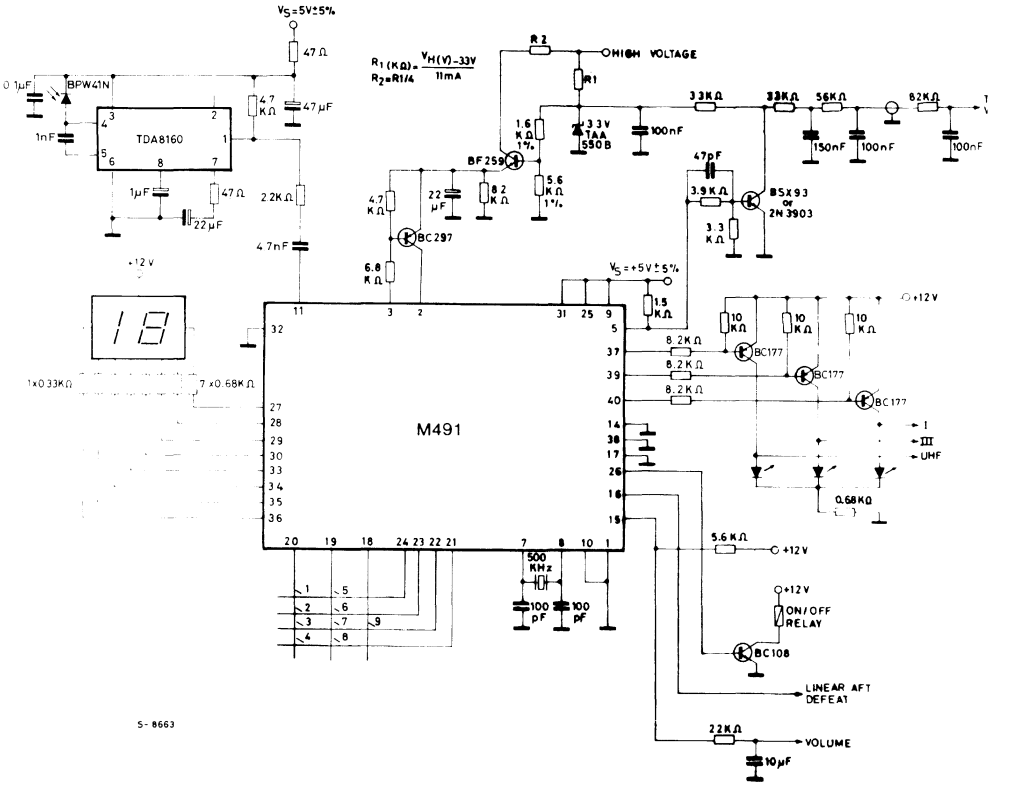
	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage	Applied between pin 3 and 6	4	5	5.25	V
I_S	Supply current (pin 3)			6		mA
V_3	Stabilized voltage at pin 3	I_3 = 8mA		5.5		V
G_V 1st	Voltage gain (1st stage)			28		dB
g_m 2nd	Transconductance (2nd stage)			15		mA/V
V_{in}	Input voltage sensitivity (pin 5)	For full swing at the output pin 1 R_{gen} = 600Ω		2		mV_p
I_{in}	Input current sensitivity (pin 5)	For full swing at the output pin 1		10		nA_p
R_{in}	Input impedance			200		KΩ
L_f R	Low frequency rejection at the input stage	C1 = 100pF f = 100Hz		30		dB
N	Noise signal at pin 7	C4 missing		200		mV_{pp}

CIRCUIT DESCRIPTION (See the block diagram)

The infrared light received from D1 generates an AC signal that comes in to the device at pin 5. The capacitor C1 and the integrated 10KΩ resistor (pin 4) filter out the low frequency noise.

The first stage shows a voltage gain of about 28dB; the second stage is a voltage to current converter of 50mA/V (R_2 = Zero). A sensitive peak detector detects the amplifier signal; one open collector output (pin 1) gives out the recovered pulses.

Fig. 1 - Recommended application circuit for the drive of the IC M491 by means of a Flash Mode IR Transmitter only, in a TV 16 station memory Remote Control subsystem.
The above shown IR receiver application must be housed inside a metal can shield.

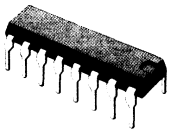


TEA1330

FM STEREO DECODER

- REQUIRES NO INDUCTORS
- LOW EXTERNAL PART COUNT
- ONLY OSCILLATOR FREQUENCY ADJUSTMENT NECESSARY
- INTEGRAL STEREO/MONAURAL SWITCH WITH HIGH LAMP DRIVING CAPABILITY
- WIDE SUPPLY RANGE: 3V TO 14V
- EXCELLENT CHANNEL SEPARATION MAINTAINED OVER ENTIRE AUDIO FREQUENCY RANGE
- LOW DISTORTION: TYPICALLY 0.3% AT 150mV (RMS) COMPOSITE INPUT SIGNAL
- EXCELLENT SCA REJECTION (76dB TYP.)

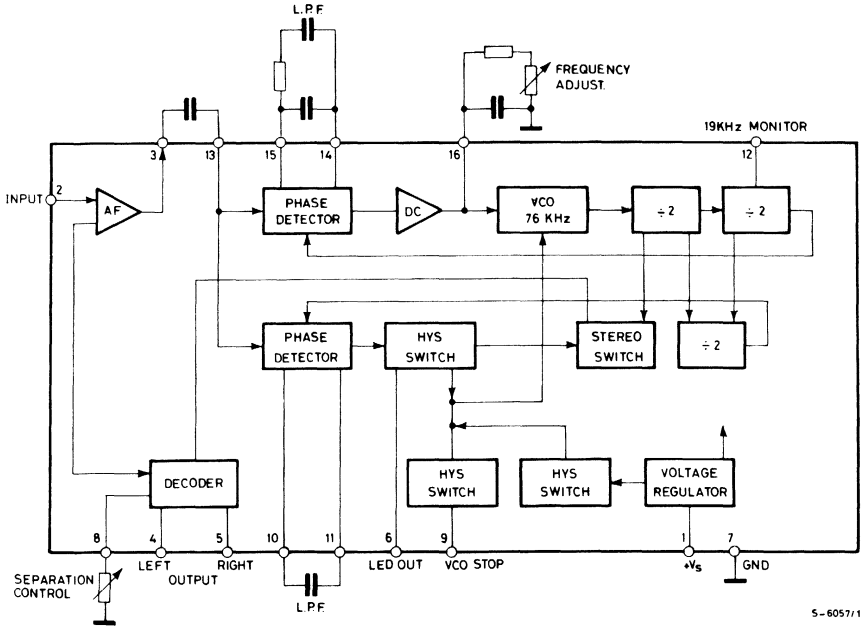
The TEA1330 is a monolithic decoder circuit for FM stereo transmissions. Packaged in a 16-pin DIP, it functions with very few external components and requires no inductors.



DIP-16 Plastic
(0.25)

ORDERING NUMBER: TEA1330

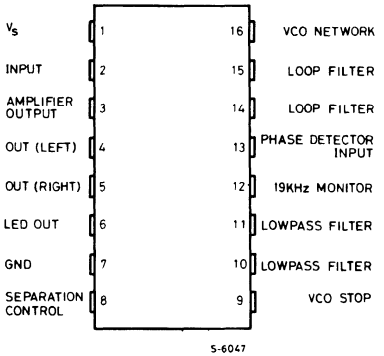
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_L	Lamp current	75	mA
P_{tot}	Power dissipation $T_{amb} = 70°C$	800	mW
T_{op}	Operating temperature	-25 to 75	°C
T_{stg}	Storage temperature	-55 to to 150	°C

CONNECTION DIAGRAM
(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

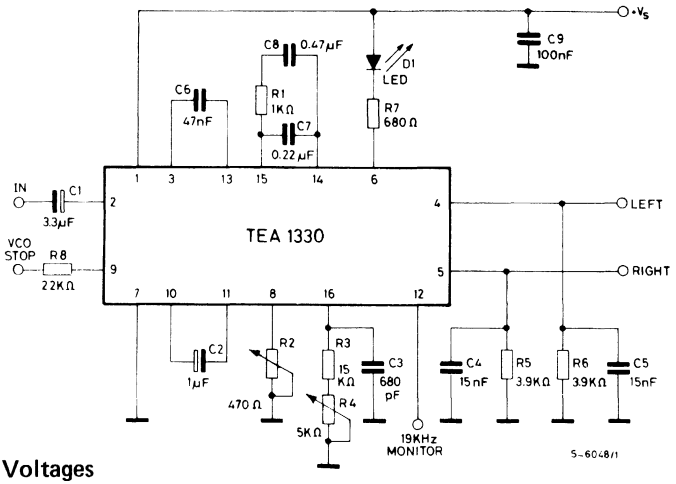
ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, V_s = 6V, V_i = 300 mV-RMS (L + R = 90%, Pilot 10%), f_m= 1 KHz, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		3		14	V
I_d	Current drain	Lamp "OFF"		18		mA
V_i	Max standard composite input signal	d = 1%	300			mV (RMS)
V_i	Max mono input signal	d = 1%	300			mV (RMS)
R_i	Input resistance			40		KΩ
Sep	Stereo channel separation	R2 = variable (*)	35	50		dB
		R2 = 270 Ω	25	40		dB
V_o	Audio output voltage			265		mV
CB	Mono channel balance	Pilot tone "OFF"	-2	0	+2	dB
d	Total harmonic distortion	V_{in}= 150 mV (RMS)		0.3		%
UR	Ultrasonic frequency rejection	f = 19 KHz		32		dB
		f = 38 KHz		48		dB
SCA-R	SCA rejection (**)	f = 67 KHz		76		dB
S/N	Signal to noise ratio			80		dB
V_{th}	Muting threshold voltage (pin 9)	ON (VCO stop)		1		V
		OFF		0.8		V
L_{on}	Pilot input level for lamp ON	f = 19 KHz	4	6	9	mV
Hys	Pilot input level hysteresis for lamp turn ON-OFF	f = 19 KHz		3		dB
CR	Capture range			± 7		%

(*) R2 has to be adjusted for best figure of channel separation.

(**) SCA = AUX. SUB. CARRIER.

Fig. 1 - Test circuit



Typical DC Voltages

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(V)	6	1.9	1.3	3	3		0	0.18		1.4	1.4	1.2	1.4	1.4	1.4	2.2

Fig. 2 - P.C. board and components layout of the test circuit of fig. 1 (1:1 scale)

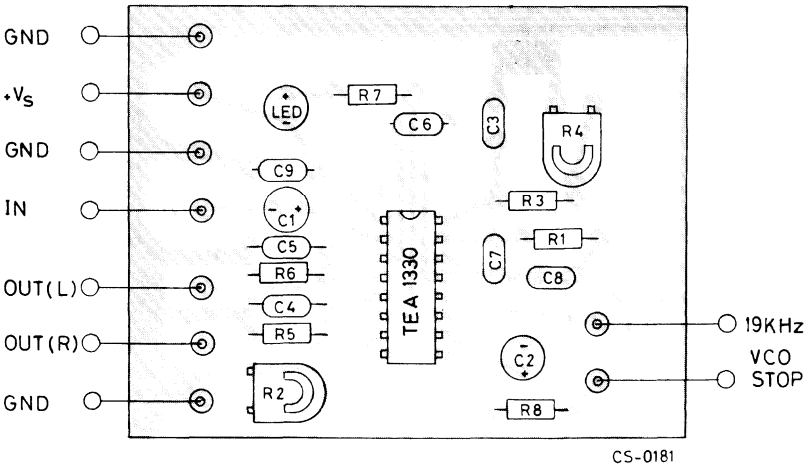


Fig. 3 - Channel separation vs. modulation frequency

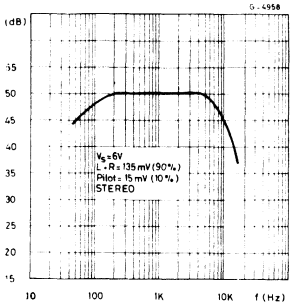


Fig. 4 - Distortion vs. modulation frequency

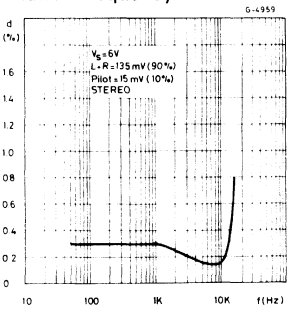


Fig. 5 - Channel separation vs. input level

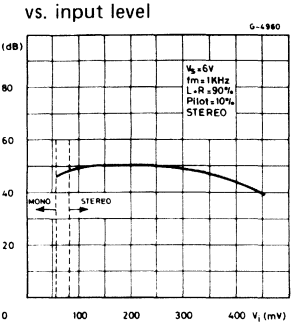


Fig. 6 - Distortion vs. input level

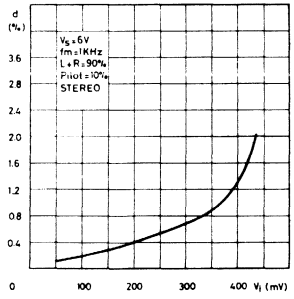


Fig. 7 - Channel separation vs. supply voltage

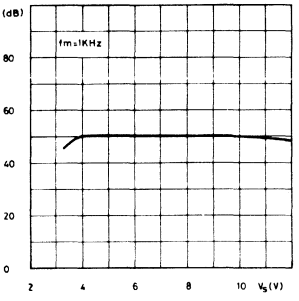
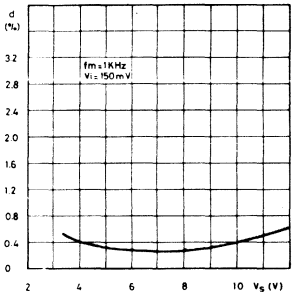


Fig. 8 - Distortion vs. supply voltage



APPLICATION SUGGESTION (see test circuit of fig. 1)

Component	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C1	3.3 μF	Input coupling	Poor low frequency response and separation	
C2	1 μF	LPF for stereo switch level detector	Shorter time to switch mono to stereo	Longer time to switch mono to stereo
C3 (*) R3 R4	680 pF 15 KΩ 5 KΩ	Set VCO free running frequency	– High VCO jitter – Wide capture range	Narrower capture range

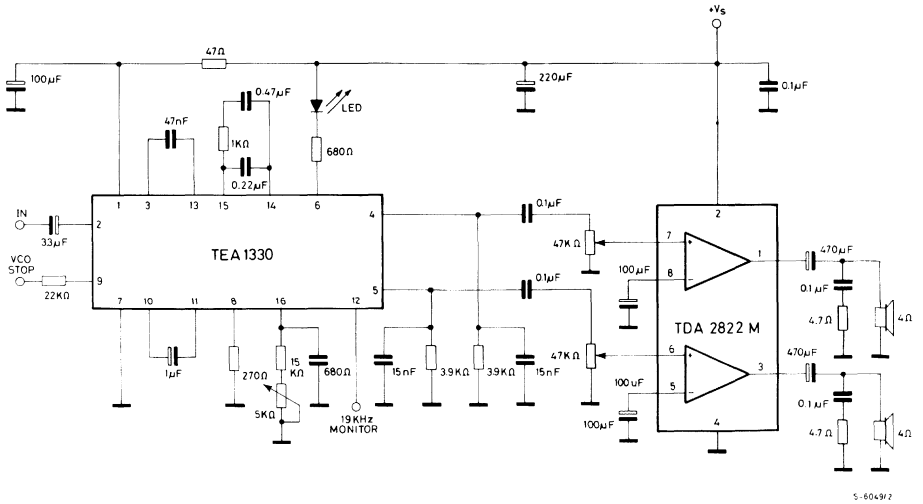
(*) Polyester ± 5%.

APPLICATION SUGGESTION (continued)

Component	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C4 R5 (**)	15 nF 3.9 KΩ	Load and deemphasis right channel	Low output voltage	Higher distortion for low V_S
C5 R6 (**)	15 nF 3.9 KΩ	Load and deemphasis left channel	Low output voltage	Higher distortion for low V_S
C6	47 nF	Input PLL coupling	Poor low frequency response and separation	
C7 C8 R1	220 nF 470 nF 1 KΩ	Loop filter	High stereo distortion	Narrower capture range
D1		Stereo indicator		
R7		Sets lamp current	Excess IC dissipation	Dim lamp
R2 (***)	270 Ω	Channel separation		

(**) Deemphasis = 50 μs.
(***) Separation can be improved by trimmer adjustement (470 Ω).

Fig. 9 - Application circuit for portable stereo radio receivers



TL072

LOW NOISE JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

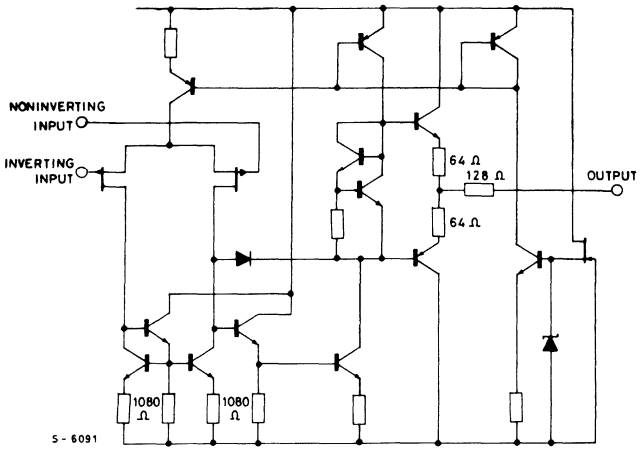
- HIGH SLEW-RATE . . . 13V/μs TYP.
- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The TL072 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset voltage temperture coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

Minidip (Plastic and Ceramic) **SO-8**

SCHEMATIC DIAGRAM
(one section)



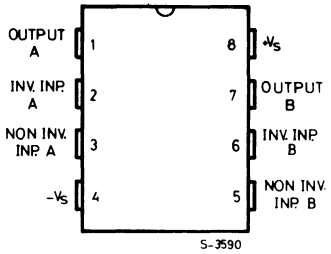
TL072

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 15	V
T_{op}	Operating temperature (TL072I)	-25 to 85	°C
	(TL072C)	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

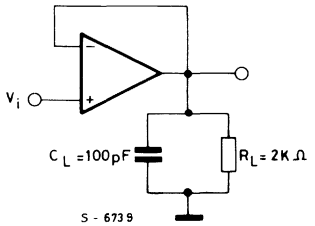
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

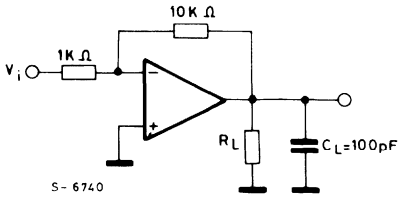


0 to 70°C	-25 + 85°C	Package
TL072CJG TL072ACJG TL072BCJG	TL072IJG — —	Ceramic Minidip
TL072CP TL072ACP TL0BCP	TL072IP — —	Plastic Minidip
TL072CD	TL072ID	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 15V, T_{amb} = 25°C, otherwise specified)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	R_s = 50Ω	TL072		3	6		3	10	mV
			TL072A					3	6	
			TL072B					2	3	
		R_s = 50Ω, T_{amb} = full range	TL072			9			13	
			TL072A						7.5	
			TL072B						5	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	R_s = 500Ω, T_{amb} = full range			10			10		µV/°C
I_{OS}	Input offset current		TL072		5	50		5	50	pA
			TL072A					5	50	
			TL072B					5	50	
		T_{amb} = full range	TL072			10			2	nA
			TL072A						2	
			TL072B						2	
I_b	Input bias current		TL072		30	200		30	200	pA
			TL072A					30	200	
			TL072B					30	200	
		T_{amb} = full range	TL072			20			7	nA
			TL072A						7	
			TL072B						7	
V_{CM}	Common mode input voltage range		TL072	± 11	± 12		± 10	± 11		V
			TL072A				± 11	± 12		
			TL072B				± 11	± 12		
V_{OPP}	Large signal voltage swing		R_L = 10KΩ	24	27		24	27		V
		T_{amb} = full range	$R_L \geq$ 10KΩ	24			24			
			$R_L \geq$ 2KΩ	20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq$ 2KΩ, V_o = ± 10V	TL072	50	200		25	200		V/mV
			TL072A				50	200		
			TL072B				50	200		
		$R_L \geq$ 2KΩ, V_o = ± 10V, T_{amb} = full range	TL072	25			15			
			TL072A				25			
			TL072B				25			
B	Unity gain bandwidth				3			3		MHz
R_I	Input resistance				10^{12}			10^{12}		Ω
CMR	Common mode rejection	$R_s \geq$ 10KΩ	TL072	80	86		70	76		dB
			TL072A				80	86		
			TL072B							
SVR	Supply voltage rejection	$R_s \geq$ 10KΩ	TL072	80	86		70	76		dB
			TL072A				80	86		
			TL072B				80	86		
I_S	Supply current	R_L = ∞			2.8	5		2.8	5	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Cs	Channel separation	G_V = 100			120			120		dB
SR	Slew-rate at	V_i = 10V C_L = 100pF	R_L = 2KΩ		13			13		V/μs
t_r	Rise time	V_i = 20mV	R_L = 2KΩ		0.1			0.1		μs
	Overshot factor	C_L = 100pF			10			10		%
e_N	Total input noise voltage	R_S = 100Ω	F = 1KHz		18			18		$\frac{nV}{\sqrt{Hz}}$
			f = 10Hz to 10KHz		4			4		μV
I_N	Input noise current	f = 1KHz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	V_O = 10V_{rms} R_S < 1KΩ R_L > 2KΩ	f = 1KHz		0.01			0.01		%

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

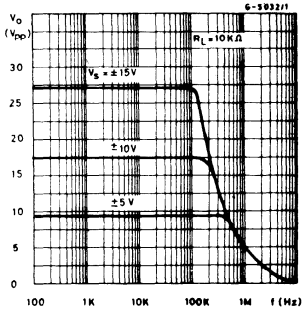


Fig. 2 – Maximum peak to peak output voltage vs. frequency

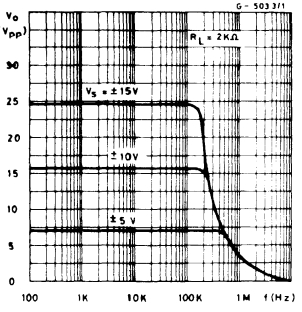


Fig. 3 – Maximum peak to peak output voltage vs. load resistance

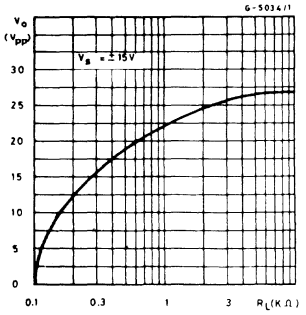


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

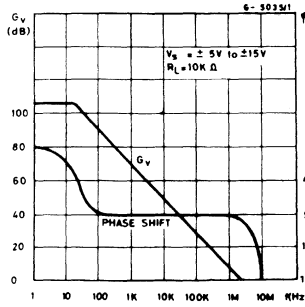


Fig. 5 Supply current vs. supply voltage

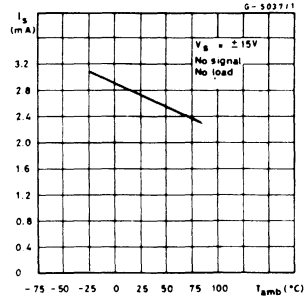


Fig. 6 – Supply current vs. supply voltage

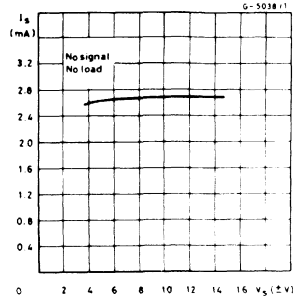


Fig. 7 – Input bias current vs. temperature

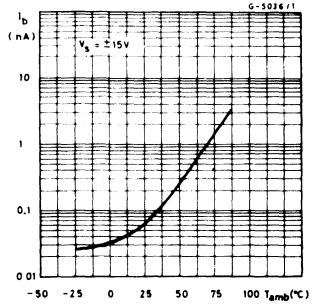


Fig. 8 – Voltage follower large signal pulse response

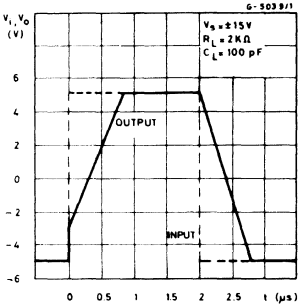


Fig. 9 – Output voltage vs. elapsed time

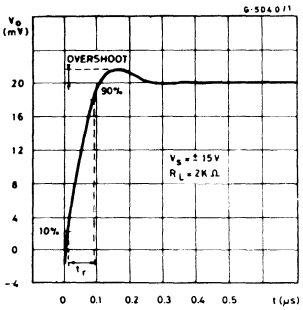


Fig. 10 – Equivalent input noise voltage vs. frequency

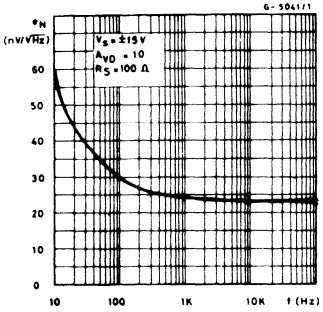


Fig. 11 – Total harmonic distortion vs. frequency

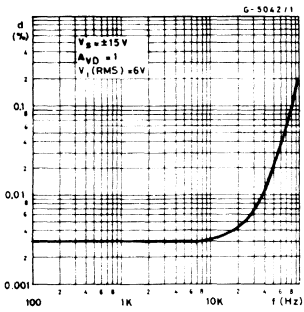
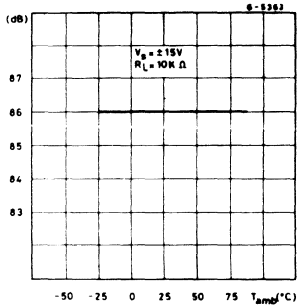
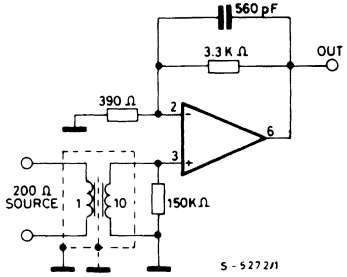


Fig. 12 Common mode rejection vs. temperature



APPLICATION INFORMATION

Fig. 13 – Low-Noise High Slew-Rate mike preamplifier (G_v = 40 dB)



APPLICATION INFORMATION (continued)

Fig. 14 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)

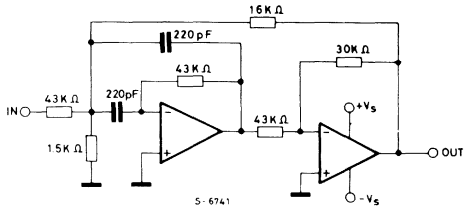


Fig. 15 - Further-order subtractive Linkwitz-Riley crossover filter (f = 200Hz)

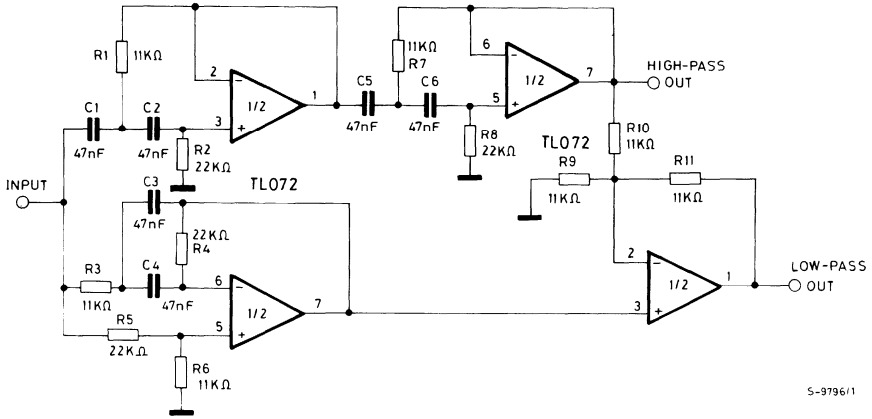
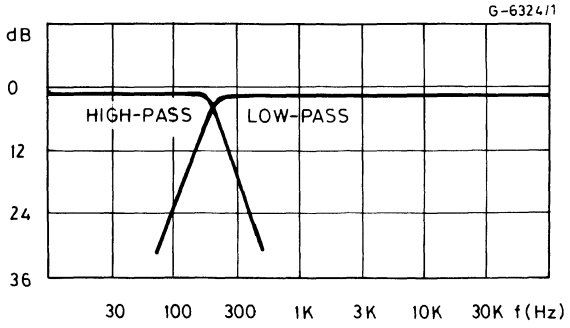


Fig. 16 - Frequency response of the 24dB/octave crossover filter of fig. 15



APPLICATION INFORMATION (continued)

Fig. 17– 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

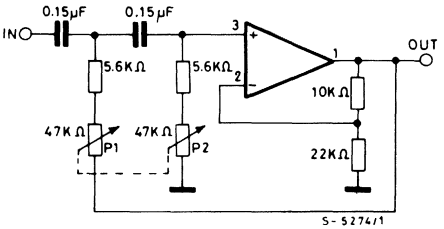


Fig. 18 - Frequency response of the high-pass filter of fig. 17

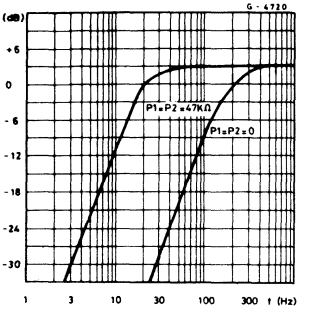


Fig. 19 - Unity-gain absolute-value circuit

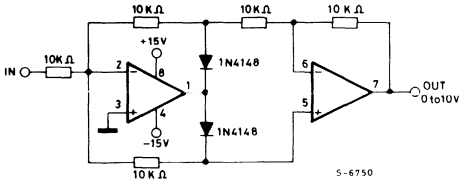


Fig. 20 - Single supply sample and hold

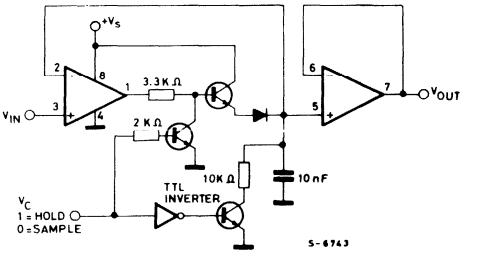
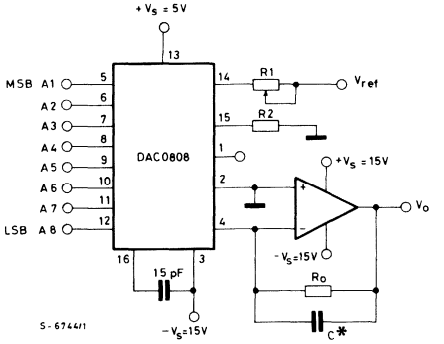


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 µs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 V_{dc}
R1 = R2 ≈ 1.0 kΩ
R_o = 5.0 kΩ

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

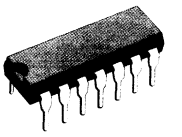
TL074

LOW NOISE JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

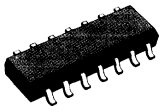
- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION
- HIGH SLEW-RATE . . . 13V/μs TYP.

The TL074 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

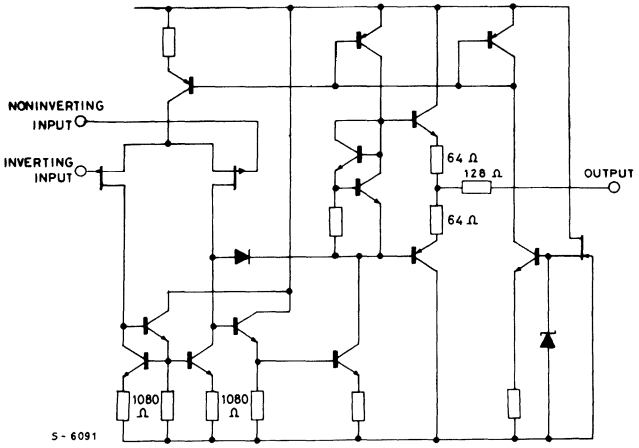


DIP-14
(Plastic and Ceramic)



SO-14J

SCHEMATIC DIAGRAM
(one section)

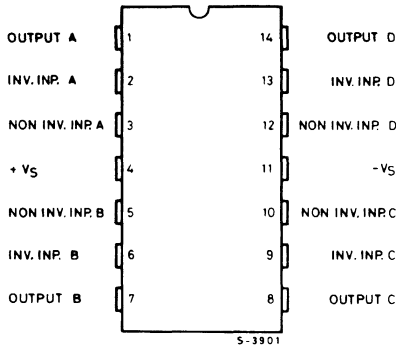


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 15	V
T_{op}	Operating temperature (TL074I)	-25 to 85	°C
	(TL074C)	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

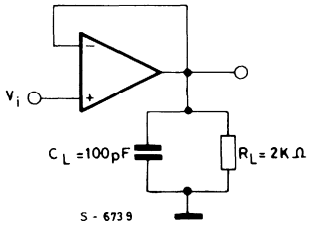
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

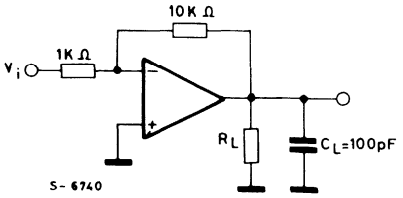


0 to 70°C	-25 + 85°C	Package
TL074CJ TL074ACJ TL074BCJ	TL074IJ – –	Ceramic DIP-14
TL074CN TL074ACN TL074BCN	TL074IN – –	Plastic DIP-14
TL074CD	TL074ID	SO-14

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 15V, T_{amb} = 25°C, otherwise specified)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	R_s = 50Ω	TL074		3	6		3	10	mV
			TL074A					3	6	
			TL074B					2	3	
		R_s = 50Ω T_{amb} = full range	TL074			9			13	
			TL074A						7.5	
			TL074B						5	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	R_s = 50Ω T_{amb} = full range			10			10		μV/°C
I_{OS}	Input offset current		TL074		5	50		5	50	pA
			TL074A					5	50	
			TL074B					5	50	
		T_{amb} = full range	TL074			10			2	nA
			TL074A						2	
			TL074B						2	
I_b	Input bias current		TL074		30	200		30	200	pA
			TL074A					30	200	
			TL074B					30	200	
		T_{amb} = full range	TL074			20			7	nA
			TL074A						7	
			TL074B						7	
V_{CM}	Common mode input voltage range		TL074	± 11	± 12		± 10	± 11		V
			TL074A				± 11	± 12		
			TL074B				± 11	± 12		
V_{OPP}	Large signal voltage swing	T_{amb} = full range	R_L = 10KΩ	24	27		24	27		V
			$R_L \geq$ 10KΩ	24			24			
			$R_L \geq$ 2KΩ	20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq$ 2KΩ V_o = ± 10V	TL074	50	200		25	200		V/mV
			TL074A				50	200		
			TL074B				50	200		
		$R_L \geq$ 2KΩ V_o = ± 10V T_{amb} = full range	TL074	25			15			V/mV
			TL074A				25			
			TL074B				25			
B	Unity gain bandwidth				3			3		MHz
R_I	Input resistance				10^{12}			10^{12}		Ω
CMR	Common mode rejection	$R_s \geq$ 10KΩ	TL074	80	86		70	76		dB
			TL074A				80	86		
			TL074B				80	86		
SVR	Supply voltage rejection	$R_s \geq$ 10KΩ	TL074	80	86		70	76		dB
			TL074A				80	86		
			TL074B				80	86		
I_S	Supply current	R_L = ∞			5.6	10		5.6	10	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Cs	Channel separation	G_V = 100			120			120		dB
SR	Slew-rate at unity gain	V_i = 10V, C_L = 100pF	R_L = 2KΩ		13			13		V/μs
t_r	Rise time	V_i = 20mV, C_L = 100pF	R_L = 2KΩ		0.1			0.1		μs
	Overshot factor				10			10		%
e_N	Total input noise voltage	R_S = 100Ω	f = 1KHz		18			18		$\frac{nV}{\sqrt{Hz}}$
			f = 10Hz to 10KHz		4			4		μV
I_N	Input noise current	f = 1KHz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	V_O = 10Vrms, R_S < 1KΩ, R_L > 2KΩ	f = 1KHz		0.01			0.01		%

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

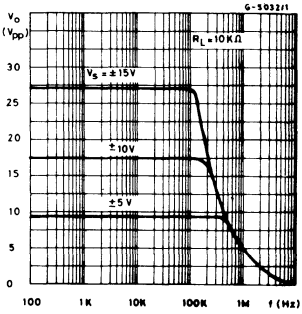


Fig. 2 – Maximum peak to peak output voltage vs. frequency

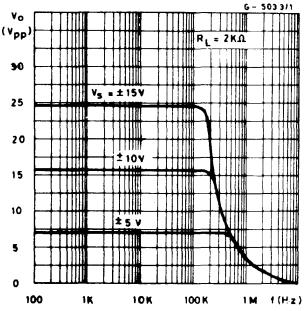


Fig. 3 – Maximum peak to peak output voltage vs. load resistance

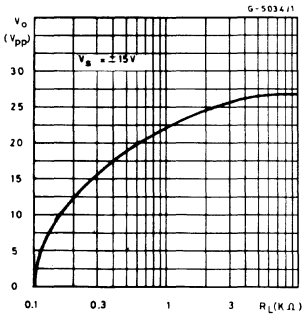


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

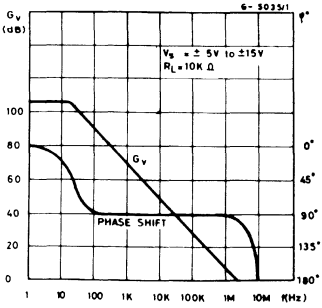


Fig. 5 Supply current vs. temperature

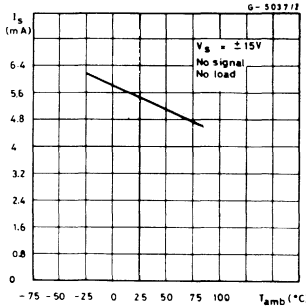


Fig. 6 – Supply current vs. supply voltage

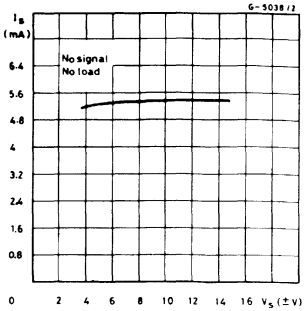


Fig. 7 – Input bias current vs. temperature

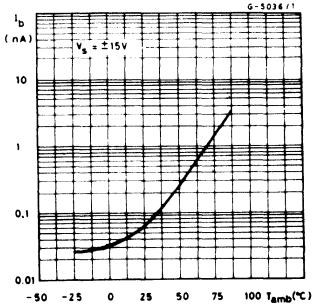


Fig. 8 – Voltage follower large signal pulse response

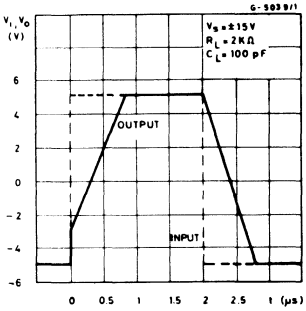


Fig. 9 – Output voltage vs. elapsed time

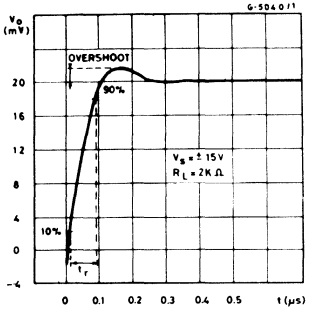


Fig. 10 – Equivalent input noise voltage vs. frequency

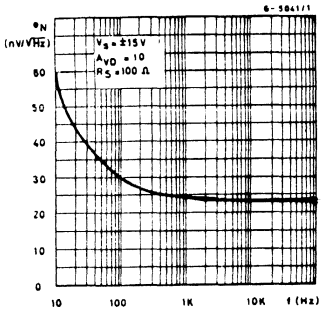


Fig. 11 – Total harmonic distortion vs. frequency

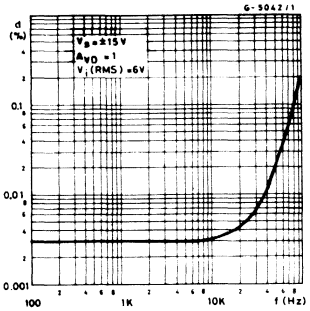
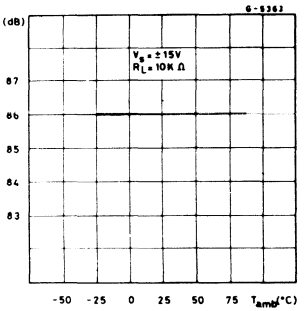
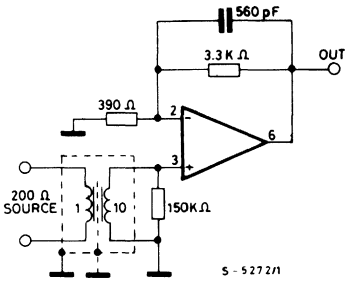


Fig. 12 Common mode rejection vs. temperature



APPLICATION INFORMATION

Fig. 13 - Low-Noise high Slew-Rate mike preamplifier (G_V = 40dB)



APPLICATION INFORMATION (continued)

Fig. 14 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)

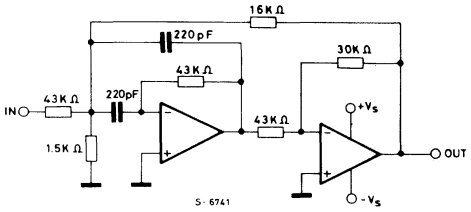
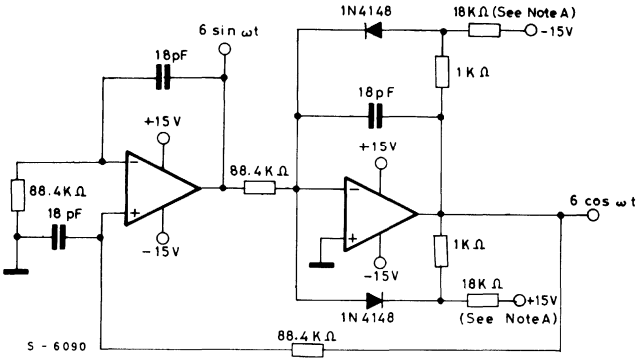


Fig. 15 – 100KHz quadrature oscillator



Note A: these resistor values may be adjusted for a simmetrical output

Fig 16 – 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

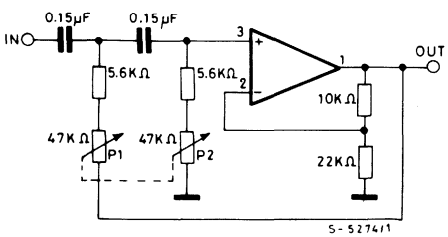
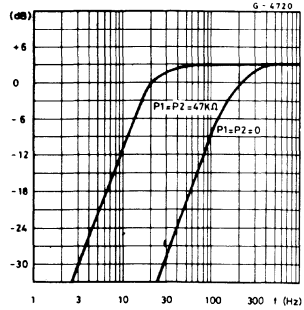


Fig. 17 – Frequency response fo the high-pass filter of fig. 16



APPLICATION INFORMATION (continued)

Fig. 18 – Unity-gain absolute-value circuit

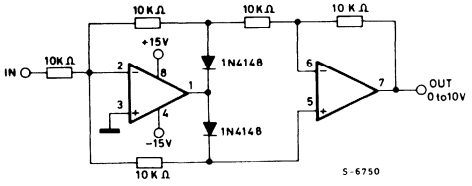


Fig. 19 – Single supply sample and hold

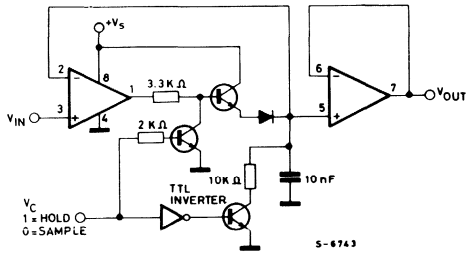
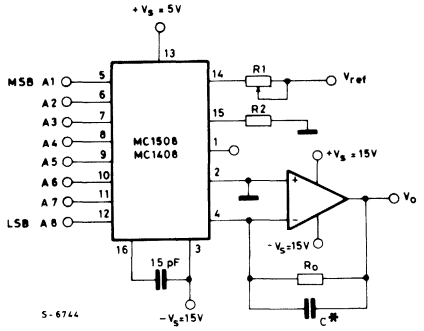


Fig. 20 – Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 V_{dc}
R1 = R2 ≈ 1.0 kΩ
R_o = 5.0 kΩ

$$V_o = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

TL082

JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

- HIGH SLEW-RATE ... 13 V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

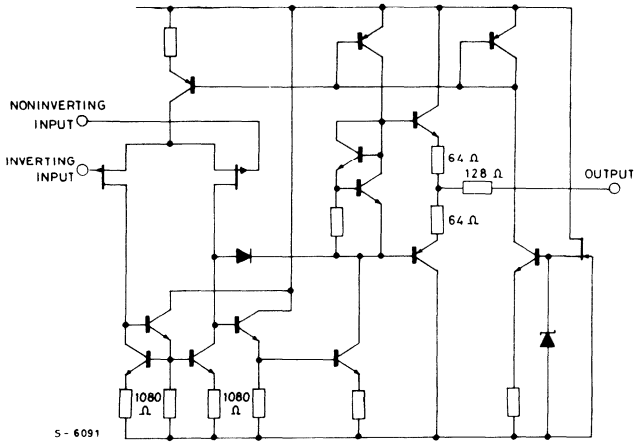
The TL082 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C. The "M" devices are characterized for operation from -55 to 125°C.

Minidip
(Plastic and Ceramic)

SO-8

SCHEMATIC DIAGRAM
(one section)



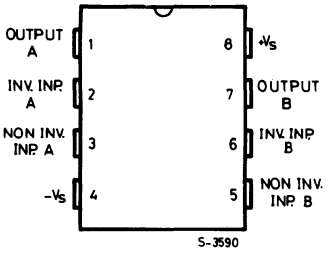
TL082

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_{is}	Differential input voltage		± 30	V
V_i	Input voltage		± 15	V
T_{op}	Operating temperature	(TL082I)	-25 to 85	°C
		(TL082C)	0 to 70	°C
		(TL082M)	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-65 to 150	°C

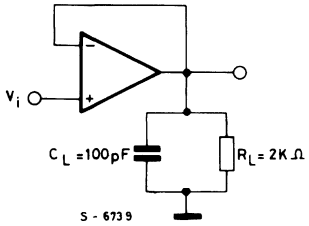
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

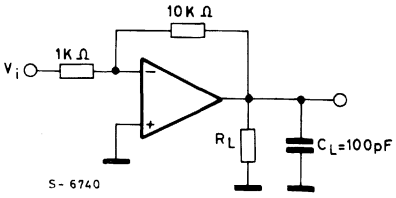


0 to 70°C	-25 to 85°C	-55 to 125°C	Package
TL082CJG TL082ACJG TL082BCJG	TL082IJG – –	TL082MJG – –	Ceramic Minidip
TL082CP TL082ACP TL082BCP	TL082IP – –	– – –	Plastic Minidip
TL082CD	TL082ID	–	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_s = 50\Omega$	TL082		3	6		5	15		3	6	mV
			TL082A					3	6				
			TL082B					2	3				
		$R_s = 50\Omega$, T_{amb} = full range	TL082			9			20			9	
			TL082A						7.5				
			TL082B						5				
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s = 50\Omega$, T_{amb} = full range			10			10			10		$\mu V/°C$
I_{OS}	Input offset current		TL082		5	100		5	200		5	100	pA
			TL082A					5	100				
			TL082B					5	100				
		T_{amb} = full range	TL082			10			5			20	nA
			TL082A						3				
			TL082B						3				
I_b	Input bias current		TL082		30	200		30	400		30	200	pA
			TL082A					30	200				
			TL082B					30	200				
		T_{amb} = full range	TL082			20			10			50	nA
			TL082A						7				
			TL082B						7				
V_{CM}	Common mode input voltage range		TL082	± 11	± 12		± 10	± 11		± 11	± 12		V
			TL082A				± 11	± 12					
			TL082B				± 11	± 12					
V_{OPP}	Large signal voltage swing		$R_L = 10K\Omega$	24	27		24	27		24	27		V
		T_{amb} = full range	$R_L \geq 10K\Omega$	24			24			24			
			$R_L \geq 2K\Omega$	20	24		20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$, $V_o = \pm 10V$	TL082	50	200		25	200					V/mV
			TL082A				50	200					
			TL082B				50	200					
		$R_L \geq 2K\Omega$, $V_o = \pm 10V$, T_{amb} = full range	TL082	25			15			15			
			TL082A				25						
			TL082B				25						
B	Unity gain bandwidth				3			3			3		MHz
R_I	Input resistance				10^{12}			10^{12}			10^{12}		Ω
CMR	Common mode	$R_s \geq 10K\Omega$	TL082	80	86		70	76		80	86		
			TL082A				80	86					
			TL082B				80	86					
SVR	Supply voltage	$R_s \geq 10K\Omega$	TL082	80	86		70	76		80	86		dB
			TL082A				80	86					
			TL082B				80	86					
I_S	Supply current	$R_L = \infty$			2.8	5.6		2.8	5.6		2.8	5.6	mA

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS	Channel separation	G_V = 100			120			120			120		dB
SR	Slew-rate at unity gain	V_I = 10V C_L = 100pF	R_L = 2KΩ		13			13		8	13		V/μs
t_r	Rise time	V_I = 20mV C_L = 100pF	R_L = 2KΩ		0.1			0.1			0.1		μs
	Overshot factor				10			10			10		%
e_N	Total input noise voltage	R_S = 100Ω f = 1KHz			25			25			25		$\frac{nV}{\sqrt{Hz}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency.

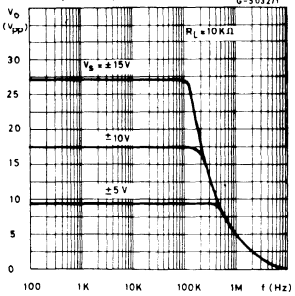


Fig. 2 - Maximum peak to peak output voltage vs. frequency.

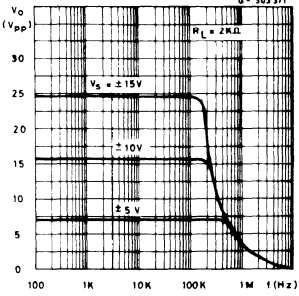


Fig. 3 - Maximum peak to peak output voltage vs. load resistance.

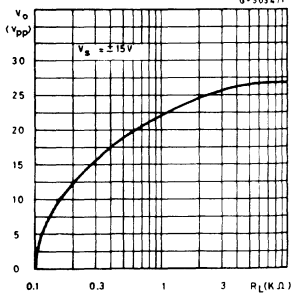


Fig. 4 - Large signal voltage gain and phase shift vs. frequency.

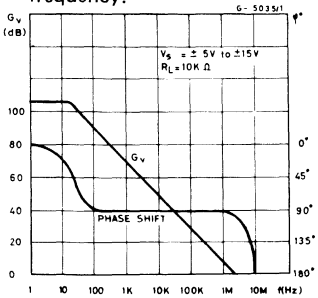


Fig. 5 - Supply current vs. temperature

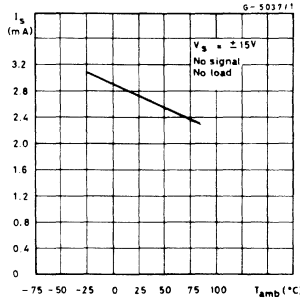


Fig. 6 - Supply current vs. supply voltage.

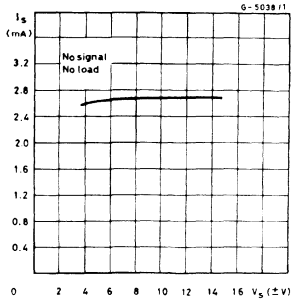


Fig. 7 - Input bias current vs. temperature.

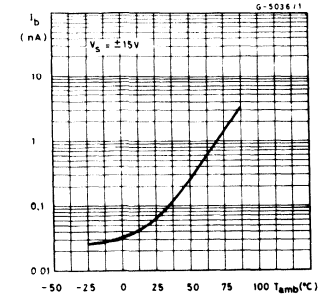


Fig. 8 - Voltage follower large signal pulse response

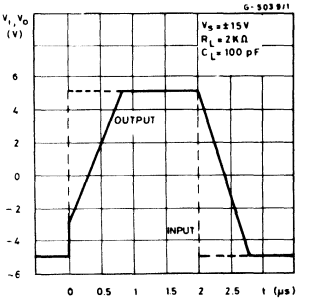


Fig. 9 - Output voltage vs. elapsed time.

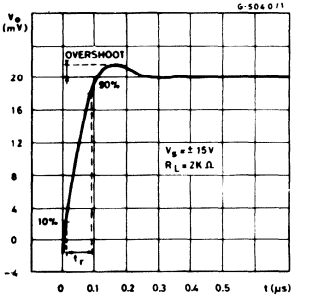


Fig. 10 - Equivalent input noise voltage vs. frequency.

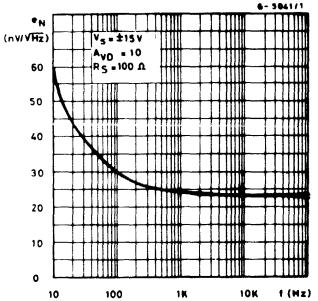


Fig. 11 - Total harmonic distortion vs. frequency.

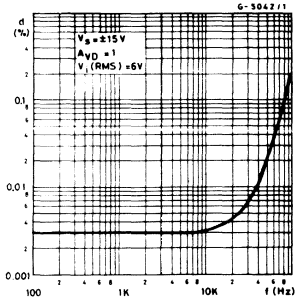
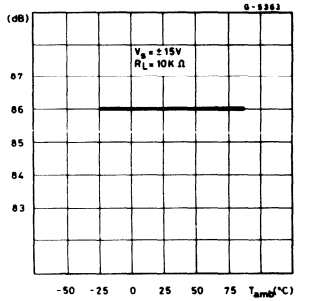
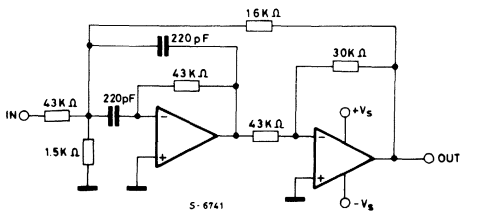


Fig. 12 - Common mode rejection vs. temperature



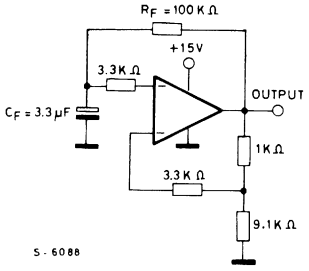
APPLICATION INFORMATION

Fig. 13 - Second order high Q band pass filter (f_o = 100 KHz, Q = 30, gain = 4)



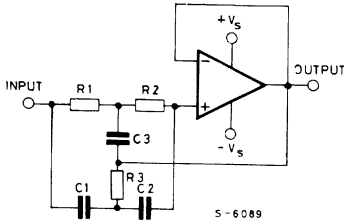
APPLICATION INFORMATION

Fig. 14 - 0.5 Hz square wave oscillator



$$f = \frac{1}{2\pi R_F C_F}$$

Fig. 15 - High Q Notch filter

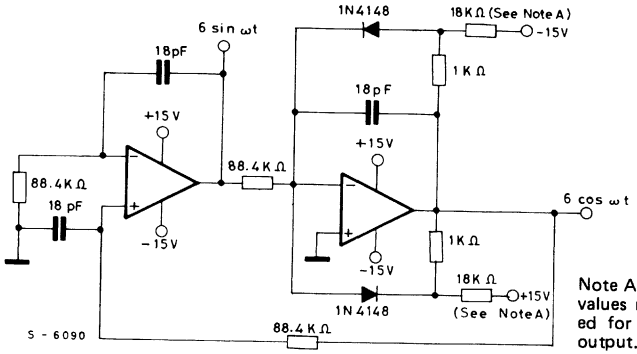


$$R1 = R2 = 2R3 = 1.5M\Omega$$

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi R1\ C1} = 1\ KHz$$

Fig. 16 - 100 KHz quadrature oscillator



Note A: These resistor values may be adjusted for a symmetrical output.

Fig. 17 - 20 Hz to 200 Hz variable High-pass filter (G_v= 3 dB)

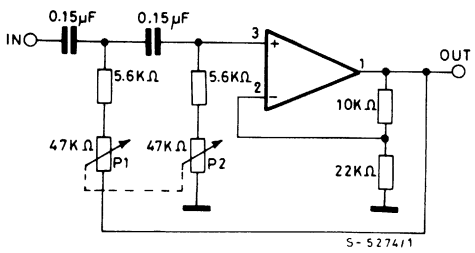
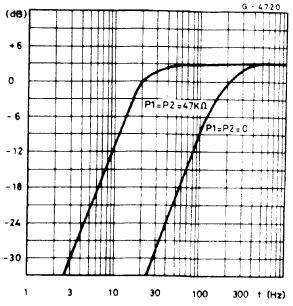


Fig. 18 - Frequency response of the high-pass filter of fig.17



APPLICATION INFORMATION (continued)

Fig. 19 - Unity-gain absolute-value circuit

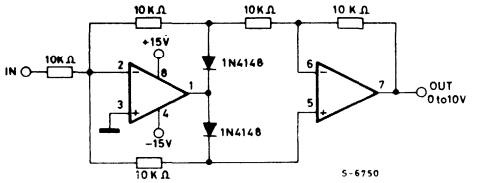


Fig. 20 - Single supply sample and hold

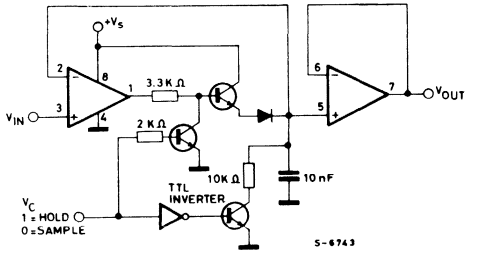
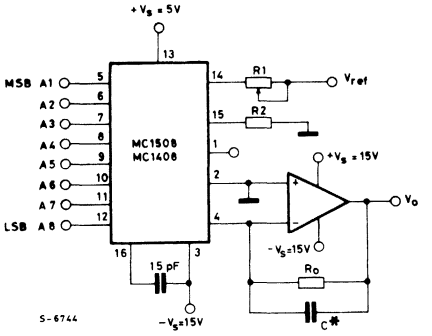


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 V_{dc}
R1 = R2 ≈ 1.0 kΩ
R_o = 5.0 kΩ

$$V_o = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

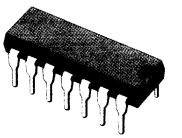
TL084

JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

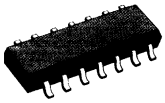
- HIGH SLEW-RATE . . . 13V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE CONNOM-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE . . . JEFT-INPUT STAGE
- LATCH-UP-FREE OPERATION

The TL084 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C. The "M" devices are characterized for operation from -55 to 125°C.

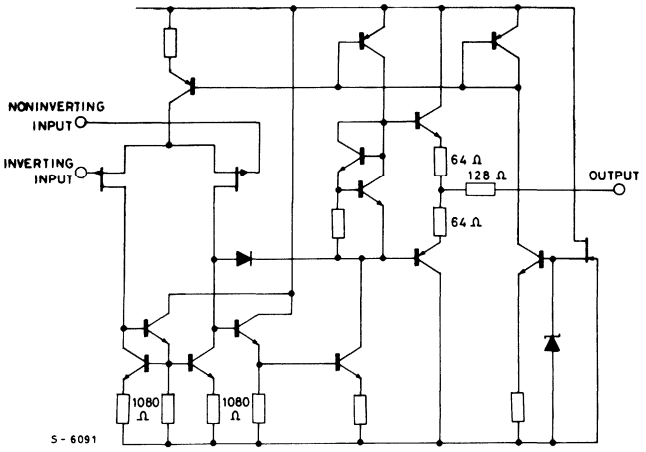


DIP-14
(Plastic and Ceramic)



SO-14J

SCHEMATIC DIAGRAM
(one section)

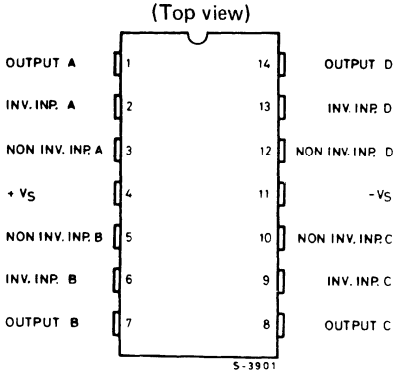


TL084

ABSOLUTE MAXIMUM RATINGS

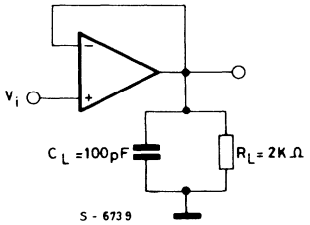
V_s	Supply voltage		± 18	V
V_{is}	Differential input voltage		± 30	V
V_i	Input voltage		± 15	V
T_{op}	Operating temperature	(TL084I)	-25 to 85	°C
		(TL084C)	0 to 70	°C
		(TL084M)	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

CONNECTION DIAGRAM AND ORDERING NUMBERS

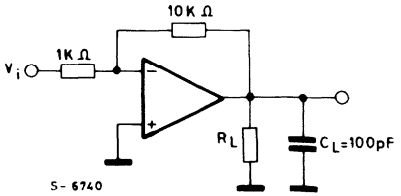


0 to 70°C	-25 + 85°C	-55 + 125°C	Package
TL084CJ TL084ACJ TL084BCJ	TL084IJ – –	TL084MJ – –	Ceramic DIP-14
TL084CN TL084ACN TL084BCN	TL084IN – –	– – –	Plastic DIP-14
TL084CD	TL084ID	–	SO-14

TEST CIRCUIT



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_s = 50\Omega$	TL084		3	6		5	15		3	9	mV
			TL084A					3	6				
			TL084B					2	3				
		$R_s = 50\Omega$, T_{amb} = full range	TL084			9			20			15	
			TL084A						7.5				
			TL084B						5				
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s = 50\Omega$, T_{amb} = full range			10			10			10		$\mu V/°C$
I_{OS}	Input offset current		TL084		5	100		5	200		5	100	pA
			TL084A					5	100				
			TL084B					5	100				
		T_{amb} = full range	TL084			10			5			20	nA
			TL084A						3				
			TL084B						3				
I_b	Input bias current		TL084		30	200		30	400		30	200	pA
			TL084A					30	200				
			TL084B					30	200				
		T_{amb} = full range	TL084			20			10			50	nA
			TL084A						7				
			TL084B						7				
V_{CM}	Common mode input voltage range		TL084	± 11	± 12		± 10	± 11		± 11	± 12		V
			TL084A				± 11	± 12					
			TL084B				± 11	± 12					
V_{OPP}	Large signal voltage gain		$R_L = 10K\Omega$	24	27		24	27		24	27		V
		T_{amb} = full range	$R_L \geq 10K\Omega$	24			24			24			
			$R_L \geq 2K\Omega$	20	24		20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$, $V_o = \pm 10V$	TL084	50	200		25	200					V/mV
			TL084A				50	200					
			TL084B				50	200					
		$R_L \geq 2K\Omega$, $V_o = \pm 10V$, T_{amb} = full range	TL084	25			15			15			
			TL084A				25						
			TL084B				25						
B	Unity gain bandwidth				3			3			3		MHz
R_I	Input resistance				10^{12}			10^{12}			10^{12}		Ω
CMR	Common mode rejection	$R_s \geq 10K\Omega$	TL084	80	86		70	76		80	86		dB
			TL084A				80	86					
			TL084B				80	86					
SVR	Supply volage rejection	$R_s \geq 10K\Omega$	TL084	80	86		70	76		80	86		dB
			TL084A				80	86					
			TL084B				80	86					
I_S	Supply current	$R_L = \infty$			5.6	11.2		5.6	11.2		5.6	11.2	mA

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	"I"			"C"			"M"			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS	Channel separation	G_V = 100		120			120			120		dB
SR	Slew-rate at unity gain	V_I = 10V, R_L = 2KΩ, C_L = 100pF		13			12		8	13		V/μs
t_r	Rise time	V_i = 20mV, R_L = 2KΩ, C_L = 100pF		0.1			0.1			0.1		μs
	Overshot factor			10			10			10		%
e_N	Total input noise Voltage	R_S = 100Ω, f = 1KHz		25			25			25		$\frac{nV}{\sqrt{Hz}}$

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

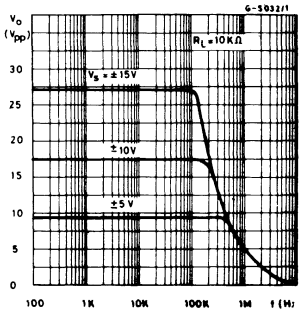


Fig. 2 – Maximum peak to peak output voltage vs. frequency

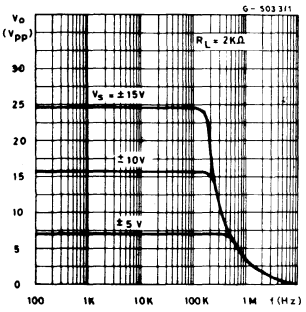


Fig. 3 – Maximum peak to peak output voltage vs. load resistance.

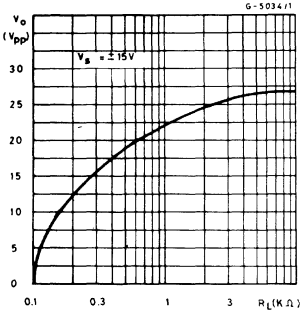


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

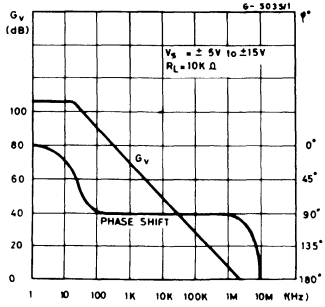


Fig. 5 – Supply current vs. temperature

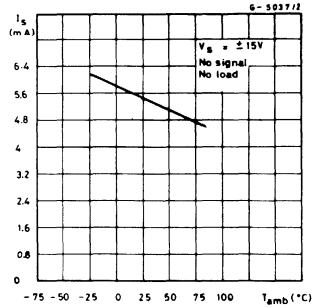


Fig. 6 – Supply current vs. supply voltage

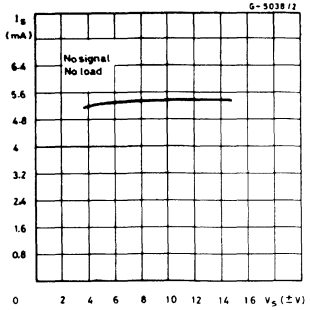


Fig. 7 – Input bias current vs. temperature

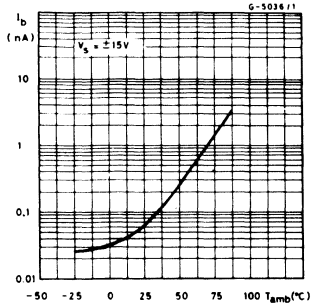


Fig. 8 – Voltage follower large signal pulse response

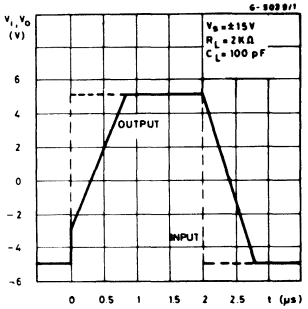


Fig. 9 – Output voltage vs. elapset time.

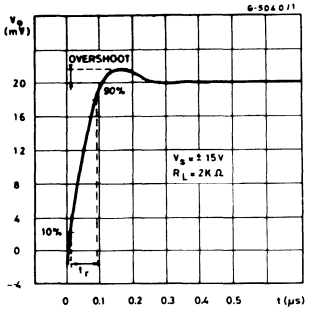


Fig. 10 – Equivalent input noise voltage vs. frequency

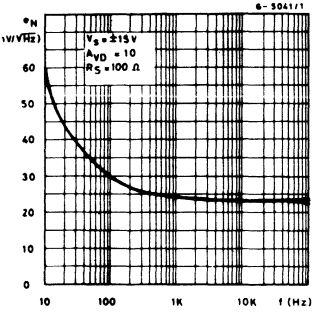


Fig. 11 Total harmonic distortion vs. frequency

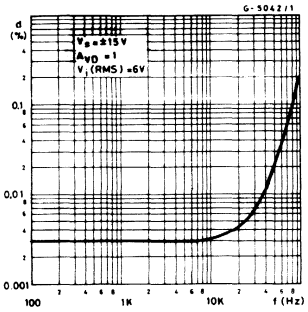
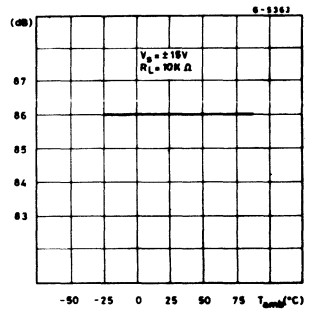
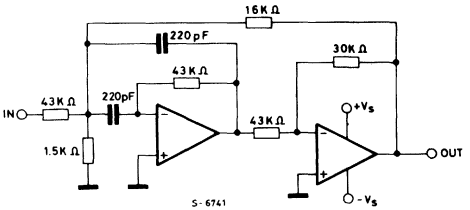


Fig. 12 – Common mode rejection vs. temperature



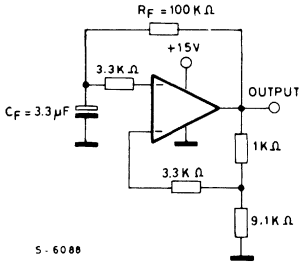
APPLICATION INFORMATION

Fig. 13 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)



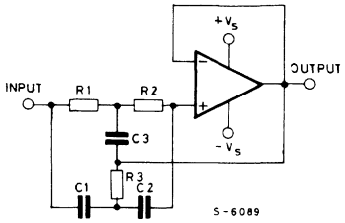
APPLICATION INFORMATION

Fig. 14 - 0.5 Hz square wave oscillator



$$f = \frac{1}{2\pi R_F C_F}$$

Fig. 15 - High Q Notch filter

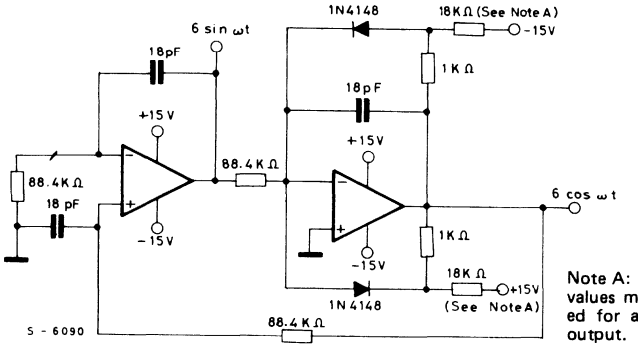


$$R1 = R2 = 2R3 = 1.5M\Omega$$

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi R1\ C1} = 1\ KHz$$

Fig. 16 - 100 KHz quadrature oscillator



Note A: These resistor values may be adjusted for a symmetrical output.

Fig. 17 - 20 Hz to 200 Hz variable High-pass filter (G_V= 3 dB)

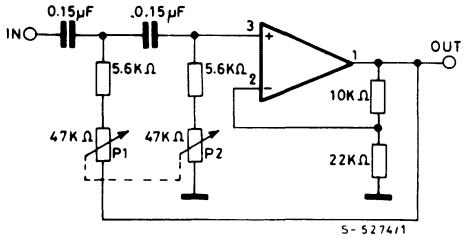
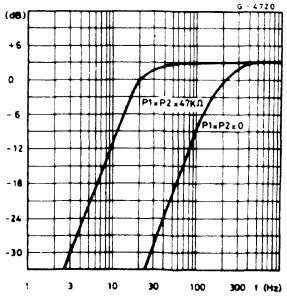


Fig. 18 - Frequency response of the high-pass filter of fig.17



APPLICATION INFORMATION (continued)

Fig. 19 – Unity-gain absolute-value circuit

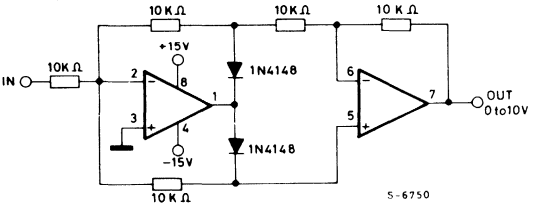


Fig. 20 – Single supply sample and hold

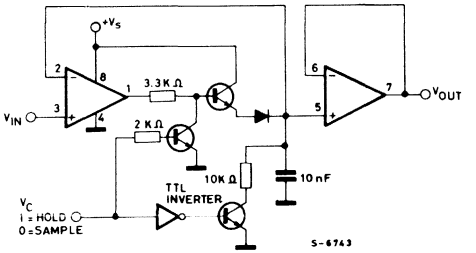
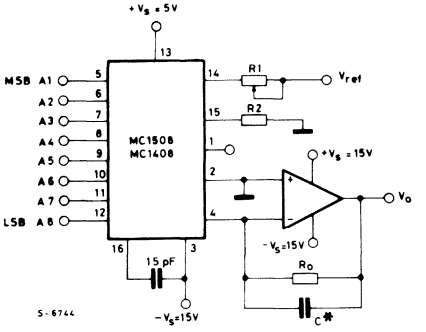


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

DISCRETE POWER DATASHEETS

BDV64 BDV65
BDV64A BDV65A
BDV64B BDV65B

POWER DARLINGTONS

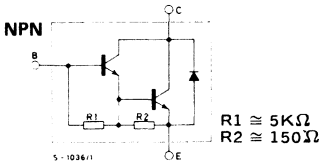
The BDV65, BDV65A, BDV65B, are silicon epitaxial-base NPN transistors in monolithic Darlington configuration and are mounted in SOT-93 plastic package. They are intended for use in power linear and switching applications.
The complementary PNP types are BDV64, BDV64A, BDV64B respectively.

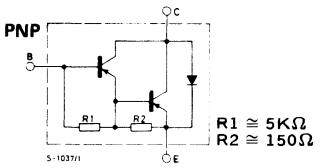
ABSOLUTE MAXIMUM RATINGS

		* PNP / NPN	BDV64 / BDV65	BDV64A / BDV65A	BDV64B / BDV65B
V_{CBO}	Collector-base voltage ($I_E = 0$)		60V	80V	100V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)		60V	80V	100V
V_{EBO}	Emitter-base voltage ($I_C = 0$)		5V		
I_C	Collector current		12A		
I_{CM}	Collector peak current (repetitive)		20A		
I_B	Base current		0.5A		
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$		125W		
T_{stg}	Storage temperature		-65 to 150°C		
T_j	Junction temperature		150°C		

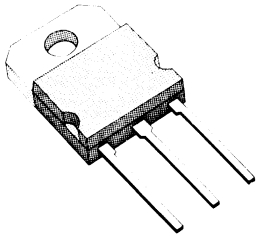
* For PNP types voltage and current values are negative

INTERNAL SCHEMATIC DIAGRAMS





SOT-93 (TO-218)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max. 1 °C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	for **BDV64/5** V_{CB} = 60V			400	μA
		for **BDV64A/5A** V_{CB} = 80V			400	μA
		for **BDV64B/5B** V_{CB} = 100V			400	μA
		T_{case} = 150°C				
		for **BDV64/65** V_{CB} = 30V			2	mA
		for **BDV64A/5A** V_{CB} = 40V			2	mA
		for **BDV64B/5B** V_{CB} = 50V			2	mA
I_{CEO}	Collector cutoff current (I_B = 0)	for **BDV64/65** V_{CE} = 30V			1	mA
		for **BDV64A/5A** V_{CE} = 40V			1	mA
		for **BDV64B/5B** V_{CE} = 50V			1	mA
I_{EBO}	Emitter cutoff current (I_C = 0)	V_{EBO} = 5V			5	mA
$V_{CEO(sus)}$ *	Collector-emitter sustaining voltage (I_B = 0)	I_C = 30mA				
		for **BDV64/65**	60			V
		for **BDV64A/5A**	80			V
		for **BDV64B/5B**	100			V
$V_{CE(sat)}$ *	Collector-emitter saturation voltage	I_C = 5A I_B = 20mA			2	V
V_{BE} *	Base-emitter voltage	I_C = 5A V_{CE} = 4V			2.5	V
h_{FE} *	DC current gain	I_C = 1A V_{CE} = 4V		2500		–
		I_C = 5A V_{CE} = 4V	1000			–
		I_C = 10A V_{CE} = 4V		500		–
V_F	Parallel diode forward voltage	I_F = 5A		1.2		V

ELECTRICAL CHARACTERISTICS (continued)

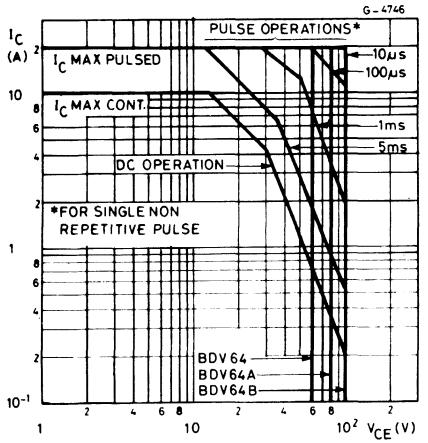
Parameter		Test conditions		Min.	Typ.	Max.	Unit
h_{fe}	Small signal current gain	I_C = 5A f = 1 MHz	V_{CE} = 4V	60			–
C_{CBO}	Collector-base capacitance	V_{CB} = 10V f = 1 MHz	I_E = 0		100		pF
t_{on}	Turn-on time	I_C = 5A I_{B2} = 20A	I_{B1} = 20mA V_{CC} = 16V		0.5		μs
t_s	Storage time				1.1 1.3	** 	μs μs
t_f	Fall time				2.5 1.0	** 	μs μs

* Pulsed: pulse duration = 300 μs duty cycle = 1.5%

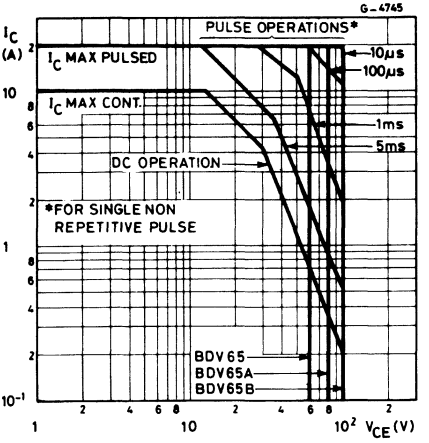
** For PNP types

For PNP types voltage and current values are negative

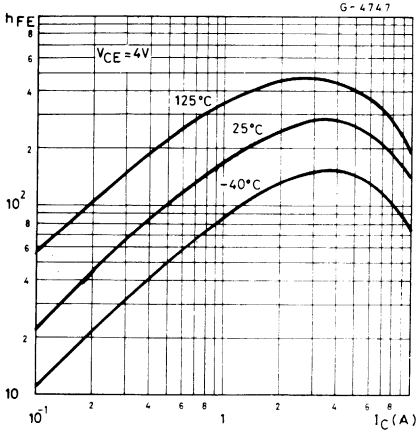
Safe operating areas



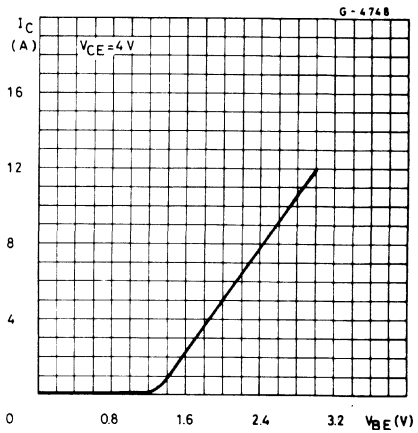
Safe operating areas



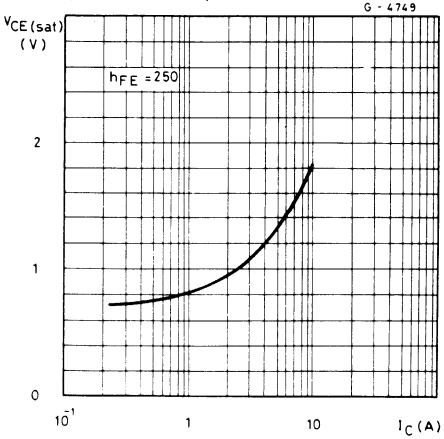
DC current gain (BDV64 series)



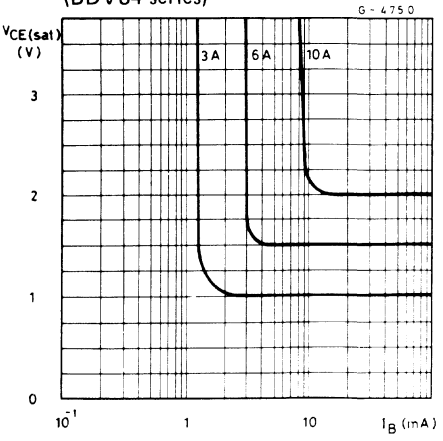
DC transconductance (BDV64 series)



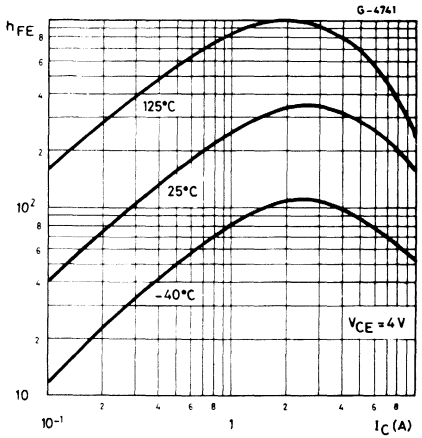
Collector-emitter saturation voltage (BDV64 series)



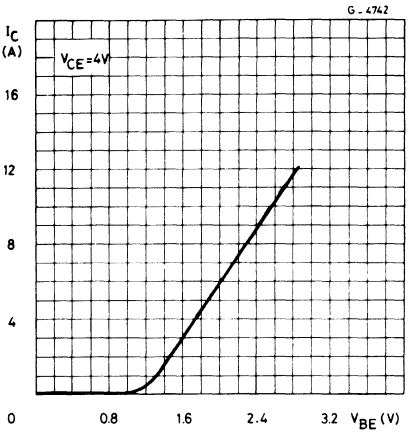
Collector-emitter saturation voltage (BDV64 series)



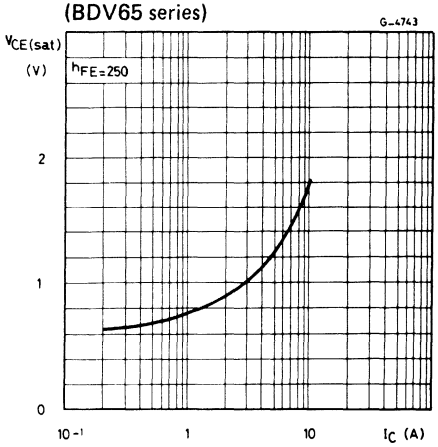
DC current gain (BDV65 series)



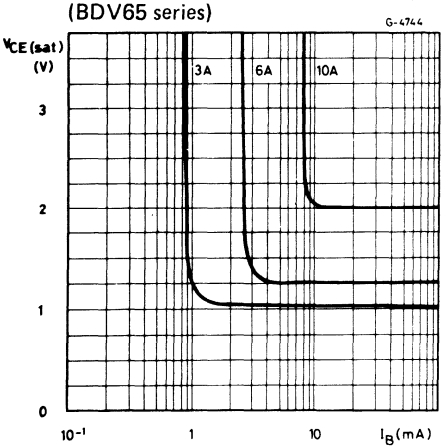
DC transconductance (BDV65 series)



Collector-emitter saturation voltage (BDV65 series)



Collector-emitter saturation voltage (BDV65 series)



POWER DARLINGTONS

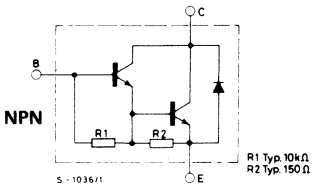
The BDW 93, BDW 93A, BDW 93B and BDW 93C are silicon epitaxial-base NPN transistors in monolithic Darlington configuration and are mounted in Jedec TO-220 plastic package. They are intended for use in power linear and switching applications. The complementary PNP types are the BDW 94, BDW 94A, BDW 94B and BDW 94C respectively.

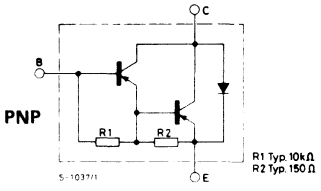
ABSOLUTE MAXIMUM RATINGS

		NPN / PNP*	BDW93 / BDW94	BDW93A / BDW94A	BDW93B / BDW94B	BDW93C / BDW94C
V_{CBO}	Collector-base voltage ($I_E = 0$)		45V	60V	80V	100V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)		45V	60V	80V	100V
I_C	Collector current		12A			
I_{CM}	Collector peak current		15A			
I_B	Base current		0.2A			
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$		80W			
T_{stg}	Storage temperature		-65 to 150°C			
T_j	Junction temperature		150°C			

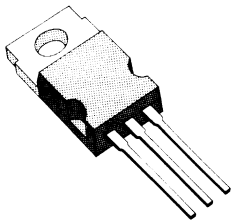
*** For PNP types voltage and current values are negative**

INTERNAL SCHEMATIC DIAGRAMS





TO-220 (Discrete Power)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1.56	°C/W

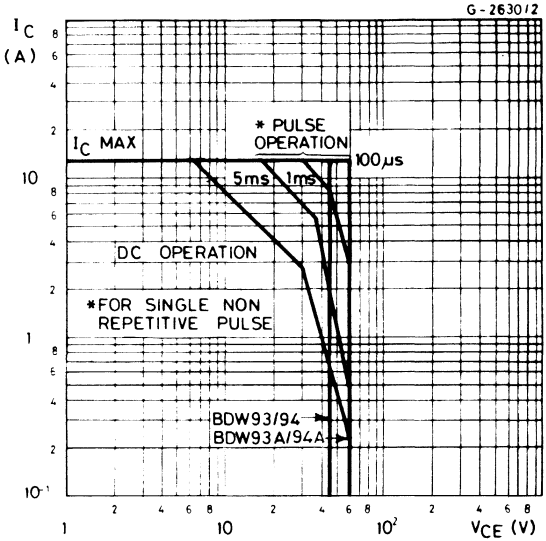
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
I_{CBO}	Collector cutoff current ($I_E = 0$)	for **BDW93/94** V_{CB} = 45V			100	μA
		for **BDW93A/94A** V_{CB} = 60V			100	μA
		for **BDW93B/94B** V_{CB} = 80V			100	μA
		for **BDW93C/94C** V_{CB} = 100V			100	μA
		T_{case} = 150°C				
		for **BDW93/94** V_{CB} = 45V			5	mA
		for **BDW93A/94A** V_{CB} = 60V			5	mA
		for **BDW93B/94B** V_{CB} = 80V			5	mA
		for **BDW93C/94C** V_{CB} = 100V			5	mA
I_{CEO}	Collector cutoff current ($I_B = 0$)	for **BDW93/94** V_{CE} = 40V			1	mA
		for **BDW93A/94A** V_{CE} = 60V			1	mA
		for **BDW93B/94B** V_{CE} = 80V			1	mA
		for **BDW93C/94C** V_{CE} = 80V			1	mA
I_{EBO}	Emitter cutoff current ($I_C = 0$)	V_{EB} = 5V			2	mA
$V_{CEO\ (sus)}$*	Collector-emitter sustaining voltage ($I_B = 0$)	I_C = 100mA				
		for **BDW93/94**	45			V
		for **BDW93A/94A**	60			V
		for **BDW93B/94B**	80			V
		for **BDW93C/94C**	100			V
$V_{CE\ (sat)}$*	Collector-emitter saturation voltage	I_C = 5A I_B = 20mA			2	V
		I_C = 10A I_B = 100mA			3	V
$V_{BE\ (sat)}$*	Base-emitter saturation voltage	I_C = 5A I_B = 20mA			2.5	V
		I_C = 10A I_B = 100mA			4	V
h_{FE}*	DC current gain	I_C = 3A V_{CE} = 3V	1000			—
		I_C = 5A V_{CE} = 3V	750		20000	—
		I_C = 10A V_{CE} = 3V	100			—
V_F*	Parallel-diode forward voltage	I_F = 5A		1.3	2	V
		I_F = 10A		1.8	4	V
h_{fe}	Small signal current gain	I_C = 1A V_{CE} = 10V				
		f = 1 MHz	20			—

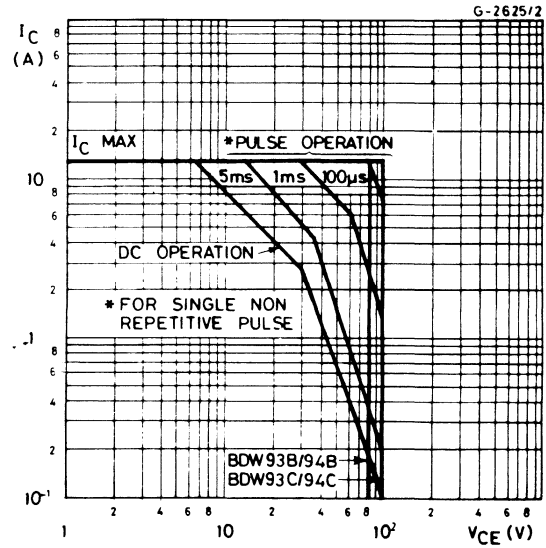
* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%

For PNP types voltage and current values are negative

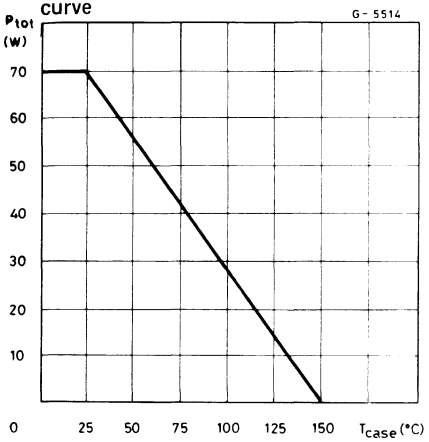
Safe operating areas
(for **BDW93, BDW93A, BDW94, BDW94A)**



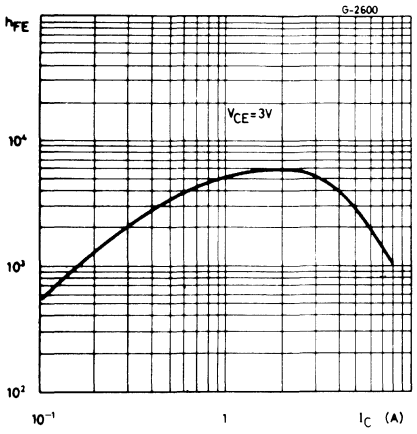
Safe operating areas
(for **BDW93B, BDW93C BDW94B, BDW94C)**



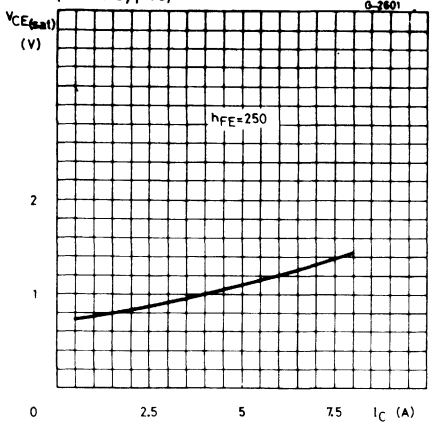
Case temperature dissipation derating curve



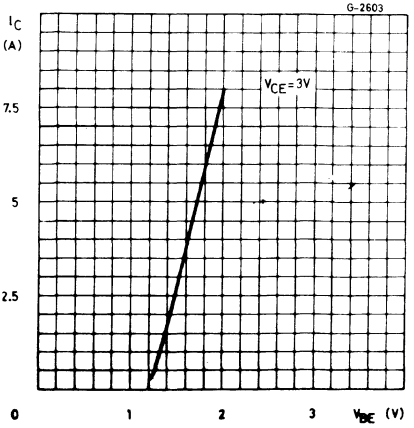
DC current gain (NPN types)



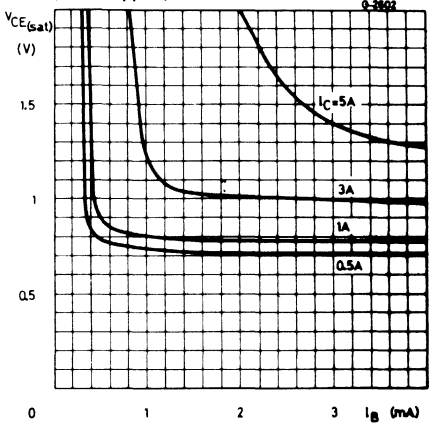
Collector-emitter saturation voltage (NPN types)



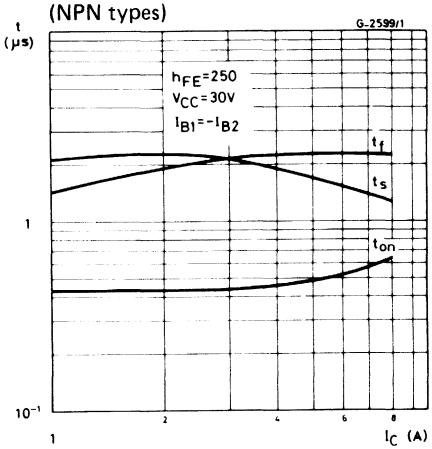
DC transconductance (NPN types)



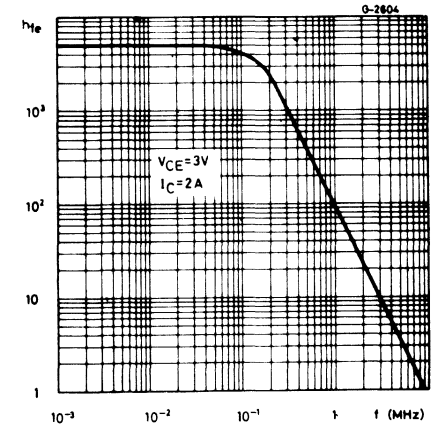
Collector-emitter saturation voltage (NPN types)



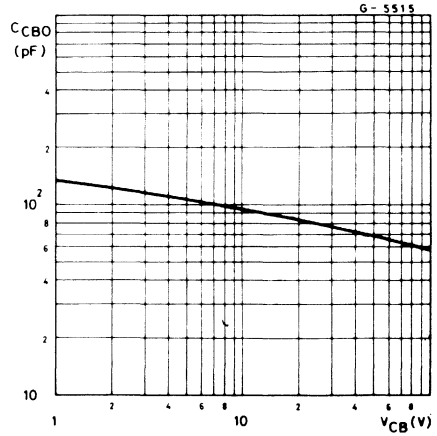
Saturated switching characteristics) (NPN types)



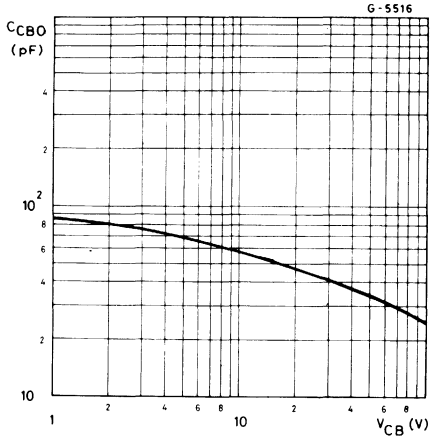
Small signal current gain (NPN types)



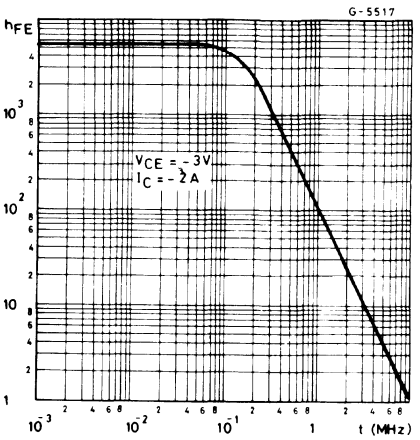
Collector-base capacitance (PNP types)



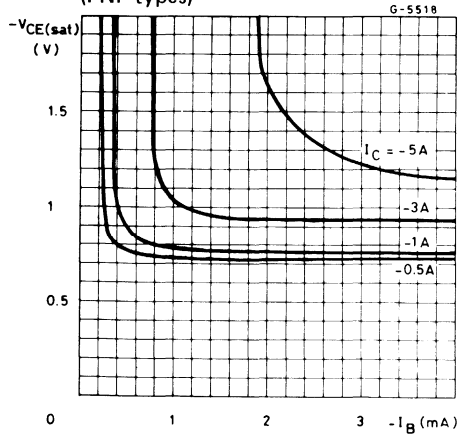
Collector-base capacitance (NPN types)



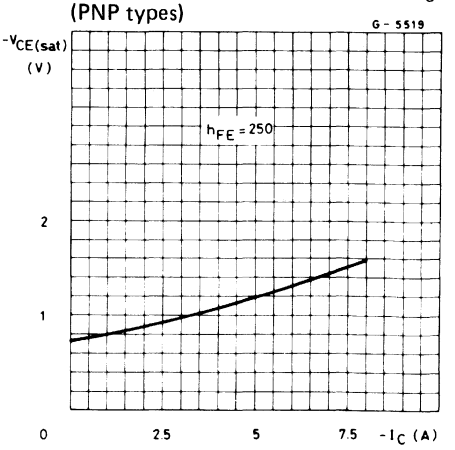
Small signal current gain (PNP types)



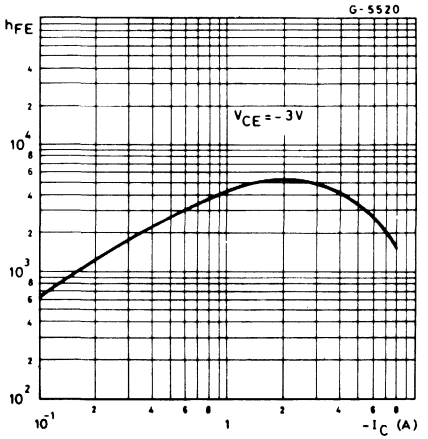
Collector-emitter saturation voltage (PNP types)



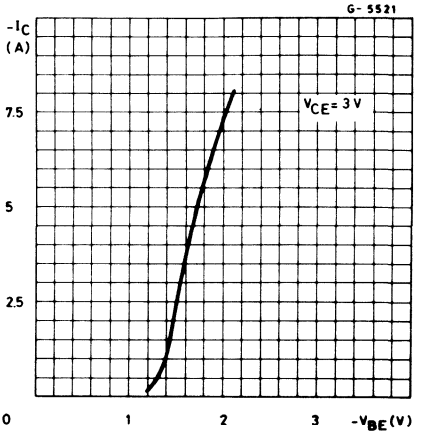
Collector-emitter saturation voltage (PNP types)



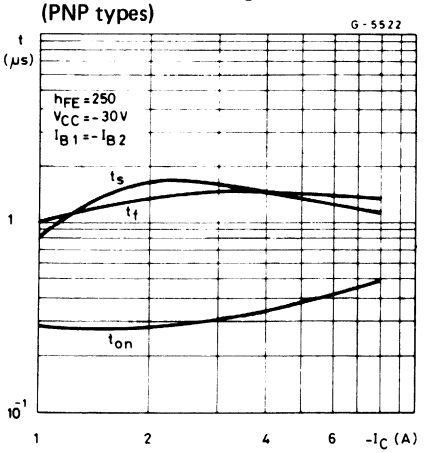
DC current gain (PNP types)



DC transconductance (PNP types)



Saturated switching characteristics (PNP types)



BUZ11
BUZ11P

HIGH SPEED SWITCHING APPLICATIONS

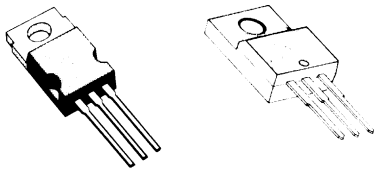
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ11	50 V	0.04 Ω	30 A
BUZ11P	50 V	0.04 Ω	20 A

- N- CHANNEL POWER MOS TRANSISTORS
- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO

APPLICATIONS:

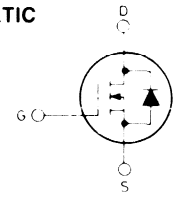
- AUTOMOTIVE POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. They also find use in DC/DC converters and uninterruptable power supplies.



TO-220 ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 ISOWATT220	BUZ11 BUZ11P	
V_{DS}	Drain-source voltage (V_{GS} = 0)		50	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		50	V
V_{GS}	Gate-source voltage		± 20	V
I_{DM}	Drain current (pulsed) T_c = 25°C		120	A
		BUZ11	BUZ11P	
I_D ■	Drain current (continuous) T_c = 30°C	30	20	A
P_{tot} ■	Total dissipation at T_c < 25°C	75	35	W
T_{stg}	Storage temperature		− 55 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT220 in this datasheet

BUZ11
BUZ11P

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 1 mA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125°C		20 100	250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 15A		0.03	0.04	Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 15A	4	8		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1MHz V_{GS} = 0		1500 750 250	2000 1100 400	pF pF pF

■ See note on ISOWATT220 in this datasheet

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SWITCHING							
$t_{d\ (on)}$	Turn-on time	$V_{DD} = 30$ V	$I_D = 3A$		30	45	ns
t_r	Rise time	$R_{GS} = 50\ \Omega$	$I_D = 10V$		70	110	ns
$t_{d\ (off)}$	Turn-off delay time				180	230	ns
t_f	Fall time				130	170	ns
SOURCE DRAIN DIODE							
I_{SD}	Source-drain current					30	A
I_{SDM}	Source-drain current (pulsed)					120	A
V_{SD}	Forward on voltage	$I_{SD} = 60$ A	$V_{GS} = 0$		1.7	2.6	V
t_{rr}	Reverse recovery time				200		ns
Q_{rr}	Reverse recovered charge	$I_{SD} = 30A$	$di/dt = 100\ A/\mu s$		0.25		μC

BUZ11
BUZ11P

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} = \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

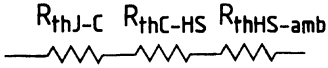
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

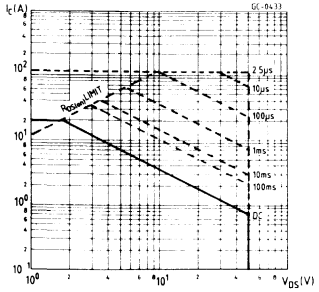
$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

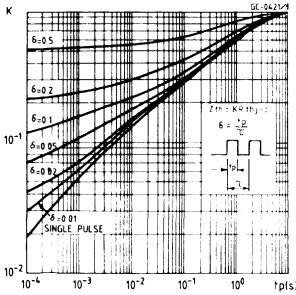
Fig. 1



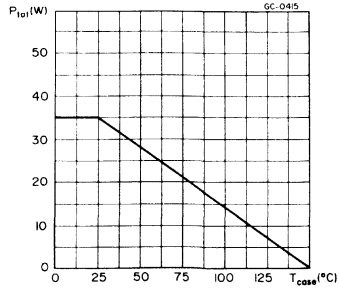
Safe operating areas



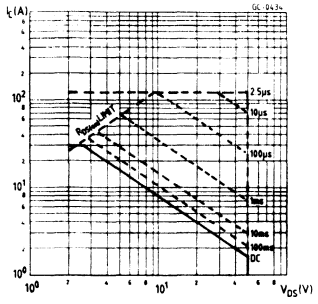
Thermal impedance



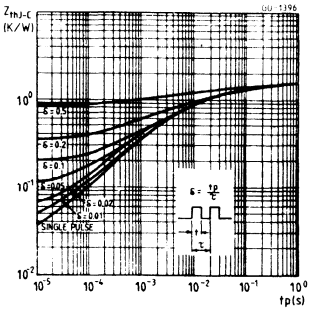
Derating curve



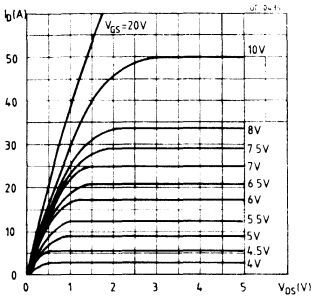
Safe operating areas



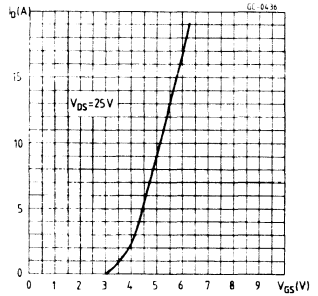
Thermal impedance



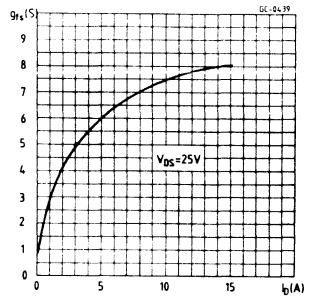
Output characteristics



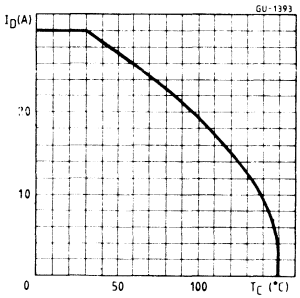
Transfer characteristics



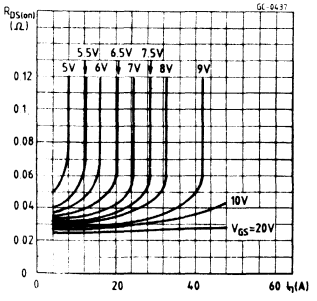
Transconductance



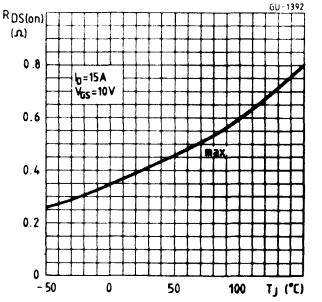
Maximum drain current vs temperature



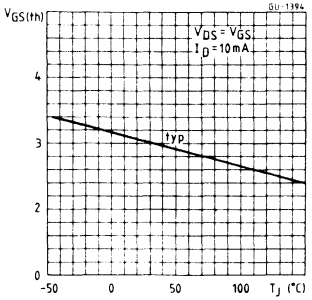
Static drain-source on resistance



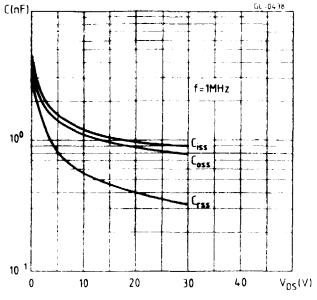
Drain-source on resitance vs temperature



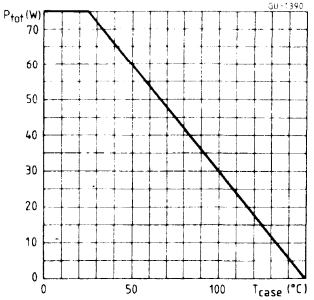
Gate threshold voltage vs temperature



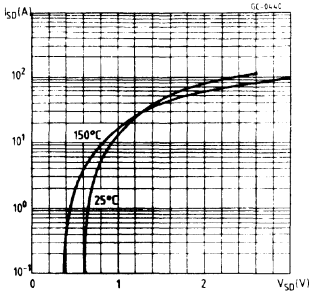
Capacitance variation



Derating curve



Source-drain diode forward characteristics



BUZ71
BUZ71P

HIGH SPEED SWITCHING APPLICATIONS

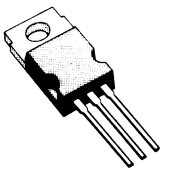
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ71	50 V	0.1 Ω	12 A
BUZ71P	50 V	0.1 Ω	10 A

- N- CHANNEL POWER MOS TRANSISTORS
- VERY FAST SWITCHING
- LOW DRIVE ENERGY FOR EASY DRIVE, REDUCED SIZE AND COST
- HIGH PULSED CURRENT - 48A FOR POWER APPLICATIONS

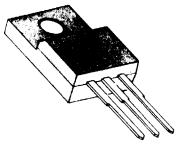
APPLICATIONS:

- POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators and many other uses in industrial automotive control applications. They also find use in DC/DC converters and uninterruptable power supplies.

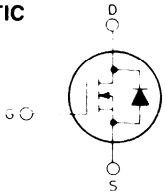


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 ISOWATT-220	BUZ71 BUZ71P	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)		50	V
V_{GS}	Gate-source voltage		±20	V
I_{DM}	Drain current (pulsed) $T_c=25°C$		48	A
		BUZ71	**BUZ71P**	
I_D ■	Drain current (continuous) $T_c=60°C$	12	10	A
P_{tot} ■	Total dissipation at $T_c<25°C$	40	30	W
T_{stg}	Storage temperature		−55 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT220 in this datasheet

BUZ71
BUZ71P

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.1	4.16	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 1 mA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125°C		25 50	250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V		±10	±100	nA
ON						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 10 mA	2.1	3.2	4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 6A		0.09	0.1	Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 6A	3	4.8		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1MHz V_{GS} = 0		480 280 160	650 450 280	pF pF pF

■ See note on ISOWATT220 in this datasheet

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SWITCHING							
$t_{d\ (on)}$	Turn-on time	$V_{DD} = 30$ V	$I_D = 3$A		20	30	ns
t_r	Rise time	$R_{GS} = 50\ \Omega$	$I_D = 10$V		55	85	ns
$t_{d\ (off)}$	Turn-off delay time				70	90	ns
t_f	Fall time				80	110	ns
SOURCE DRAIN DIODE							
I_{SD}	Source-drain current					12	A
I_{SDM}	Source-drain current (pulsed)					48	A
V_{SD}	Forward on voltage	$I_{SD} = 24$ A	$V_{GS} = 0$		1.6	2.2	V
t_{rr}	Reverse recovery time				120		ns
Q_{rr}	Reverse recovered charge	$I_{SD} = 12$A	di/dt = 100 Aμ		0.15		μC

BUZ71
BUZ71P

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} = \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

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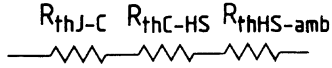
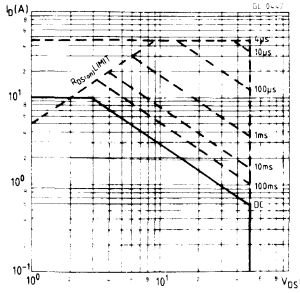
$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

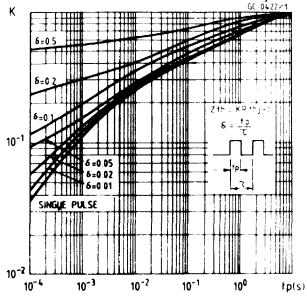
Fig. 1



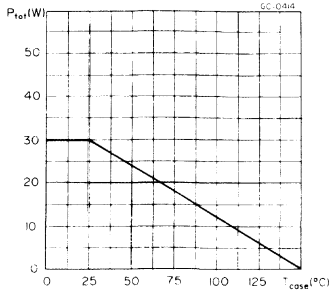
Safe operating areas



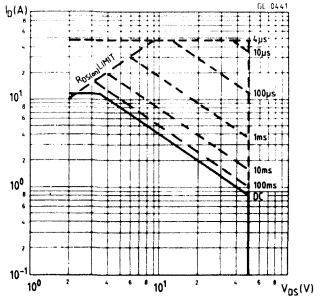
Thermal impedance



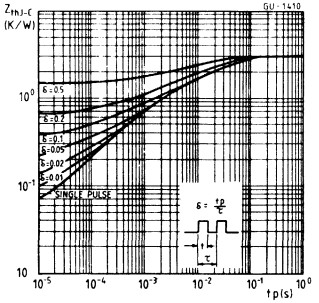
Derating curve



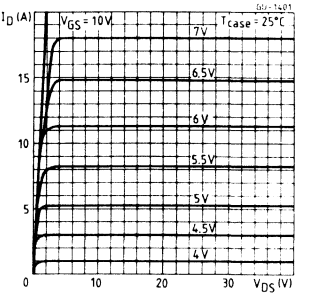
Safe operating areas



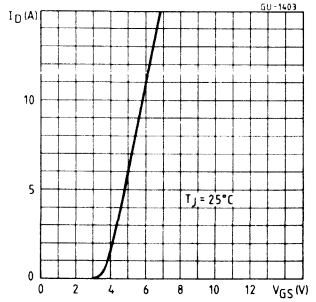
Thermal impedance



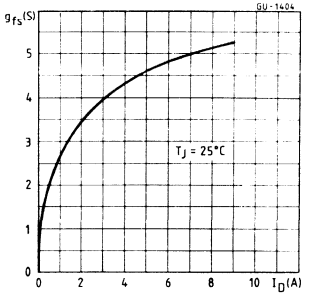
Output characteristics



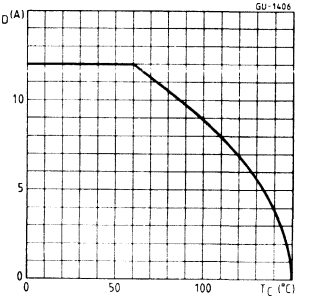
Transfer characteristics



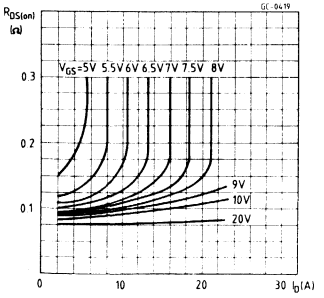
Transconductance



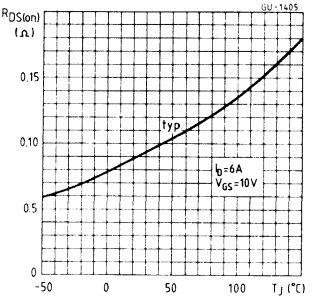
Maximum drain current vs temperature



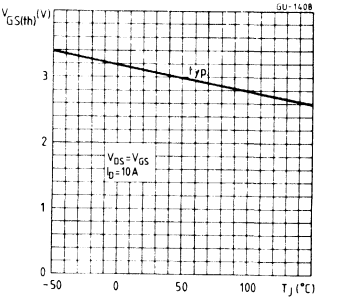
Static drain-source on resistance



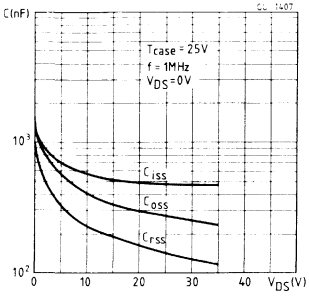
Drain-source on resitance vs temperature



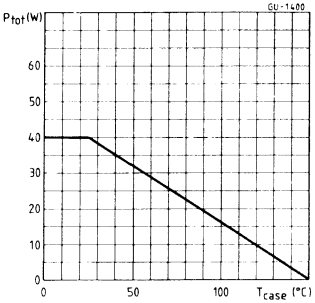
Gate threshold voltage vs temperature



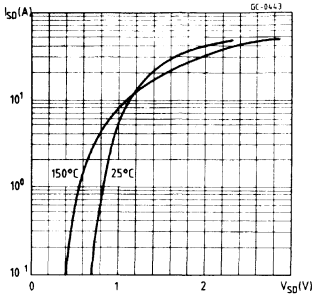
Capacitance variation



Derating curve



Source-drain diode forward characteristics



IRFZ20
IRFZ20P

HIGH SPEED SWITCHING APPLICATIONS

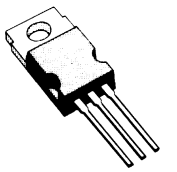
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRFZ20	50 V	0.1 Ω	15 A
IRFZ20P	50 V	0.1 Ω	12.5 A
IRFZ22	50 V	0.12 Ω	14 A
IRFZ22P	50 V	0.12 Ω	12 A

- N- CHANNEL POWERMOS TRANSISTORS
- VERY LOW $R_{DS\ (on)}$
- LOW DRIVE ENERGY FOR EASY DRIVE
- COST EFFECTIVE

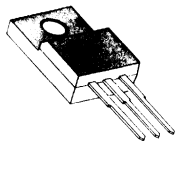
HIGH POWER INDUSTRIAL APPLICATIONS:

- AUTOMOTIVE POWER ACTUATORS
- MOTOR CONTROLS
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive and automatic guided vehicle applications. They also use in DC/DC converters and uninterruptable power supplies.

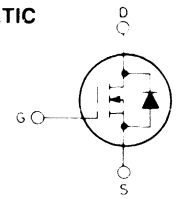


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 ISOWATT220	IRF Z20 Z20P	IRF Z22 Z22P	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		50		V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		50		V
V_{GS}	Gate-source voltage		± 20		V
I_{DM} (•)	Drain current (pulsed)		60	56	A
I_{DLM}	Drain inductive current, clamped (L = 100/μH)		60	56	A
			Z20	**Z22**	
I_D	Drain current (cont.) at T_c = 25°C		15	14	A
I_D	Drain current (cont.) at T_c = 100°C		10	9	A
			Z20P	**Z22P**	
I_D ■	Drain current (cont.) at T_c = 25°C		12.5	12	A
I_D ■	Drain current (cont.) at T_c = 100°C		7.5	7	A
		TO-220	**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C	40	30		W
■	Derating factor	0.32	0.24		W/°C
T_{stg}	Storage temperature	− 55 to 150			°C
T_j	Max. operating junction temperature	150			°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature

■ See note on ISOWATT220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	1		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 V	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON**						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max}$ V_{GS} = 10 V for **IRFZ20/IRFZ20P** for **IRFZ22/IRFZ22P**	 15 14			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 9.0A for **IRFZ20/IRFZ20P** for **IRFZ22/IRFZ22P**		 0.08 0.11	 0.10 0.12	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D(on)}$ × $R_{DS(on)\ max}$ I_D = 9.0A	5	6		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1MHz V_{GS} = 0		560 250 60	850 350 100	pF pF pF

** Pulsed: Pulse duration ≤ 300μs, duty cycle ≤ 2%

■ See note on ISOWATT220 in this datasheet

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 25 V I_D = 9.0A		15	30	ns
t_r	Rise time	Z_o = 50 Ω		45	90	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		20	40	ns
t_f	Fall time			15	30	ns
Q_g	Total gate charge	V_{GS} = 10V I_D = 20 A		12	17	nC
Q_{gs}	Gate-source charge	V_{DS} = Max Rating × 0.8		9		nC
Q_{gd}	Gate-drain charge	(see test circuit)		3		nC
L_D	Internal drain inductance	Measured from the contact screw on tab to center of die		3.5		nH
L_D	Internal drain inductance	Measured from the drain lead 6mm from package to center of die		4.5		nH
L_S	Internal source inductance	Measured from the source lead 6mm from package to source bonding pad		7.5		nH
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **IRFZ20/IRFZ20P**			15	A
		for **IRFZ22/IRFZ22P**			14	A
I_{SDM} (•)	Source-drain current (pulsed)	for **IRFZ20/IRFZ20P**			60	A
		for **IRFZ22/IRFZ22P**			56	A
V_{SD} **	Forward on voltage	V_{GS} = 0				
		for **IRFZ20/IRFZ20P** I_{SD} = 15 A			1.25	V
		for **IRFZ22/IRFZ22P** I_{SD} = 14 A			1.1	V
t_{rr}	Reverse recovery time	T_j = 150°C		100		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 15A di/dt = 100 A/μs		0.4		μC

** Pulsed: Pulse duration ≤ 300μs. duty cycle ≤ 2%
(•) Repetitive Rating: Pulse width limited by max junction temperature

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} = \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

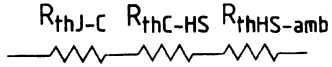
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

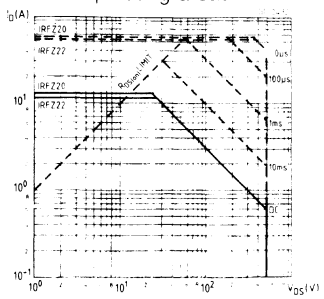
$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

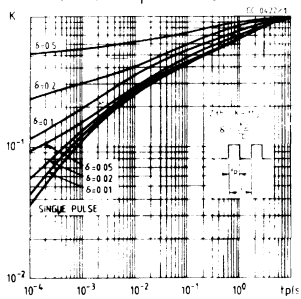
Fig. 1



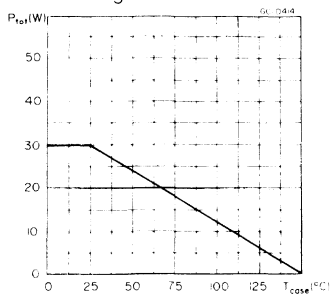
Safe operating areas



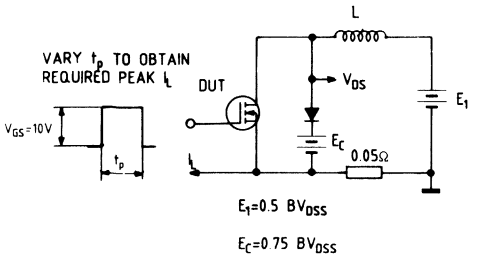
Thermal impedance



Derating curve

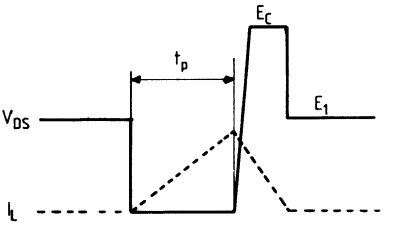


Clamped inductive test circuit



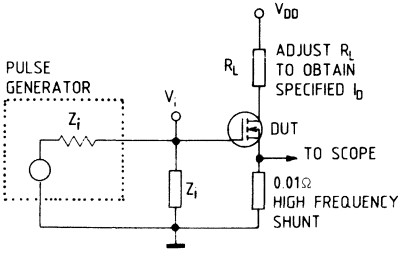
SC-0242

Clamped inductive waferforms



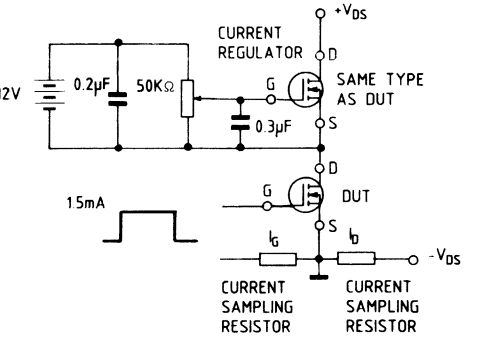
SC-0243

Switching times test circuit



SC-0245

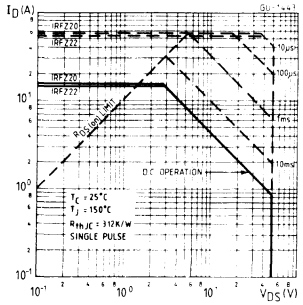
Gate charge test circuit



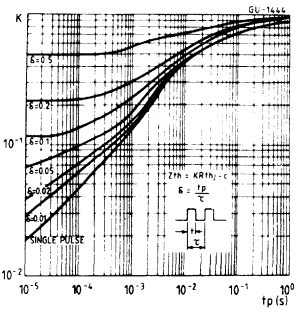
SC-0244

IRFZ20
IRFZ20P

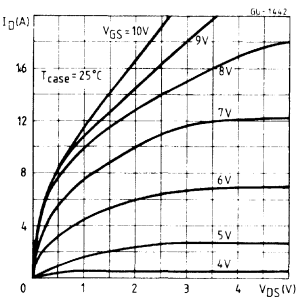
Safe operating areas



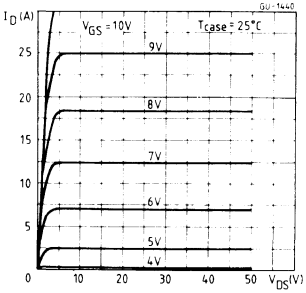
Thermal impedance



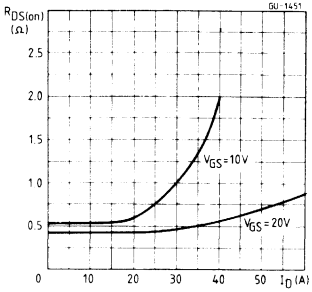
Output characteristics



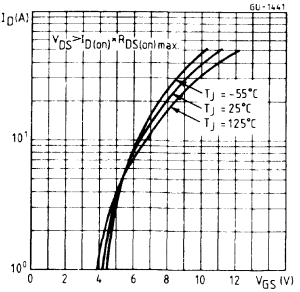
Output characteristics



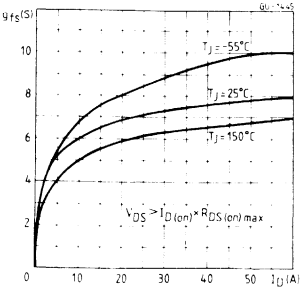
Static drain-source on resistance



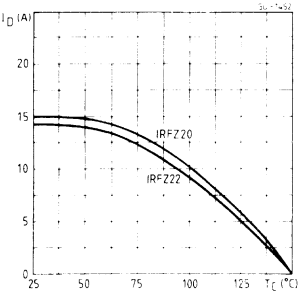
Transfer characteristics



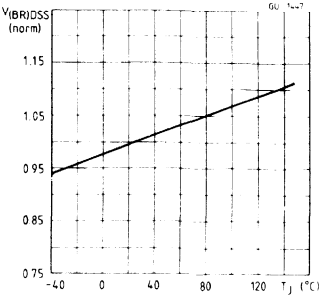
Transconductance



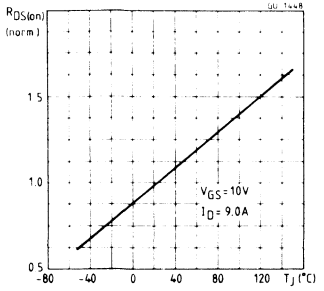
Maximum drain current vs temperature



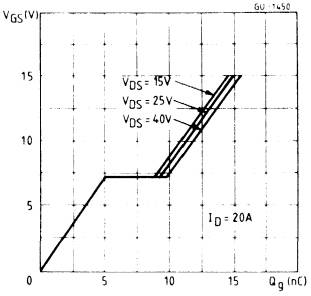
Normalized breakdown voltage vs temperature



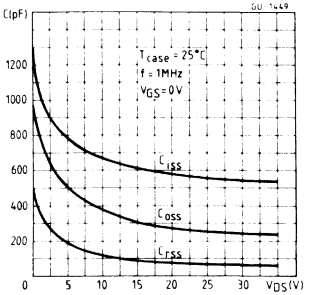
Normalized on resistance vs temperature



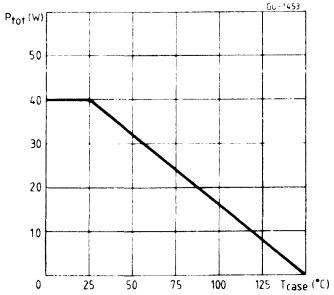
Gate charge vs gate source voltage



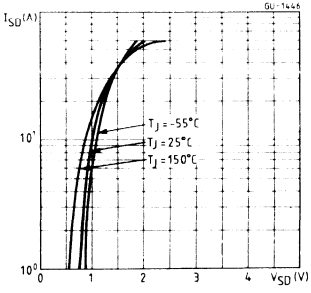
Capacitance variation



Derating curve



Source-drain diode forward characteristics



MJ11011 MJ11012
MJ11013 MJ11014
MJ11015 MJ11016

COMPLEMENTARY POWER DARLINGTONS

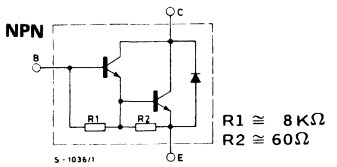
The MJ11011/12/13/14/15/16 are epitaxial-base silicon transistors in monolithic Darlington configuration in Jedec TO-3 metal case. They are intended for general purpose and amplifier applications.

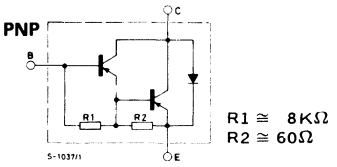
ABSOLUTE MAXIMUM RATINGS

		PNP* / NPN	MJ11011 / MJ11012	MJ11013 / MJ11014	MJ11015 / MJ11016
V_{CBO}	Collector-base voltage ($I_E = 0$)		60V	90V	120V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)		60V	90V	120V
V_{EBO}	Base-emitter voltage ($I_C = 0$)			5V	
I_C	Collector current			30A	
I_B	Base current			1A	
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$			200W	
T_{stg}	Storage temperature			-65 to 200°C	
T_j	Junction temperature			200°C	

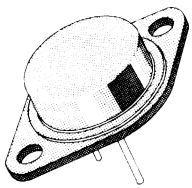
* For PNP types voltage and current values are negative

INTERNAL SCHEMATIC DIAGRAMS





TO-3



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	0.87	°C/W

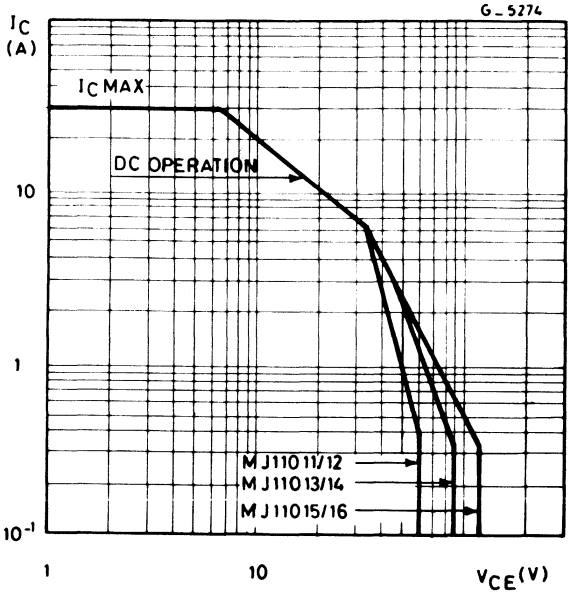
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector cutoff current ($I_B = 0$)	$V_{CE} = 50V$			1	mA
I_{EBO}	Emitter cutoff current ($I_C = 0$	$V_{EB} = 5V$			5	mA
I_{CER}	Collector cutoff current ($R_{BE} = 1K\Omega$)	V_{CE} = rated V_{CEO} $T_{case} = 150°C$ V_{CE} = rated V_{CEO}			1 5	mA mA
$V_{CEO(sus)}$*	Collector-emitter sustaining voltage ($I_B = 0$)	$I_C = 100mA$ **MJ11011, MJ11012** **MJ11013, MJ11014** **MJ11015, MJ11016**			 60 90 120	 V V V
h_{FE}*	DC current gain	$I_C = 20A$ $V_{CE} = 5V$ $I_C = 30A$ $V_{CE} = 5V$	1000 200			— —
$V_{CE(sat)}$*	Collector-emitter saturation voltage	$I_C = 20A$ $I_B = 200mA$ $I_C = 30A$ $I_B = 300mA$			3 4	V V
$V_{BE(sat)}$*	Base-emitter saturation voltage	$I_C = 20A$ $I_B = 200mA$ $I_C = 30A$ $I_B = 300mA$			3.5 5	V V
h_{fe}	Small signal current gain	$I_C = 10A$ $V_{CE} = 3V$ $f = 1MHz$	4			—

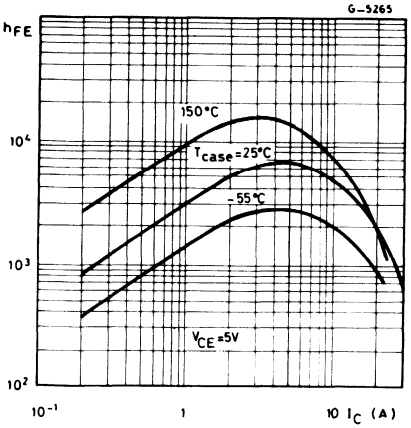
* Pulsed: pulse duration = 300 μs, duty cycle $\leqslant 1.5\%$

For PNP devices voltage and current values are negative

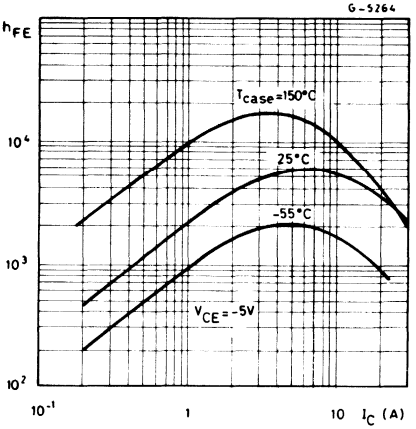
Safe operating areas



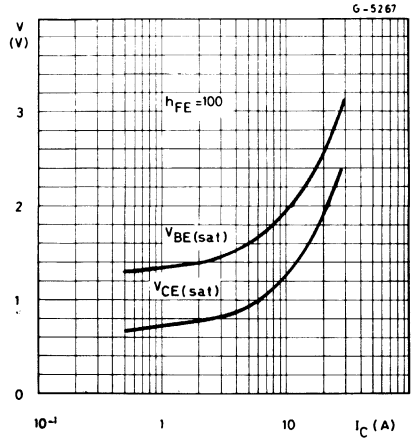
DC current gain (NPN types)



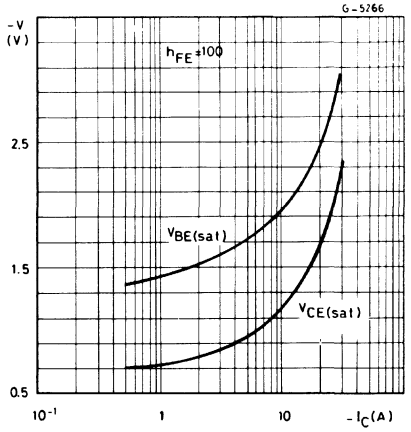
DC current gain (PNP types)



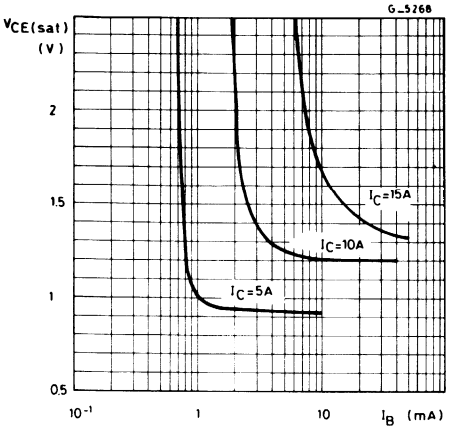
Saturation voltages (NPN types)



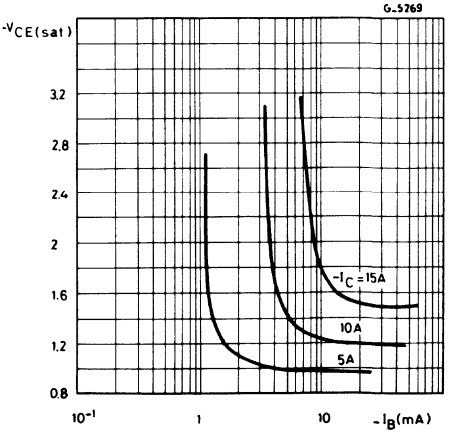
Saturation voltages (PNP types)



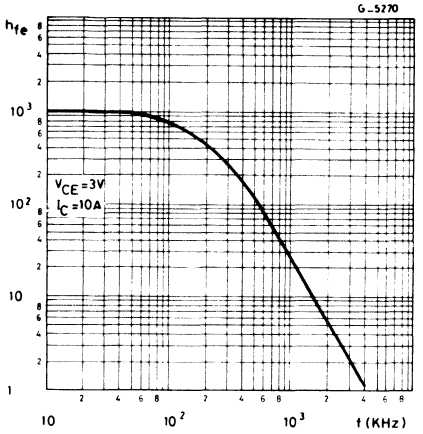
Collector-emitter saturation voltage (NPN types)



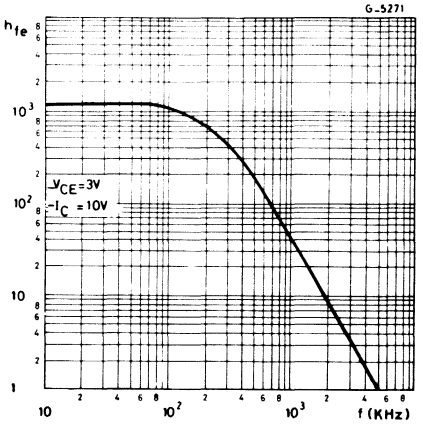
Collector-emitter saturation voltage (PNP types)



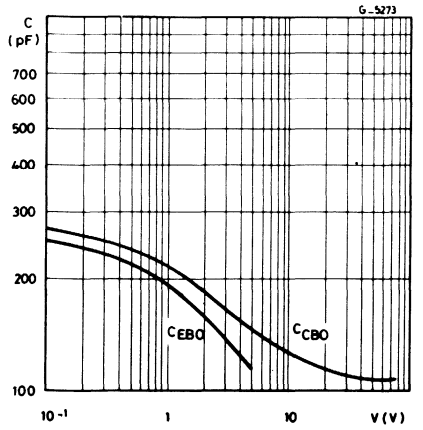
Small signal current gain (NPN types)



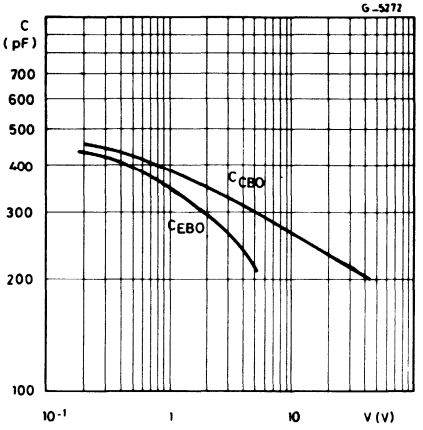
Small signal current gain (PNP types)



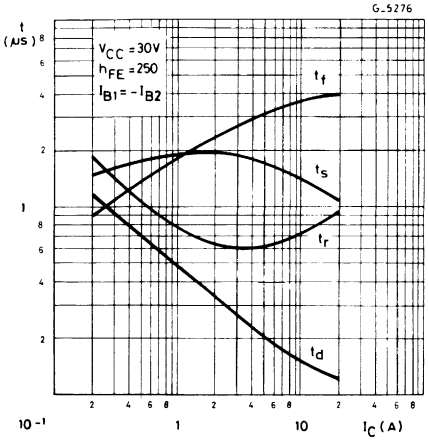
Capacitances (NPN types)



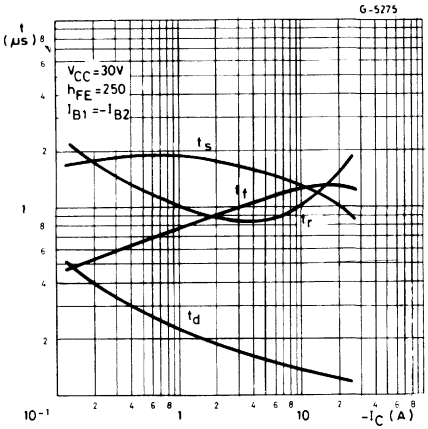
Capacitances (PNP types)



Saturated switching times (NPN types)



Saturated switching times (PNP types)



MTH40N06
MTH40N06P

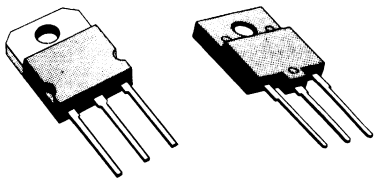
HIGH SPEED SWITCHING APPLICATIONS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
MTH40N06	60 V	0.028 Ω	40 A
MTH40N06P	60 V	0.028 Ω	26 A

- N- CHANNEL POWER MOS TRANSISTORS
- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO

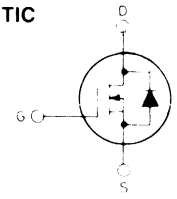
AUTOMOTIVE POWER APPLICATIONS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. They also find use in DC/DC converters and uninteruptable power supplies.



TO-218 ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-218 / ISOWATT218	MTH40N06 / MTH40N06P	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	V
V_{DGR}	Drain-gate voltage ($R_{GS}=1$ MΩ)		60	V
V_{GS}	Gate-source voltage		±20	V
I_{DM}	Drain current (pulsed)		200	A
I_{GM}	Gate current (pulsed)		1.5	A
		TO-218	**ISOWATT218**	
I_D ■	Drain current (cont.) $T_c=20°C$	40	26	A
P_{tot} ■	Total dissipation at $T_c<25°C$	150	65	W
■	Derating factor	1.2	0.52	W/°C
T_{stg}	Storage temperature		−55 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT 218 in this datasheet

THERMAL DATA ■

			TO-218	ISOWATT218	
$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	0.83	1.92	°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 100 μA V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating X 0.85 V_{DS} = Max Rating X 0.85 T_c = 100°C			250 2500	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 20 A			0.028	Ω
$V_{DS\ (on)}$	Drain-source on voltage	V_{GS} = 10V I_D = 40 A V_{GS} = 10V I_D = 20 A T_c = 100°C			1.32 1.12	V V
DYNAMIC						
g_{fs} *	Forward transconductance	V_{DS} = 15V I_D = 20A	10			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1MHz V_{GS} = 0			5000 2500 1000	pF pF pF

* Pulsed: Pulse duration ≤ 300μs, duty cycle ≤2%

■ See Note on ISOWATT218 in this datasheet

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 25 V I_D = 20A			50	ns
t_r	Rise time	R_{gen} = 50 Ω			300	ns
$t_{d\ (off)}$	Turn-off delay time				150	ns
t_f	Fall time				100	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = 40 A V_{GS} = 0			1	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A V_{GS} = 0			150	ns
t_{on}	Forward turn-on time				200	ns

ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT218 is fully isolated to 4000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.
The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs. Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance.
ISOWATT218 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWERMOS can be calculated:

$$I_{Dmax} = \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of a transistor heatsink assembly, using ISOWATT218 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

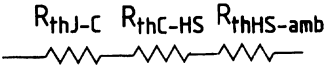
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

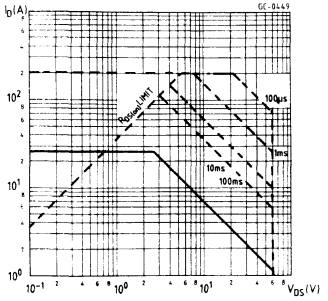
$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

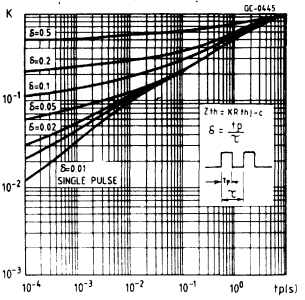
Fig. 1



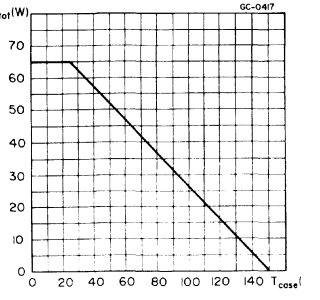
Safe operating areas



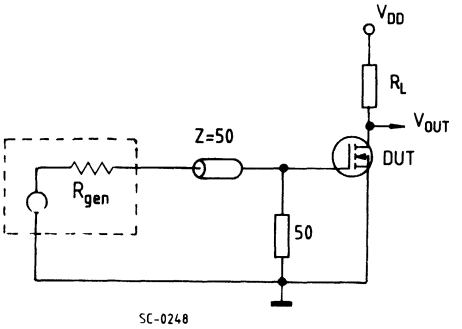
Thermal impedance



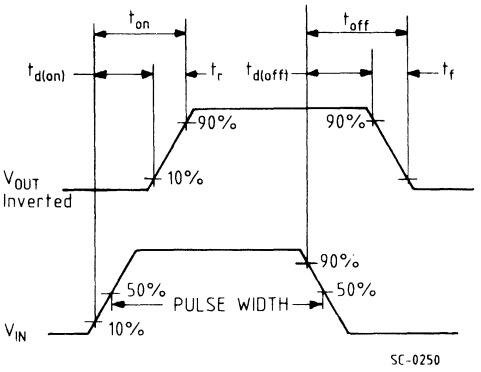
Derating curve



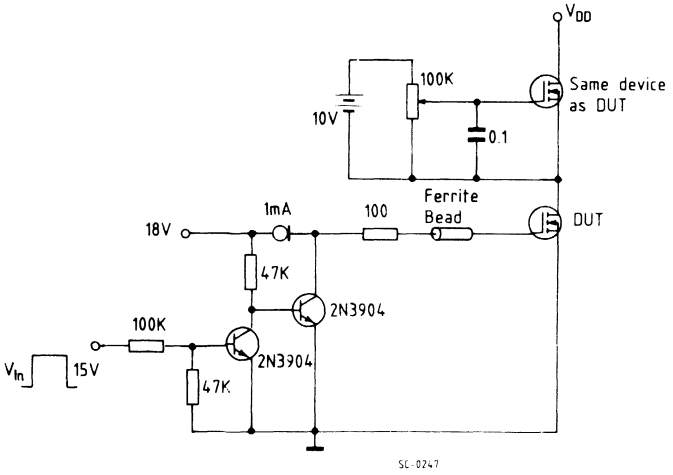
Switching times test circuit



Switching times wawerform

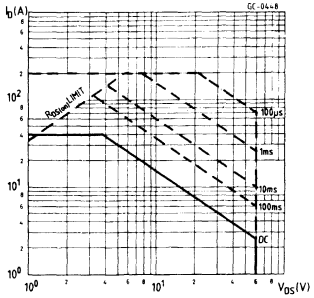


Gate charge test circuit

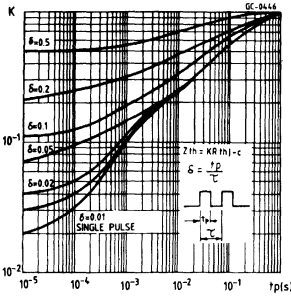


MTH40N06
MTH40N06P

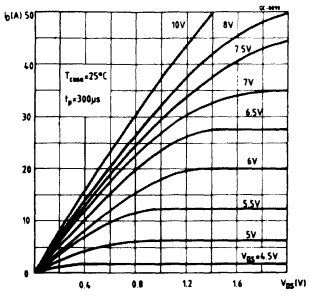
Safe operating areas



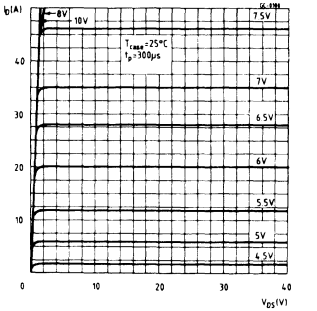
Thermal impedance



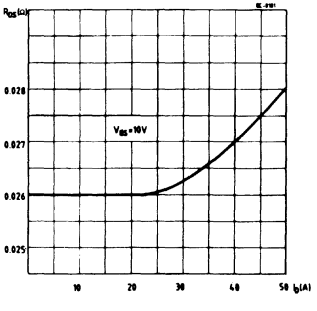
Output characteristics



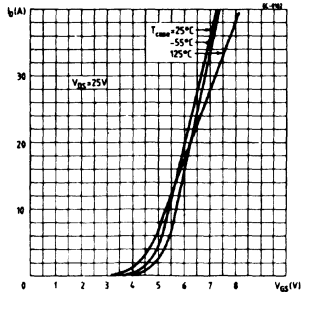
Output characteristics



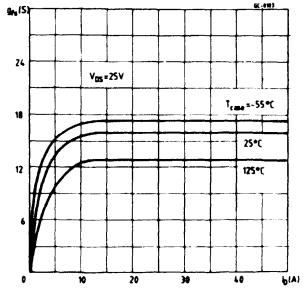
Static drain-source on resistance



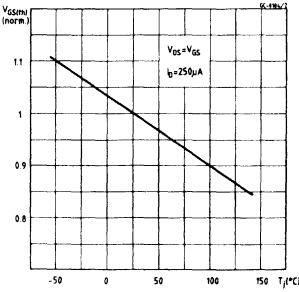
Transfer characteristics



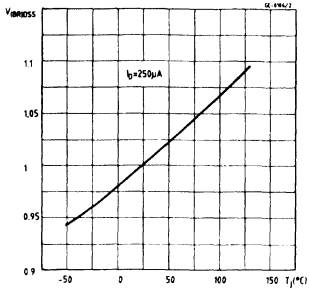
Transconductance



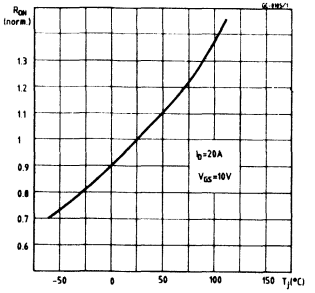
Normalized gate threshold voltage vs temperature



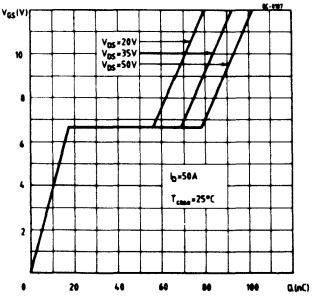
Normalized breakdown voltage vs temperature



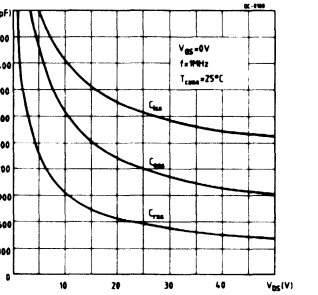
Normalized on resistance vs temperature



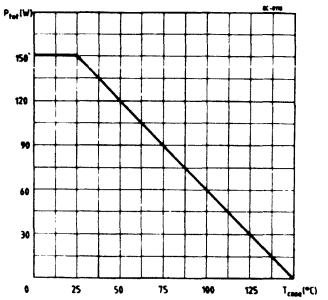
Gate charge vs gate source voltage



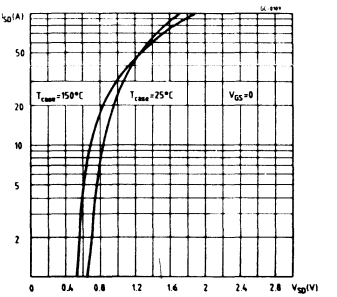
Capacitance variation



Derating curve



Source-drain diode forward characteristics



MTP3055A
MTP3055AP

HIGH SPEED SWITCHING APPLICATIONS

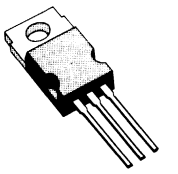
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
MTP3055A	60 V	0.15 Ω	12 A
MTP3055AP	60 V	0.15 Ω	10 A

- N- CHANNEL POWER MOS TRANSISTORS
- ULTRA FAST SWITCHING - UP TO >100KHz
- LOW DRIVE ENERGY FOR EASY DRIVE REDUCED SIZE AND COST
- INTEGRAL SOURCE - DRAIN DIODE

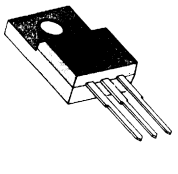
INDUSTRIAL APPLICATIONS:

- GENERAL PURPOSE SWITCH
- SERIES REGULATOR

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators lamp driving, series regulator and many other uses in industrial control applications. They also find use in DC/DC converters and uninterruptable power supplies.

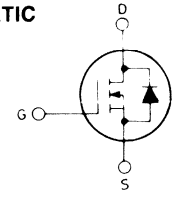


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	MTP3055A / MTP3055AP	
V_{DS}	Drain-source voltage (V_{GS} = 0)		60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		60	V
V_{GS}	Gate-source voltage		±20	V
I_{DM}	Drain current (pulsed)		26	A
I_{GM}	Gate current (pulsed)		1.5	A
		TO-220	**ISOWATT220**	
I_D ■	Drain current (continuous)	12	10	A
P_{tot} ■	Total dissipation at T_c <25°C	40	30	W
■	Derating factor	0.32	0.24	W/°C
T_{stg}	Storage temperature		−65 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
T_l	Maximum lead temperature for soldering purpose		275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 V	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 6A			0.15	Ω
$V_{DS\ (on)}$	Drain-source on voltage	V_{GS} = 10V I_D = 12A V_{GS} = 10V I_D = 6A V_{GS} = 10V I_D = 6A T_c = 100°C			2.0 0.9 1.5	V V V
DYNAMIC						
g_{fs} *	Forward transconductance	V_{DS} = 10V I_D = 6A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1MHz V_{GS} = 0			500 200 100	pF pF pF
Q_g	Total gate charge	V_{DS} = 48 V I_D = 12A V_{GS} = 10 V			17	nC

* Pulsed: Pulse duration ≤ 300μs, duty cycle ≤ 2%

■ See note on ISOWATT220 in this datasheet

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	$V_{DD} = 25$ V $I_D = 6$A			20	ns
t_r	Rise time	$R_{gen} = 50\ \Omega$			60	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)			65	ns
t_f	Fall time				65	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	$I_{SD} = 12$ A $V_{GS} = 0$			2	V
t_{rr}	Reverse recovery time	$I_{SD} = 12$ A $V_{GS} = 0$			80	ns
t_{on}	Forward turn-on time				75	ns

MTP3055A
MTP3055AP

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} = \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

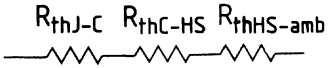
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

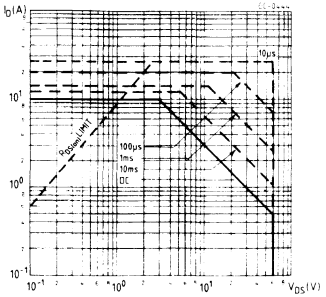
$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

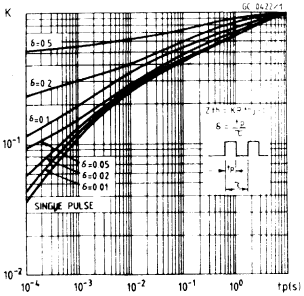
Fig. 1



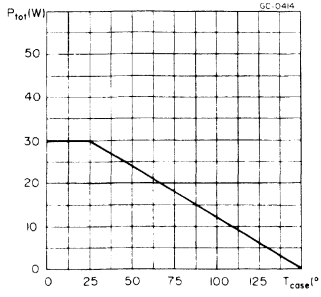
Safe operating areas



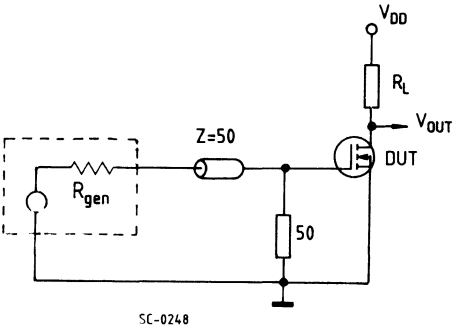
Thermal impedance



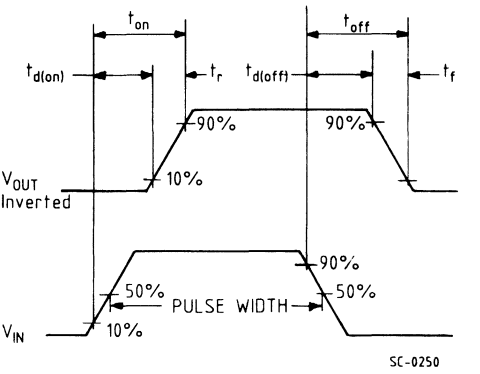
Derating curve



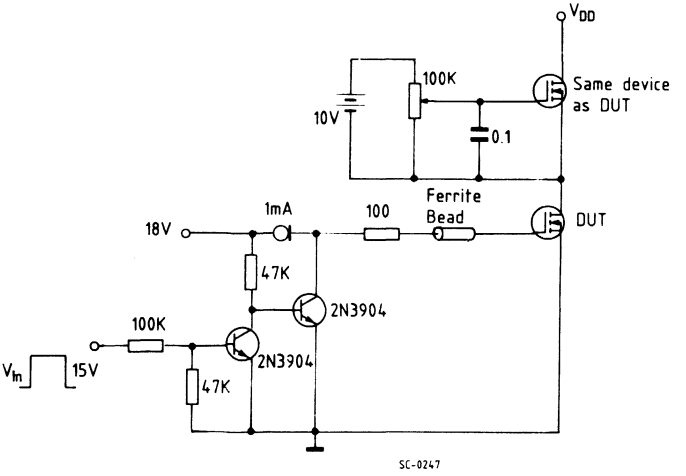
Switching times test circuit



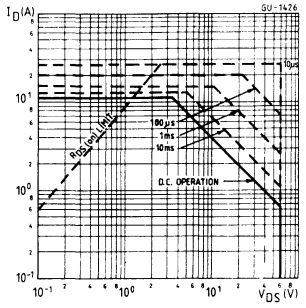
Switching times wawerform



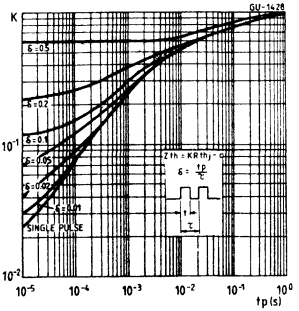
Gate charge test circuit



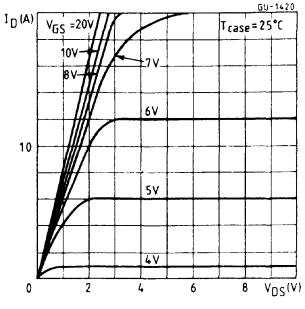
Safe operating areas



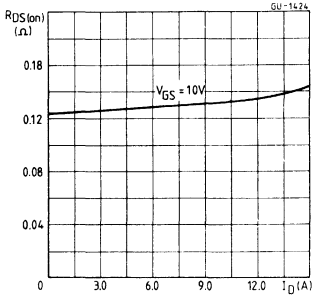
Thermal impedance



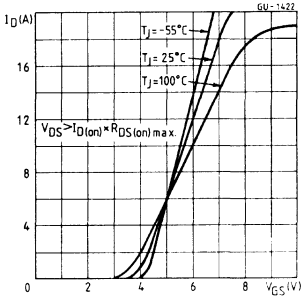
Output characteristics



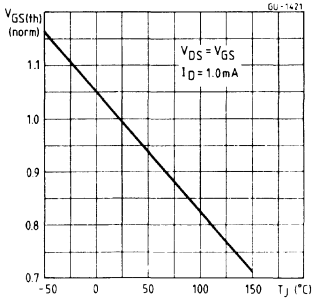
Static drain-source on resistance



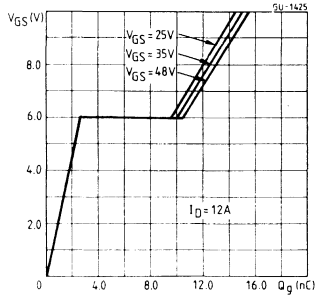
Transfer characteristics



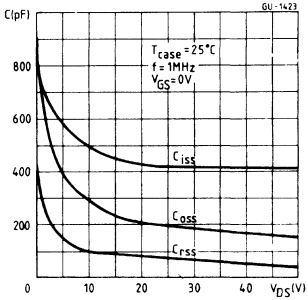
Gate threshold voltage vs temperature



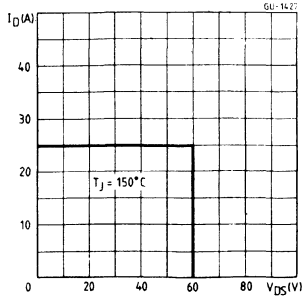
Gate charge vs gate to source voltage



Capacitance variation



Maximum rated switching safe operating areas



TIP140 TIP145
TIP141 TIP146
TIP142 TIP147

POWER DARLINGTONS

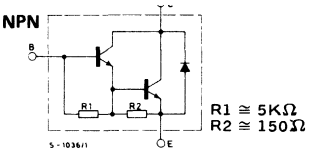
The TIP140, TIP141, TIP142 are silicon epitaxial base NPN transistors in monolithic Darlington configuration and are mounted in SOT-93 plastic package. They are intended for use in power linear and switching applications.
The complementary PNP types are TIP145, TIP146, TIP147 respectively.

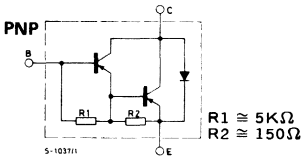
ABSOLUTE MAXIMUM RATINGS

		NPN *PNP	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147
V_{CBO}	Collector-base voltage ($I_E = 0$)		60V	80V	100V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)		60V	80V	100V
V_{EBO}	Emitter base voltage ($I_C = 0$)			5V	
I_C	Collector current			10A	
I_{CM}	Collector peak current (repetitive)			20A	
I_B	Base current			0.5A	
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$			125W	
T_{stg}	Storage temperature			-65 to 150°C	
T_j	Junction temperature			150°C	

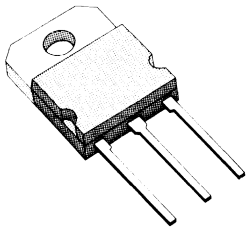
* For PNP types voltage and current values are negative.

INTERNAL SCHEMATIC DIAGRAMS





SOT-93 (TO-218)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1	°C/W

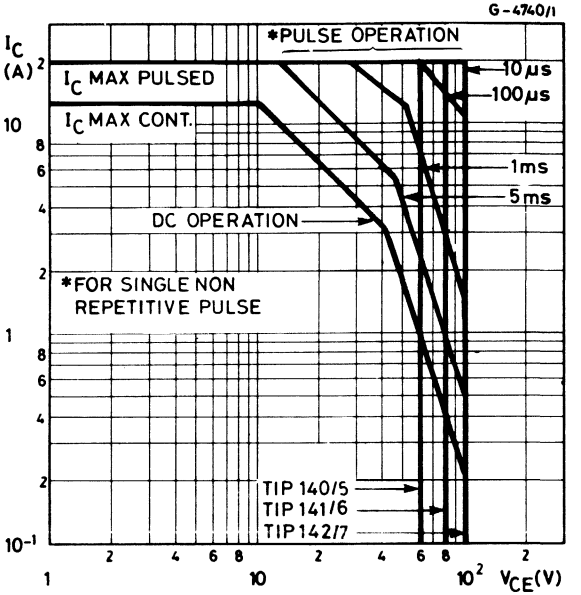
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	for **TIP140/5** V_{CB} = 60V for **TIP141/6** V_{CB} = 80V for **TIP142/7** V_{CB} = 100V			1 1 1	mA mA mA
I_{CEO}	Collector cutoff current (I_B = 0)	for **TIP140/5** V_{CB} = 30V for **TIP141/6** V_{CE} = 40V for **TIP142/7** V_{CE} = 50V			2 2 2	mA mA mA
I_{EBO}	Emitter cutoff current (I_C = 0)	V_{EBO} = 5V			2	mA
$V_{CEO\ (sus)}$*	Collector emitter sustaining voltage (I_B = 0)	I_C = 30 mA for **TIP140/5** for **TIP141/6** for **TIP142/7**	60 80 100			V V V
$V_{CE\ (sat)}$*	Collector-emitter saturation voltage	I_C = 5A I_B = 10 mA I_C = 10A I_B = 40 mA			2 3	V V
V_{BE}*	Base-emitter voltage	I_C = 10A V_{CE} = 4V			3	V
h_{FE}*	DC current gain	I_C = 5A V_{CE} = 4V I_C = 10A V_{CE} = 4V	1000 500			– –
t_{on}	Turn-on time	I_C = 10A I_{B1} = 40 mA I_{B2} = -40 mA R_L = 3Ω		0.9		μs
t_{off}	Turn-off time			4		μs

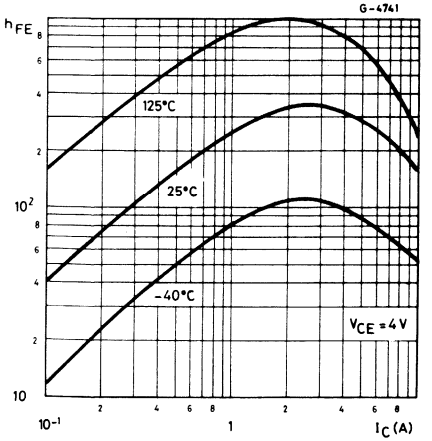
* Pulsed: pulse duration = 200 μs, duty cycle = 1.5%.

For PNP devices voltage and current values are negative

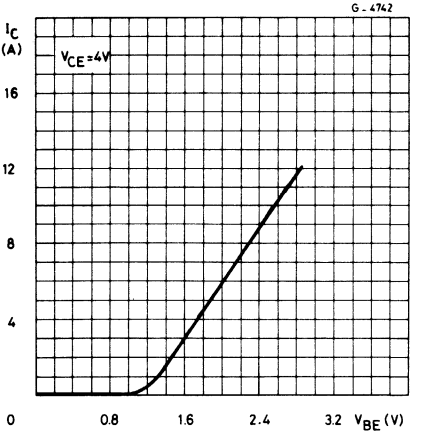
Safe operating areas



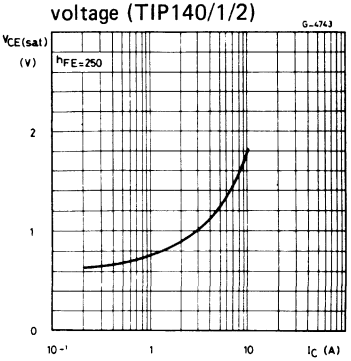
DC current gain (TIP140/1/2)



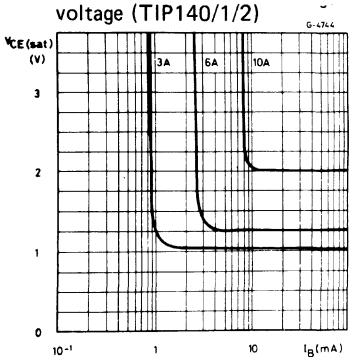
DC transconductance (TIP140/1/2)



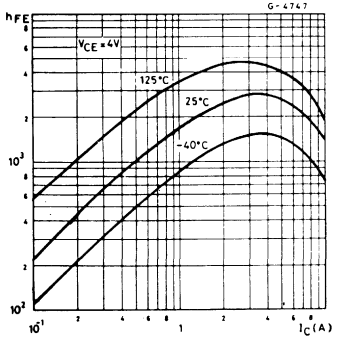
Collector-emitter saturation voltage (TIP140/1/2)



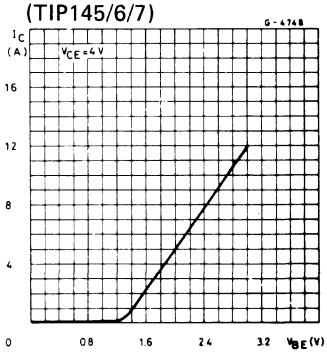
Collector-emitter saturation voltage (TIP140/1/2)



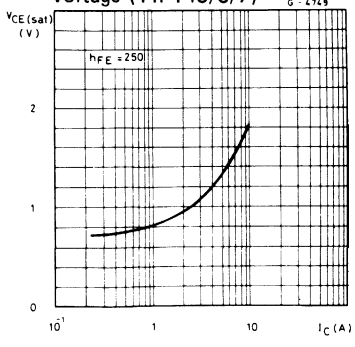
DC current gain (TIP145/6/7)



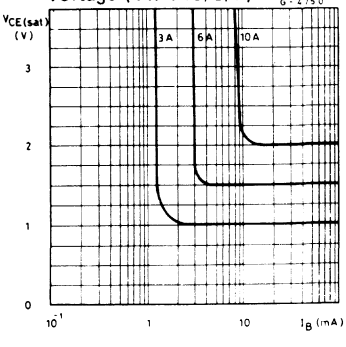
DC transconductance (TIP145/6/7)



Collector-emitter saturation voltage (TIP145/6/7)

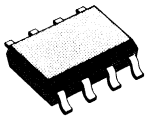


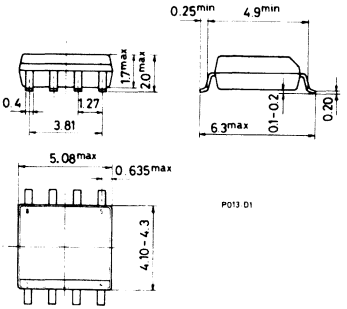
Collector-emitter saturation voltage (TIP145/6/7)



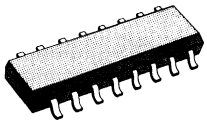
PACKAGES

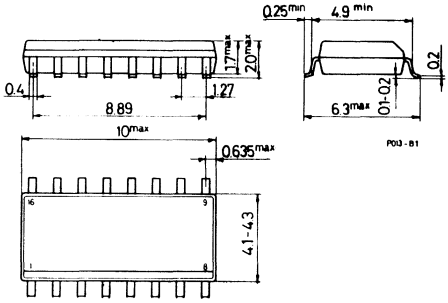
SO-8



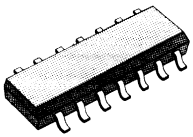


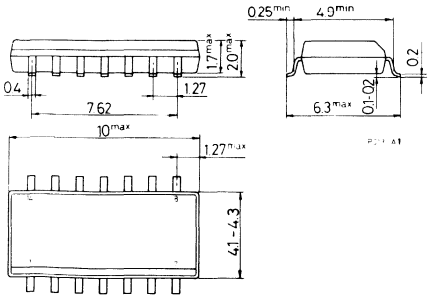
SO-16J



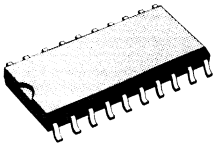


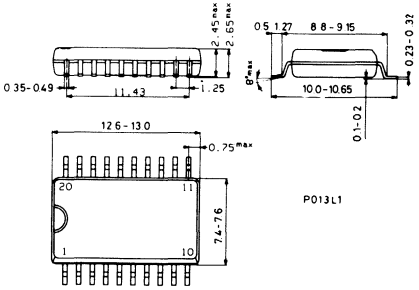
SO-14J





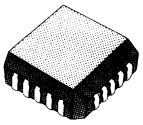
SO-20L

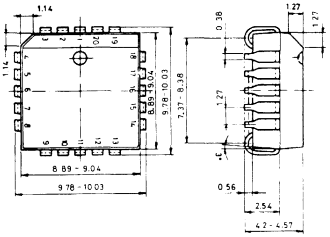




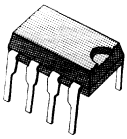
PACKAGES

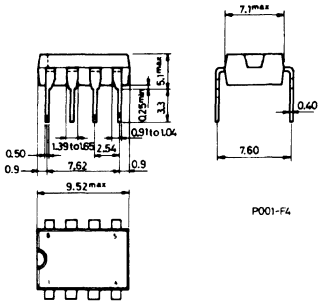
PLCC-20 Plastic Chip Carrier
PLCC 15 + 15



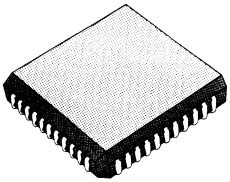


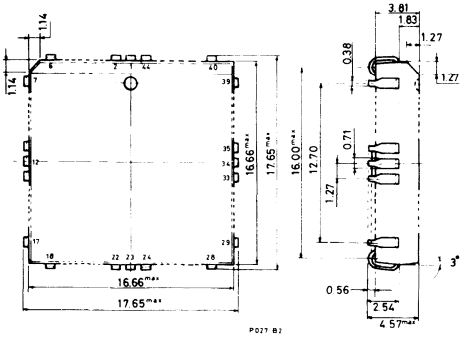
8 lead Plastic Minidip
4 + 4 lead Powerdip



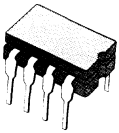


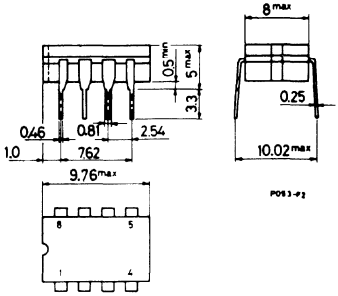
PLCC-44 Plastic Chip Carrier



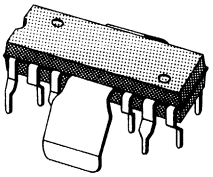


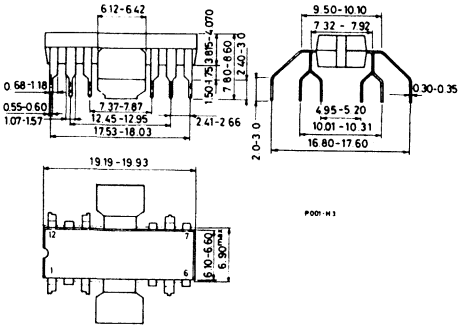
8 lead Ceramic Minidip



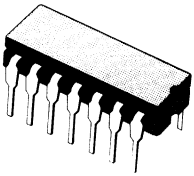


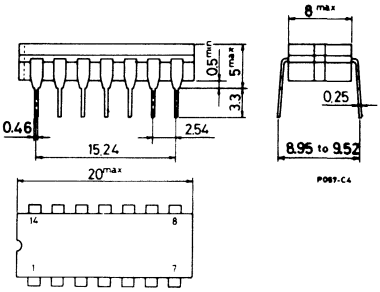
Findip



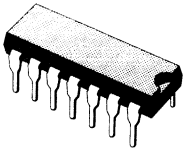


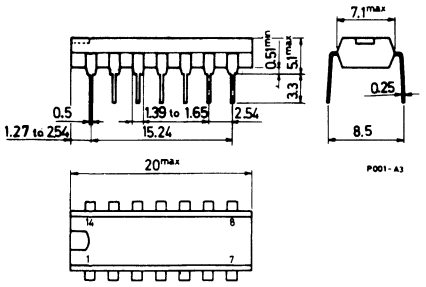
14 lead Ceramic Dip



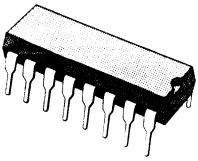


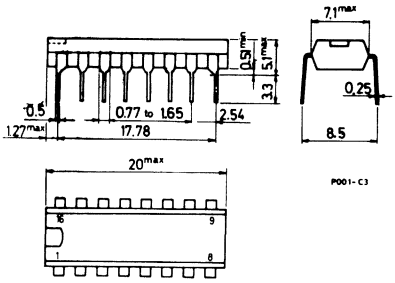
14 lead Plastic Dip





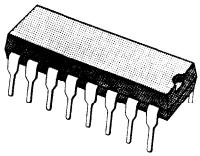
16 lead Plastic Dip (0.25)

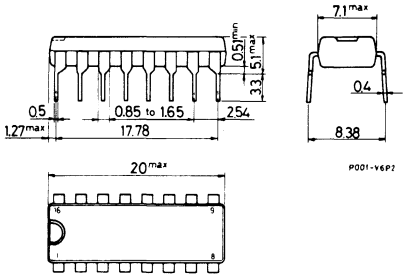




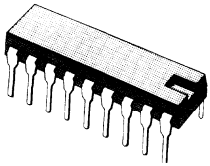
PACKAGES

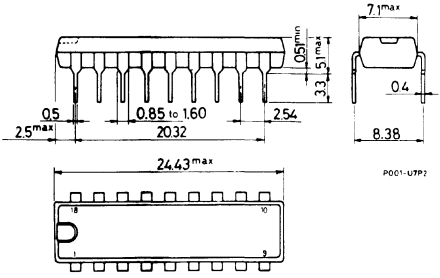
16 lead Plastic Dip (0.4)
8 + 8 lead Powerdip
12 + 2 + 2 lead Powerdip



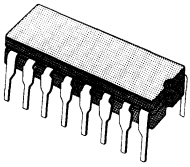


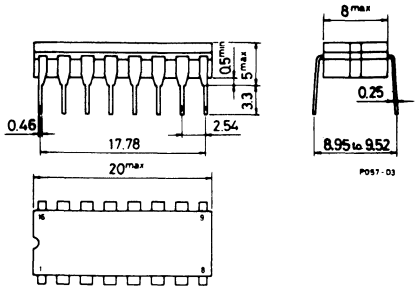
18 lead Plastic Dip
12 + 3 + 3 lead Powerdip
9 + 9 lead Powerdip



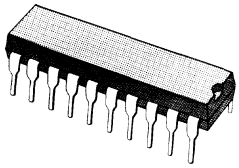


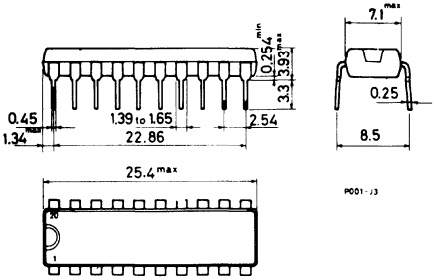
16 lead Ceramic Dip



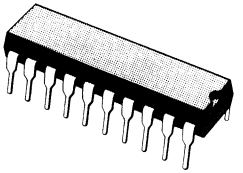


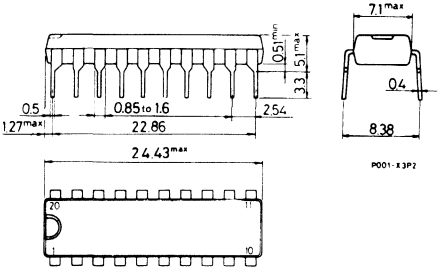
20 lead Plastic Dip (0.25)



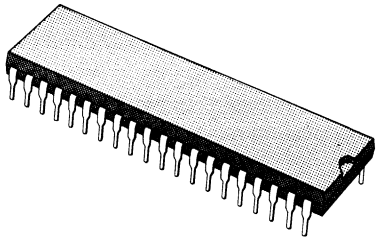


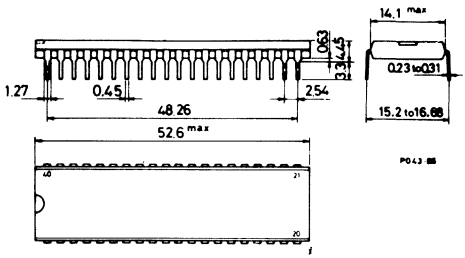
20 lead Plastic Dip (0.4)
16 + 2 + 2 Powerdip



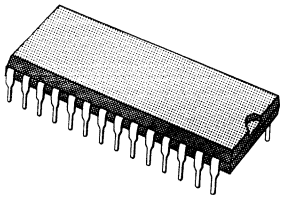


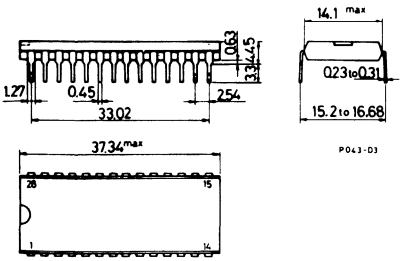
40 lead Plastic Dip



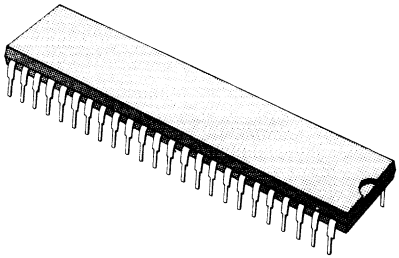


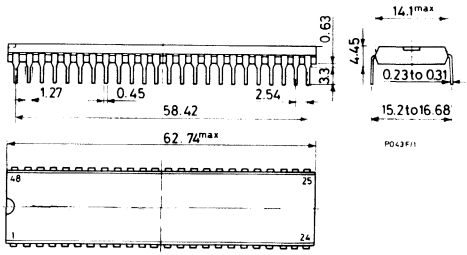
28 lead Plastic Dip





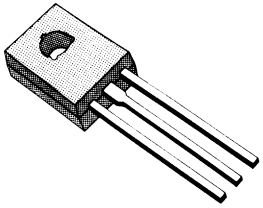
48 lead Plastic Dip

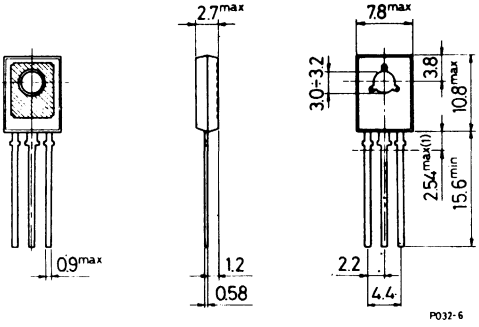




PACKAGES

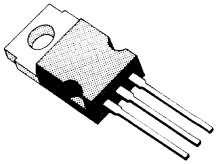
SOT-32 (TO-126)

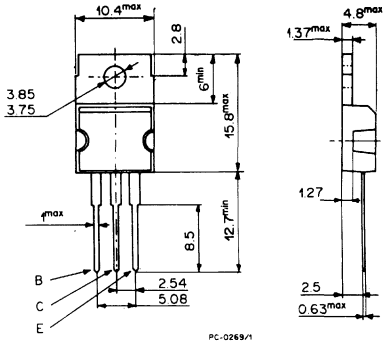




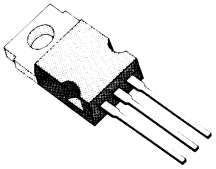
(1) Within this region the cross-section of the leads is uncontrolled

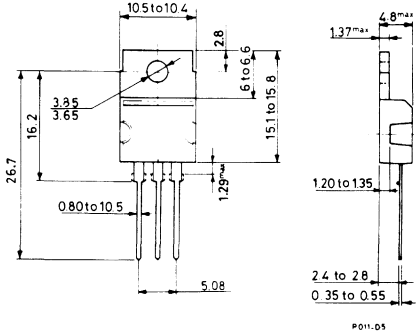
TO-220 (Discrete Power)



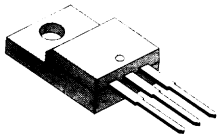


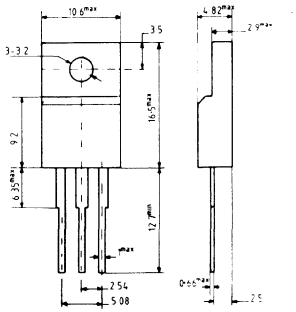
TO-220 (ICs)



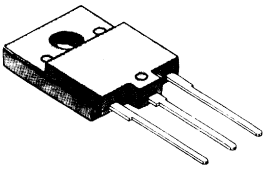


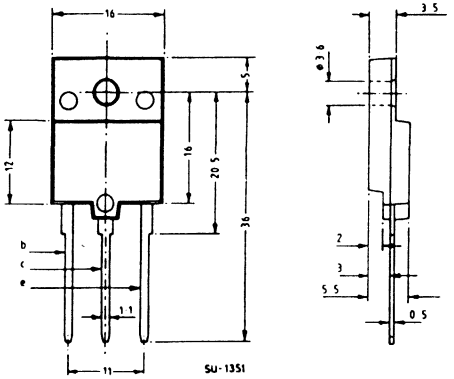
ISOWATT 220



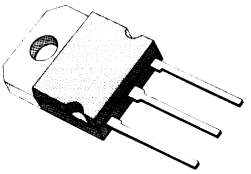


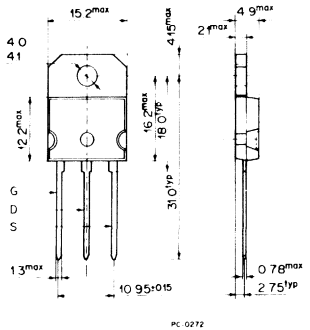
ISOWATT218



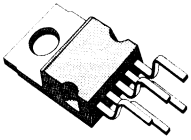


SOT-93 (TO-218)

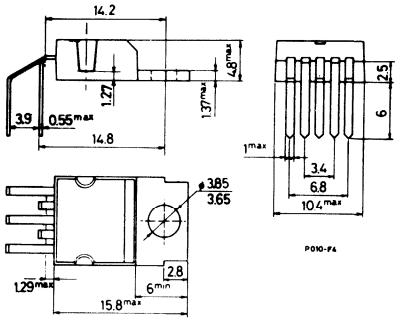




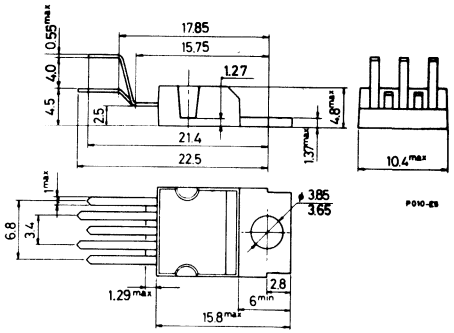
PENTAWATT



Horizontal Version

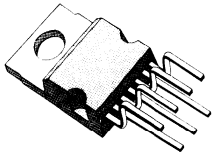


Vertical Version



PACKAGES

HEPTAWATT



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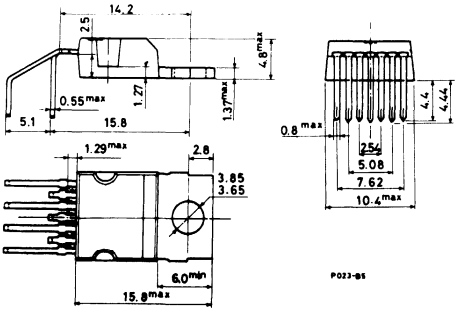

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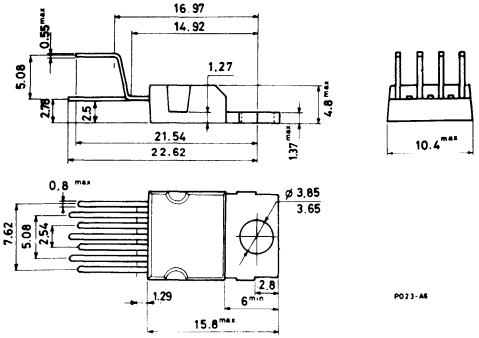

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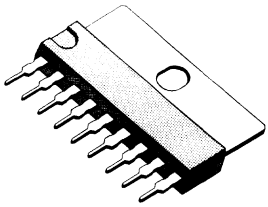

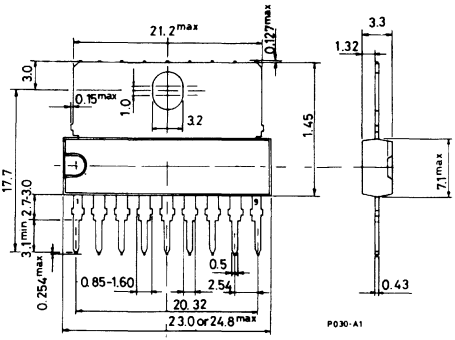

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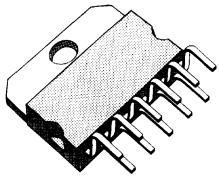

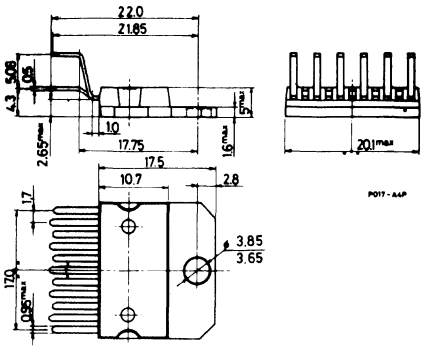

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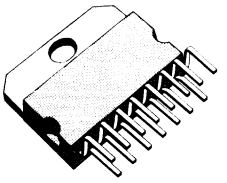

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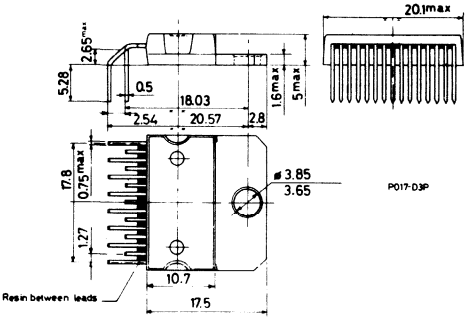

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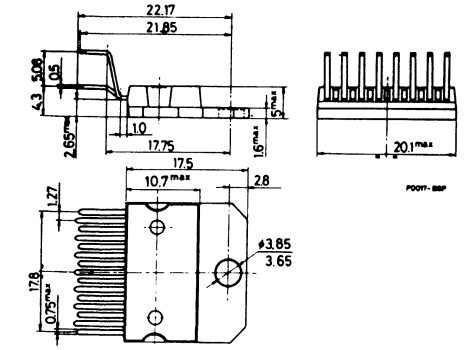
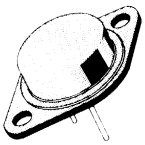
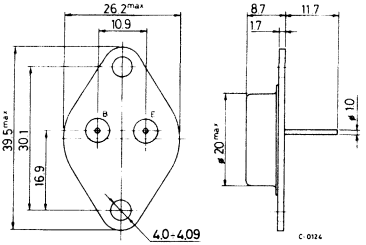


TO-3





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